YAMAR Electronics Ltd
Preliminary *Data Sheet*

QDC10 - Multiplex Data On Battery Power Lines

The information in this data sheet is preliminary and may be changed without notice. January 2002

1 GENERAL

The QDC10 is a VLSI device for Data communication over noisy DC power lines to eliminate complex wiring and provide quick and simple installation. If required, the device can operate on a single wire bus. It is a complete solution to multiplex commands and data between wide range of modules in a vehicle such as Climate Control and its Temperature sensors, Security detectors and Immobilizers, Car Audio components, Remote operation buttons on the steering wheel, etc.

The QDC10 is based on a patented DC-BUS™ technology. It contains a Modem, Channel Coder/decoder (ECC), Communication Controller to overcome the hostile environment on vehicle battery lines.

Applications

- **Vehicle Electronics**
- **Security Systems**
- **Car Audio Control**
- **Climate Control**
- **Navigation Systems**

Features

- **Noise Robust, 10Kbps Communication on Battery Power Lines**
- **Peer to Peer, Up to 16 Devices, 2-16 bytes Packet Message**
- **Low Cost, Flexible, Eliminates Complex Cabling, Saves installation**
- **Sleep Mode for Low Power Consumption**
- **Opens New Dimensions for Car Electronics Design**
- **Data Bandwidth can be Shared dynamically Between active devices**

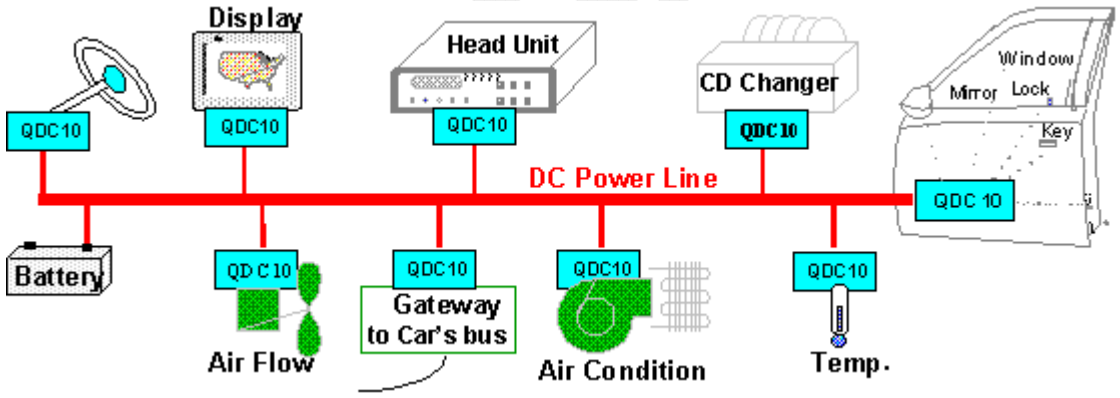


Figure 1.1 - Typical QDC10 Applications

2 OVERVIEW

2.1 DC-BUS™ System

A QDC10 network serves up to 16 devices, each of them can broadcast data messages to other devices on the bus. The device can be interfaced and controlled by a Host microprocessor via a serial synchronous communication. Simple applications, such as switches can be implemented directly on the device eliminating the need of a host. The DC-BUS is a Carrier Sense Multiple Access (CSMA) Collision detection / resolving system. It uses a dedicated frequency for Data and Control transfer between

devices. The rest of the spectrum is reserved for higher speed channels and for multimedia communication over the same DC power lines.

2.1.1 QDC10 Channel

The QDC10 channel is designed to operate over a single DC power line in the noisy conditions of a car. Up to 16 devices can be connected on a DC line.

Center frequency F0: 1.79 MHz
Data transfer rate: 10 Kbps.
Cable length: Up to 12m on DC cable.

2.2 QDC10 Device

The QDC10 device is responsible to receive and transfer messages to and from destination devices. A message consists of 2 to 16 data bytes. The device handles the communication physical layer and part of link layer (Modem, Channel coder, Carrier sense, Collision detection, and basic protocol).

The QDC10 device consists of a serial synchronous Host interface for communication with its Host, Transmit and receive buffers, channel coder for error correction handling and a modem for line communication. The device has special carrier detection logic and protocol handling logic. Figure 1.2 outlines the building blocks of the QDC10 device.

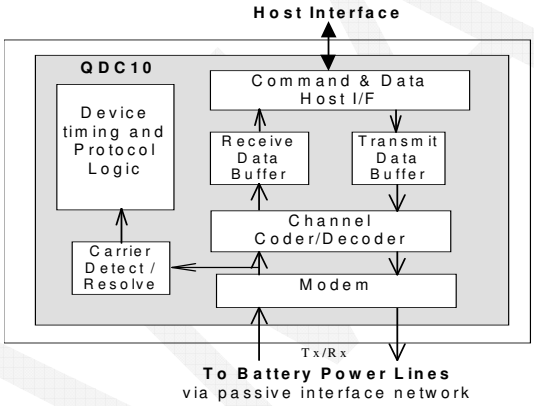


Figure 2.1 - QDC10 logical blocks

2.2.1 Device Ports

The QDC10 has the following ports:
Host Interface - A serial interface using 3 lines between the device and its Host micro-controller.
DC Line - Two lines for connection to and from the DC line interface or single wire bus.

2.2.2 Protocol

The communication is performed in messages. Each message starts with a header byte, followed by up to 16 bytes of data. The device and its host coordinate message transmission, message reception, entering Sleep mode and Wake-Up.. Higher level protocol (link and application layers) are under the responsibility of the system designer.

2.2.3 Error Correction

Data is protected by an Error correction mechanism designed to meet impulse burst noises with characteristic similar to those existing over the DC power lines.

2.2.4 Power Management

A Sleep mode, controlled by the Host, saves power by disabling most of the circuits. The device enters into Sleep mode by a Host Sleep command. While in Sleep mode the device is periodically switched to receive mode to sense for activity on the bus. If an activity is detected the device and its Host wake up. Else, If an activity is not detected, the device returns to the Sleep mode. A transition on the serial DataIn pin caused by the Host wakes the device as well.

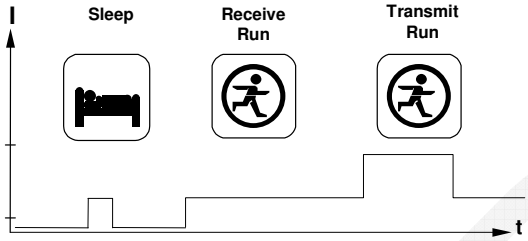


Figure 2.2 - Operation modes

3 OPERATION

The QDC10 implements the physical layer and the MAC layer of the OSI data communication model. The Host is responsible for the implementation of the link and application layers. The following paragraph describes the operation of the QDC10 device.

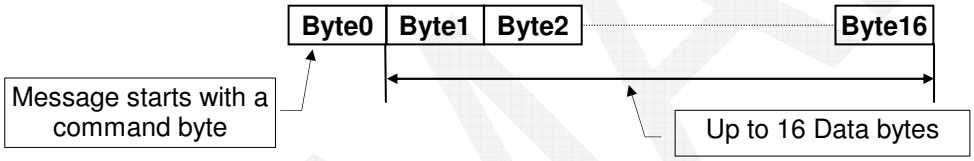


Figure 3.1 - Message construction

3.1 Message Construction

The Host constructs a message with a header byte that describes the message content (Command or Data), followed by 2 to 16 data bytes of data (when applicable).

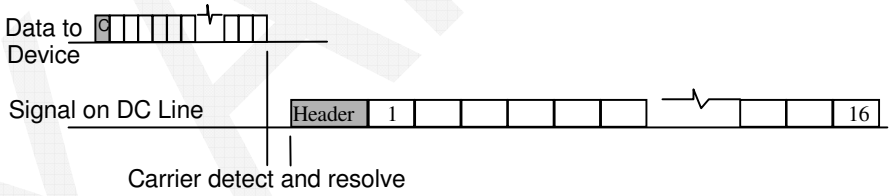


Figure 3.2 - Message delay

3.2 Transmit Mode

Transmission procedure is initiated by the host by a TxData or TxWakeData command followed by data bytes. The device starts the transmission with an arbitration procedure used in order to detect and resolve collisions on the channel. The arbitration procedure consists of a pattern of time slots, each dedicated for transmission or for sensing of the DC-BUS. If the device senses a transmission during the arbitration procedure it aborts the transmission. If the device succeeds to access the channel, the device continues the transmission of a preamble sequence, followed by the rest of the coded message and returns a TxAck to its host (which means that the transmission is over). If the device fails in resolving the channel, it switches to Receive mode and receives a message (or RxError). If the device does not return TxAck within 40mS, the Host (application) may wait a random period of time (to avoid collisions) and send the message again to the device.

3.3 Receive Mode

Upon detection of a legal header, a message with a header and up to 16 data bytes will be received into the device internal buffer. The device indicates the Host that a message is ready by raising the DataOut signal. The Host has to read that message in 2mS to enable reception of a new message from the bus.

3.4 Sleep Mode

The Host can command the device to enter into sleep mode (e.g. when no signal is received or transmitted for a time period defined by the application). The device wakes up every 18mS to detect activity on the bus. A change on the DataIn signal will also wake-up the device. When the bus is quiescent and the device needs to transmit a message to the bus, the Host has to send a TxWakeData command. The TxWakeData command has a long preamble, to allow all other devices on the bus to wake-up during the preamble and before the data is transmitted.

3.5 Controlling the QDC10

3.5.1 Data from Host to QDC10

The QDC10 device is controlled by a set of commands as listed in table 3.1. Data transmission starts after the Host finishes to transfer the command byte and the data bytes into the QDC10 internal transmit buffer.

3.5.2 Command Set

Host controls the QDC10 device with the following set of commands:

Table 3.1 - Command Set

Command	Code	Description
TxData	F**x**h	Transmit the following 16-x bytes of data (2-16)
TxWakeData	8**x**h	Transmit a long header followed by 16-x bytes of data (2-16)
Reset	01h	Restart the QDC10
Sleep	02h	QDC10 enter to Sleep mode

For the value of **x** - see table 3.3

3.5.3 Data from QDC10 to Host

When QDC10 device receives a message from the DC-BUS, data errors are corrected and sent to the Host via a synchronous protocol. A header byte indicates the Host of a data transfer. The following table describes the formats of data transferred to the Host.

Table 3.2 - Device response header

Header	Code	Description
RxData	F**x**h	Receive the following 16-x bytes of Data
TxAck	40h	Message transmission completed
TxWakeAck	40h	Message transmission completed
Reset	01h	Reset operation was performed
Sleep	02h	The device entered to Sleep mode
RxError	04h	Corrupted message received. (Would not be transferred to Host)

For the value of **x** - see table 3.3

Table 3.3 - Transmit/Receive number of data bytes conversion table

bytes	-	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
x	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

Notice:

1. The Host has to begin reading data from the QDC10 within 2mS after the rise of DataOut and finish reading it within 10mS in order not to miss a new message on the DC-BUS.

2. Device responds to Reset and Sleep within 30uS after the command is received. In such case DataOut rises for byte transfer very quickly. The device responds to Tx command (TxAck) within 30mS.

3. Host has to read device response (Reset, Sleep, TxAck, etc.) within 2mS, otherwise the device may miss a new message.

4. Transmit of one byte (RxData=FFh) is an illegal command.

4 SIGNALS

Device signals are defined in table 4.1.

Table 4.1 - Device signals

Signal Name	I/O	Description	Pin
DataIn	I	Serial Data input (for transmission)	6
DataOut	O	Serial Data output	13
ClockIn	I	Synchronous data transfer Host Clock	12
TxData	O	Transmit signal	7
RxData	I	Received signal	17
TxEnable	O	When high, Transmit signal is enabled	8
~Reset	I	Reset device	4
RxEnable	O	When high, Receive signal is enabled	2
OscIn	I	Crystal In	16
OscOut	O	Crystal Out	15
Res6	I	SSI Operation – connect to Ground	18
Other I/O		Application dependent	

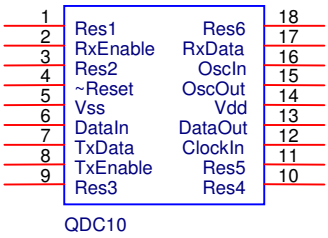


Figure 4.1 - Device Pin-out

4.1 Host interface

4.1.1 Host Interface Ports

Three lines control the operation of the Host interface. The QDC10 device receives and sends data in bytes, MSB bit first.

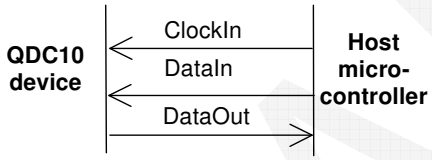


Figure 4.2 - Host Interface signals

4.1.1.1 ClockIn

Clock signal from the Host for the synchronous interface.

4.1.1.2 DataIn

Data input signal to the QDC10.
1) Transfer Data from Host to QDC10 during the falling edge of ClockIn signal.
2) When high, indicates to the QDC10 that Host is ready to send data. When low, Host is busy.

4.1.1.3 DataOut

Data out signal from the QDC10.
1) Transfers Data to Host on the rising edge of ClockIn. DataOut transitions on falling edge of ClockIn.
2) On the rise of DataOut signal the QDC10 indicates the Host that a data byte is ready to be transferred to the Host (DataIn and ClockIn have to be low).

4.1.2 Data Transfers

Data transfers between Host and QDC10 should be performed by the Host in the highest speed allowed by this data sheet to reduce the message delay between devices. During Data transfer, the QDC10 does not listen to the DC line. If during message transfer to/from Host, the Host does not send clock for more than 65mS between two consecutive bytes, the QDC10 will abort its Data transfer task and return to Receive (search for new message on the DC-BUS).

4.1.2.1 QDC10 to Host data transfer

Byte transfer starts after the QDC10 checks that DataIn is low, then raise its DataOut signal to interrupt the Host. When ready, the Host raises its ClockIn and DataIn signals to indicate the QDC10 to continue the byte transfer. The QDC10 sets its DataOut according to the bit to be sent and waits for the falling of the ClockIn signal to update its DataOut. The Host has to sample the DataOut on the rising edge of the ClockIn. This data transfer continues for 8 bits, then the QDC10 sets its DataOut signal to Low. If the Host is ready to receive another byte, it lowers the DataIn signal.
Notice: 9 clocks are used for a byte transfer from QDC10 to Host

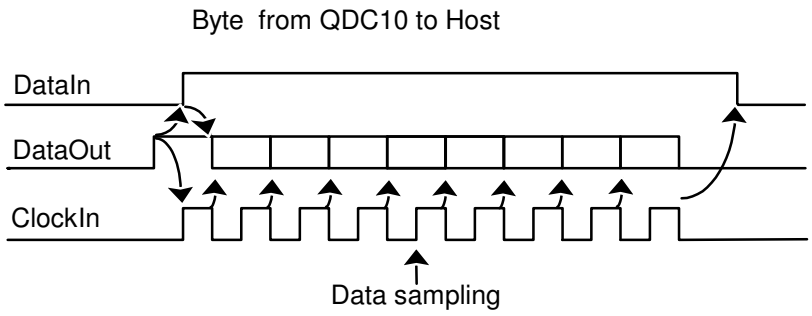


Figure 4.3 - QDC10 to Host byte transfer

4.1.2.2 Host to QDC10 data transfer

Host to QDC10 byte transfer starts when DataIn goes high and ClockIn goes high too (within 100uS). When QDC10 is ready to accept the data, its DataOut signal goes high. The Host sets DataIn signal according to the data bits to be transferred, then ClockIn goes Low. The QDC10 samples the data on the falling edge of ClockIn. Eight bits are transferred this way. After 8 bits transfer, ClockIn goes low. DataIn goes low only when the Host is ready to accept data from QDC10. Otherwise it should be left high. The QDC10 DataOut signal goes low to indicate reception of a byte and ready to receive another byte. If QDC10 does not raise its DataOut in response to the first DataIn rise within 2mS, the Host has to assume that the QDC10 is receiving a message. In this case Host shall wait 3mS for QDC10 response (RxData or RxError) then the Host has to lower the DataIn signal and may try to send its data again later.

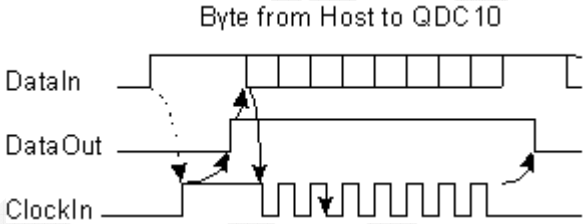


Figure 4.4 - Host to QDC10 byte transfer

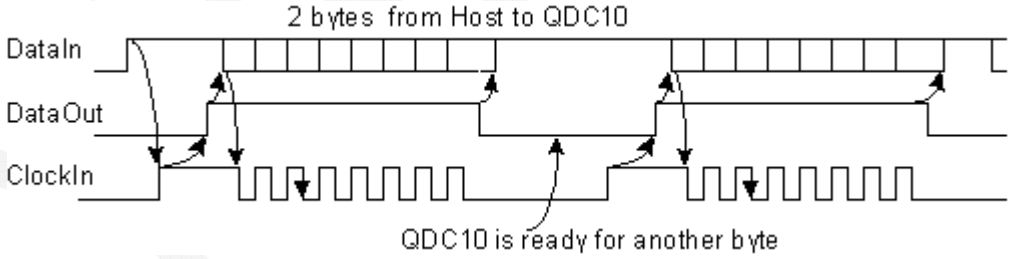
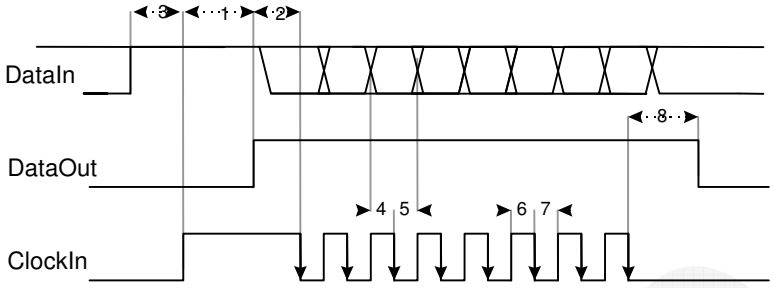


Figure 4.5 - Example for two bytes transfer

4.1.3 Timing Requirements

Byte from Host to QDC10



Byte from QDC10 to Host

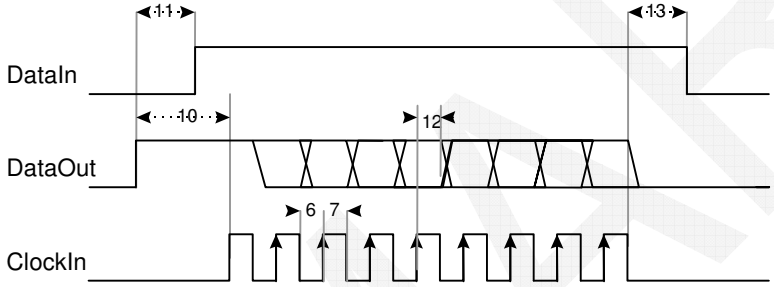


Figure 4.6 - Host interface timing

Table 4.2 - Timing requirements

DataIn			**Min.**	**Max.**
1	TClk2Dout	Time between ClockIn and Host DataOut response		65mS
4	TsuDI	DataIn setup time before ClockIn falling edge	8uS	
5	ThDI	DataIn hold time after ClockIn falling edge	8uS	
ClockIn			**Min.**	**Max.**
6	TwClkH	Clock high time	8uS	
7	TwHostClkL	Clock low time	8uS	
3	TdDIH2ClkH	DataIn High to 1st ClockIn High	0uS	100uS
2	TdDO2CI	DataOut to 1st ClockIn Delay	0uS	65mS
DataOut			**Min.**	**Max.**
10	TdClkDo	DataOut to first ClockIn raise Delay	10uS	65mS
11	TdDoDi	DataOut first raising edge to DataIn stable signal	4uS	65mS
8	TdClkDo	Last ClockIn falling edge to DataOut falling edge	4uS	65mS
12	TpdDo	Delay from ClockIn raising edge to DataOut valid	8uS	

4.2 Oscillator

The QDC10 design requires the use of a 7.130MHz parallel cut crystal. The crystal is connected between OscIn and OscOut pins. Two 22pF capacitors should be connected between these pins and ground. External clock source may be used by driving the OscIn pin.

5 ELECTRICAL PARAMETERS

5.1 Connectivity

Maximal length between extreme devices	12 meters
Minimal length between two devices	0.5 m

5.2 Absolute Maximal Rating

Ambient Temperature under bias	-40°C to 125°C
Storage Temperature	-65°C to 150°C
Voltage on any pin with respect to Vss (except Vdd and ~Reset)	-0.6V to Vdd+0.6V
Voltage on Vdd with respect to Vss	0 to +7.5V
Voltage on ~Reset pin with respect to Vss	0 to +14V
Total power Dissipation	1.0W
Maximum current out of Vss pin	300mA
Maximum current into Vdd pin	250mA
Maximum Output Current sunk by any I/O pin	25mA
Maximum Current sourced by any I/O pin	25mA

5.3 DC Characteristics

Symbol	Characteristics	Min	Typ	Max	Units	Conditions
Vdd	Supply Voltage	4.5		5.5	V	
Idd	Supply Current		9.0		mA	
Ipd	Power Down Current			500	uA	

5.4 Operating Temperature

Commercial: 0°C to 70°C

Industrial: -40°C to 85°C

5.5 Package Type

18 lead plastic small outline (SO) - Wide, 300 mil