HDMI Switch ICs

2 for input 1 output switch with Termination sense correspondence (Sync with HPD_SINK)

BU16006KV

No.09063EDT01

●Description

BU16006KV is 2 input 1 output HDMI/DVI switch LSI. Each Port supports 2.25Gbps. (HDMI 1.3a).
This device control is simple. It requires only 3.3V and a few GPIO controls.
Terminated resistors(50Ω) are integrated at each input port. When channel is not selected, termination resistors are disconnected. TMDS inputs are high impedance.
This device is integrated equalization function and DDC buffer function, so it can adapt long cable.

●Features

1) Supports 2.25 Gbps signaling rate for 480i/p, 720i/p, and 1080i/p resolution to 12-bit color depth
2) Compatible with HDMI 1.3a
3) 5V tolerance to all DDC and HPD_SINK inputs
4) Integrated DDC buffer
5) Integrated switchable 50Ω receiver termination
6) Integrated equalizer circuit to adapt long cable
7) HBM ESD protection exceeds 10kV
8) 3.3V fixed supply to TMDS I/Os
9) 64Pin VQFP package
10) ROHS compatible

●Applications

Digital TV, DVD Player, Set-Top-Box, Audio Video Receiver, Digital Projector, DVI or HDMI Switch Box

●Line up matrix

Part No.	Power Supply (V)	ESD (KV)	Input (ch)	Output (ch)	Data rate (Gbps)	Hot Plug Control	Termination Sense Correspondence	Switching Method	DDC Buffer	Equalizer	De emphasis	Package	RoHS
BU16020KV	3 to 3.6	10	HDMI 4ch	HDMI 1ch	2.7	Yes	Yes	GPIO/I^{2}C	Yes	Yes (adaptive)	Yes	VQFP100	Yes
BU16018KV	3 to 3.6	10	HDMI 3ch	HDMI 1ch	2.25	Yes	Yes	GPIO	Yes	Yes	Yes	VQFP80	Yes
BU16027KV	3 to 3.6	10	HDMI 3ch	HDMI 1ch	2.25	Yes	Yes	GPIO	Yes	Yes	Yes (Always ON)	VQFP64	Yes
BU16006KV	3 to 3.6	10	HDMI 2ch	HDMI 1ch	2.25	Yes	Yes	GPIO	Yes	Yes	Yes (Always ON)	VQFP64	Yes
BU16024KV	3 to 3.6	10	HDMI 1ch	HDMI 1ch	2.25	Yes	Yes	-	Yes	Yes	Yes	VQFP48C	Yes

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●OUTSIDE DIMENSION CHART

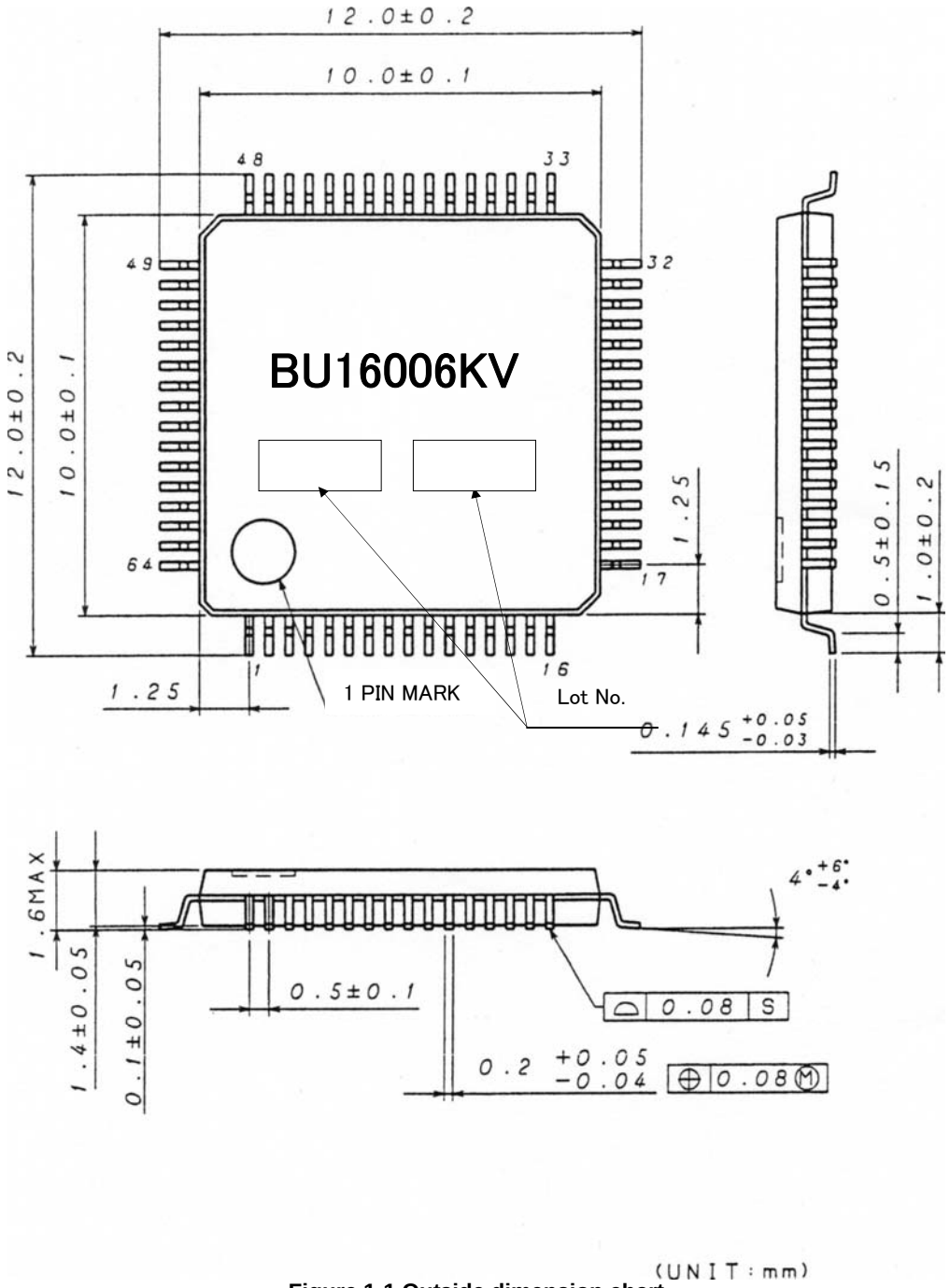

Figure 1-1 Outside dimension chart

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●BLOCK DIAGRAM

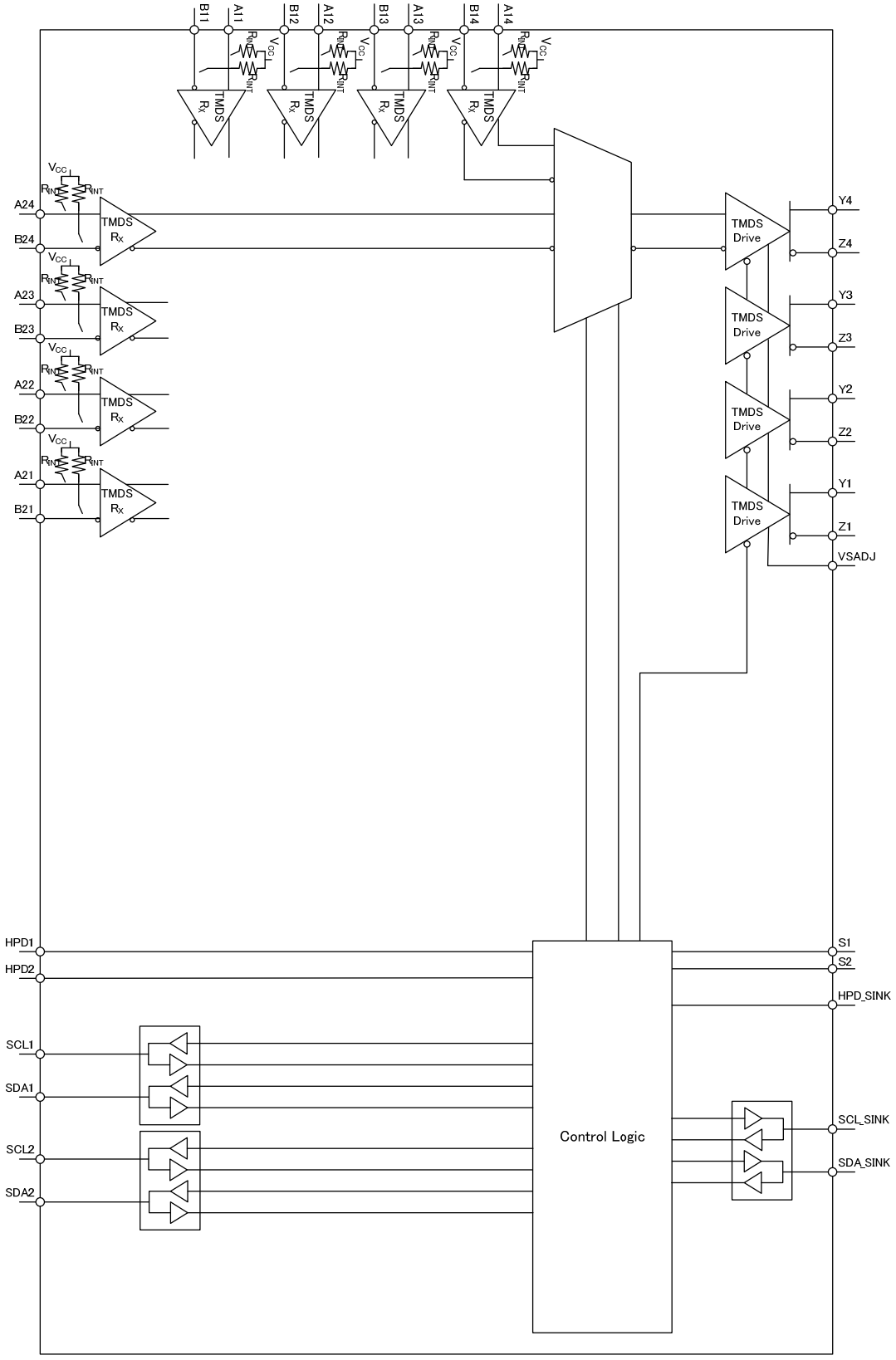

Figure 2-1 Block Diagram

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●PIN EXPLANATION

1). PIN ASSIGNMENT **(TOP VIEW)**

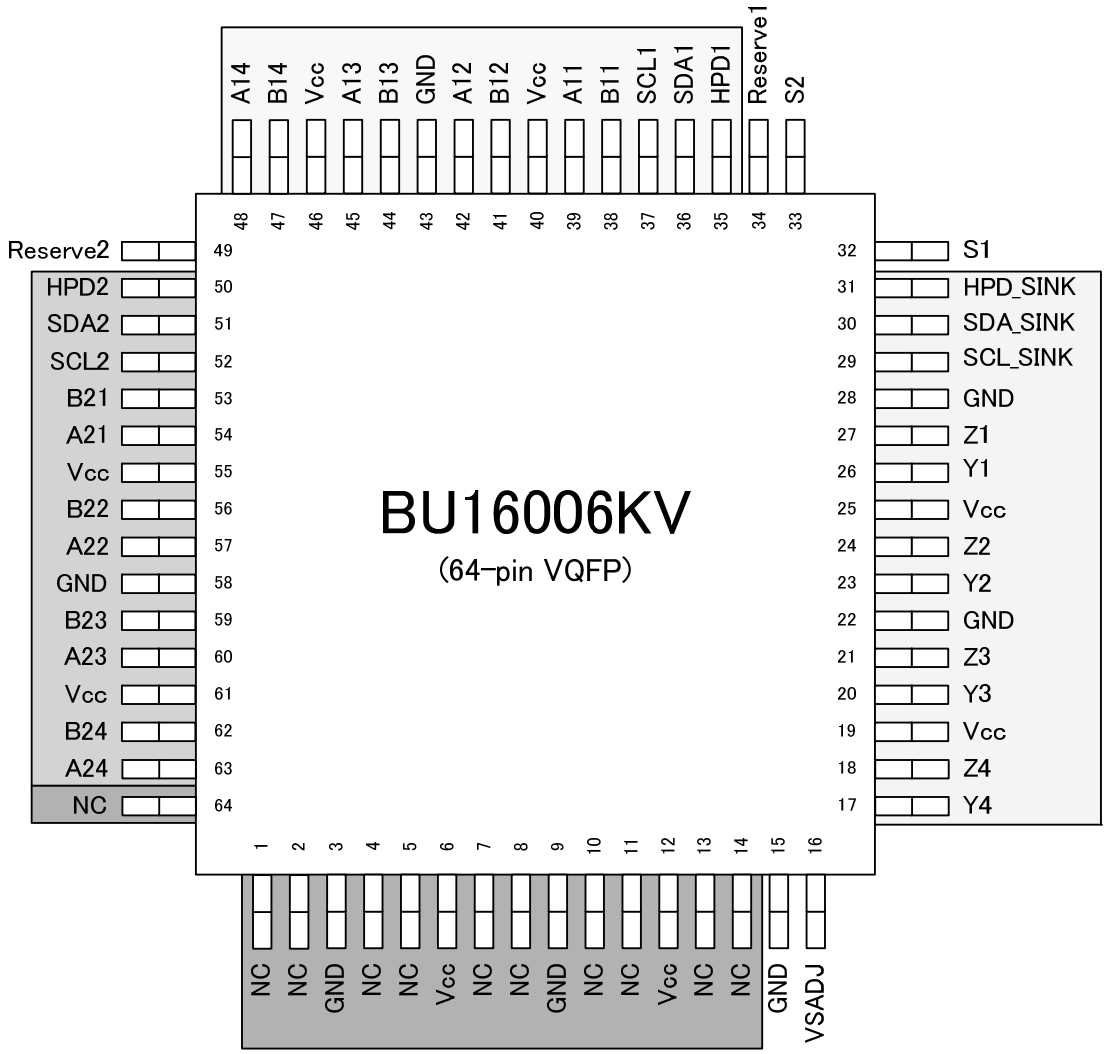

Figure 3-1 Pin Location

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2). PIN LIST

TERMINAL		I/O	DESCRIPTION
NAME	**No.**		
A11, A12, A13, A14	39, 42, 45, 48	I	Source port 1 TMDS positive inputs
A21, A22, A23, A24	54, 57, 60, 63	I	Source port 2 TMDS positive inputs
B11, B12, B13, B14	38, 41, 44, 47	I	Source port 1 TMDS negative inputs
B21, B22, B23, B24	53, 56, 59, 62	I	Source port 2 TMDS negative inputs
GND	3, 9, 15, 22, 28, 43, 58	-	Ground
HPD1	35	O	Source port 1 hot plug detector output (status pin)
HPD2	50	O	Source port 2 hot plug detector output (status pin)
HPD_SINK	31	I	Sink port hot plug detector input (status pin)
Reserve1	34	I/O	Set to HIGH/LOW/OPEN
Reserve2	49	I/O	Non Connect Pin
SCL1	37	I/O	Source port 1 DDC I2C clock line
SCL2	52	I/O	Source port 2 DDC I2C clock line
SCL_SINK	29	I/O	Sink port DDC I2C clock line
SDA1	36	I/O	Source port 1 DDC I2C data line
SDA2	51	I/O	Source port 2 DDC I2C data line
SDA_SINK	30	I/O	Sink port DDC I2C data line
S1, S2	32, 33	I	Source selector
VCC	6, 12, 19, 25, 40, 46, 55, 61	-	Power supply
VSADJ	16	I	TMDS compliant voltage swing control (via 4.64kΩ to GND)
Y1, Y2, Y3, Y4	26, 23, 20, 17	O	Sink port TMDS positive outputs
Z1, Z2, Z3, Z4	27, 24, 21, 18	O	Sink port TMDS negative outputs

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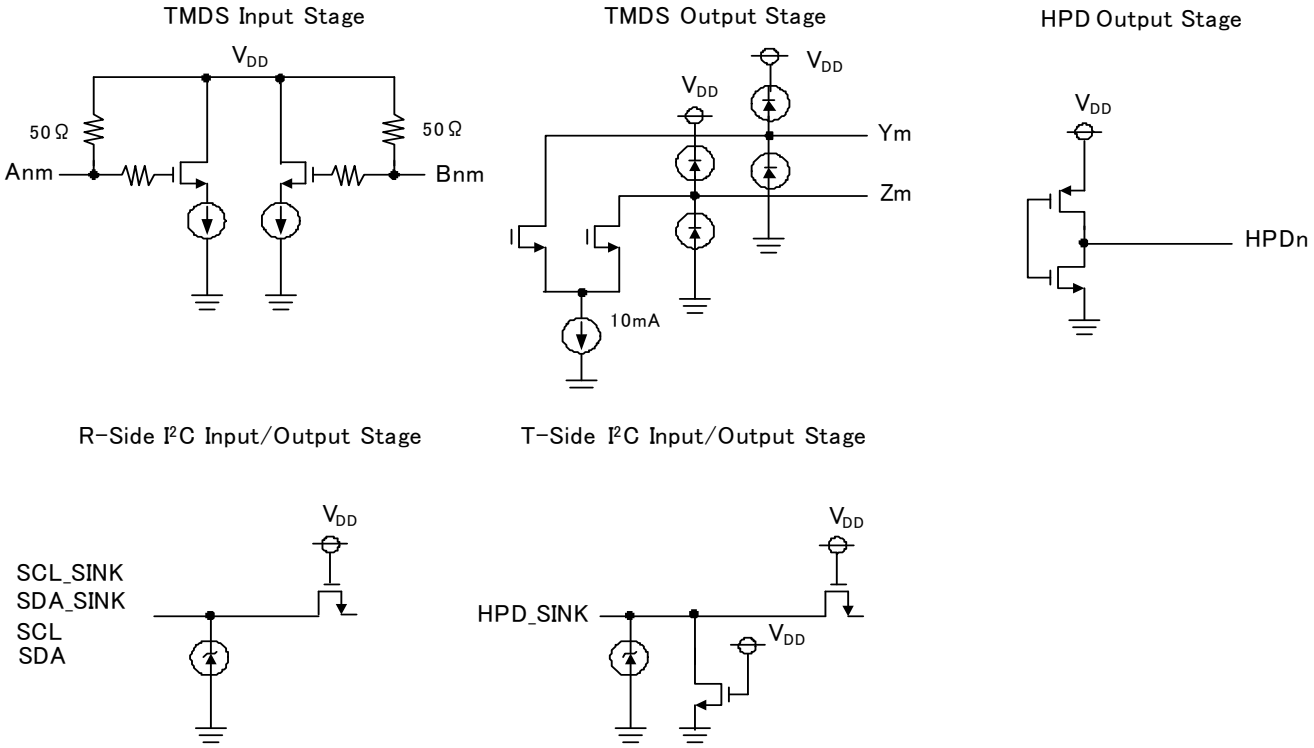
●EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



※n=1,2 m=1,2,3,4

Figure 4-1 I/O pin schematic diagram

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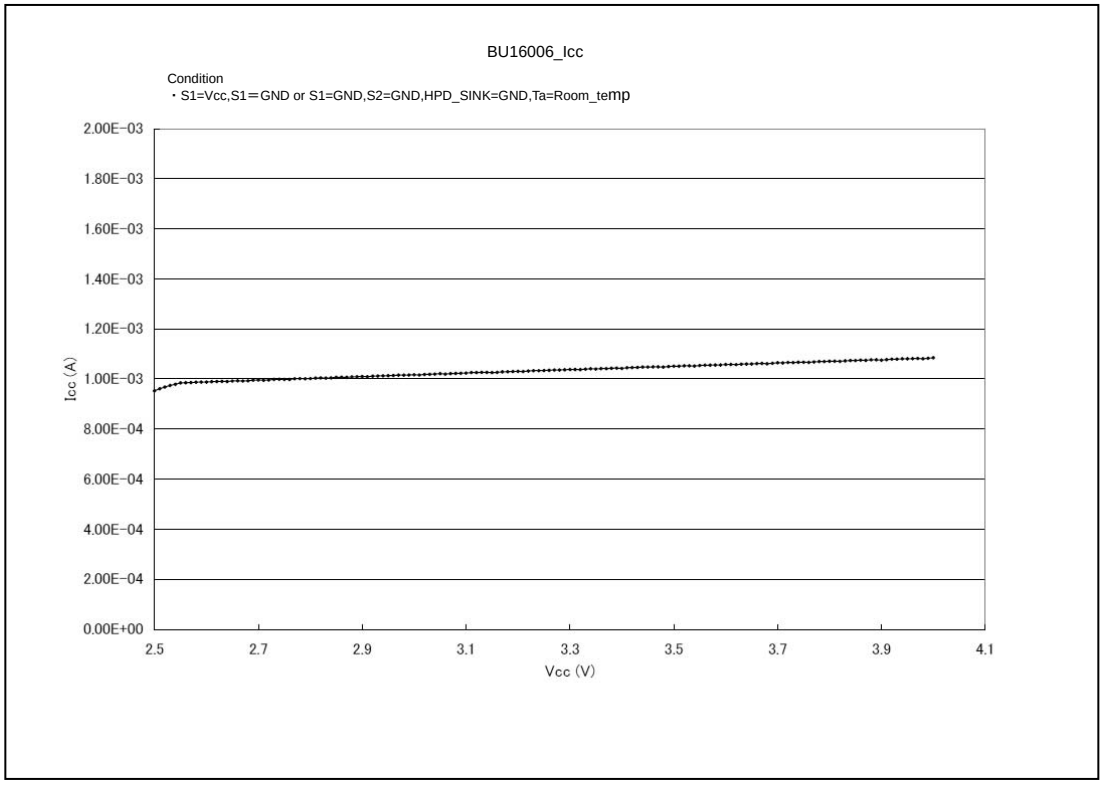
●SOURCE SELECTION LOOKUP TABLE

CONTROL PINS			I/O SELECTED	HOT PLUG DETECT STATUS			
HPD_SINK	**S1**	**S2**	**Y/Z**	**SCL_SINK SDA_SINK**	**HPD1**	**HPD2**	**HPD3**
H	H	H	A1/B1 Terminations of A2/B2 and A3/B3 are disconnected	SCL1 SDA1	H	L	L
H	L	H	A2/B2 Terminations of A1/B1 and A3/B3 are disconnected	SCL2 SDA2	L	H	L
H	L	L	Disallowed (indeterminate)State All terminations are disconnected	None (Z) Are pulled HIGH by external pull-up termination	L	L	H
H	H	L	None (Z) All terminations are disconnected		H	H	H
L	H	H	Disallowed (indeterminate)State All terminations are disconnected	SCL1 SDA1	L	L	L
L	L	H	Disallowed (indeterminate)State All terminations are disconnected	SCL2 SDA2	L	L	L
L	L	L	Disallowed (indeterminate)State All terminations are disconnected	None (Z) Are pulled HIGH by external pull-up termination	L	L	L
L	H	L	None (Z) All terminations are disconnected		L	L	L



(1)H: Logic high; L: Logic low; X: Don't care; Z: High impedance Icc increase about 6mA if HPD_SINK=Vcc.

Figure 4-2 Supply voltage(Vcc) vs. Supply current(Icc) [S1=H,S2=L]

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● **Electrical characteristics**

1.）ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)(1)

ITEM	MIN.	TYP.	MAX.	UNIT
Power supply voltage (Vcc)	-0.3	-	4.0	V
DDC, HPD_SINK input voltage	-0.3	-	6.0	V
Differential input voltage	2.5	-	4.0	V
S1, S2 input voltage	-0.3	-	4.0	V
Power dissipation	-	-	1250※	mW
Strage temperture range	-55	-	125	℃

※70mm×70mm×1.6mm glass epoxy board mount.（Reverse Cu occupation rate：15mm×15mm）

When it's used by than Ta=25℃, it's reduced by 12.5mW/℃.

2.）RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
T_A	Operating free-air temperature	0	-	70	℃
TMDS DIFFERENTIAL PINS					
V_{IC}	Input common mode voltage	V_{CC}–0.6	-	V_{CC}+0.01	V
V_{ID}	Receiver peak-to-peak differential input voltage	150	-	1560	mVp-p
R_{VSADJ}	Resistor for TMDS compliant voltage swing range	4.60	4.64	4.68	kΩ
AV_{CC}	TMDS Output termination voltage, see Figure 5-1.	3	3.3	3.6	V
R_T	Termination resistance, see Figure 5-1.	45	50	55	Ω
	Signaling rate	0	-	2.25	Gbps
CONTROL PINS (S1,S2)					
VIH	LVTTL High-level input voltage	2	-	V_{CC}	V
VIL	LVTTL Low-level input voltage	GND	-	0.8	V
STATUS(HPD_SINK)					
V_{IH}	LVTTL High-level input voltage	2.4	-	5.5	V
V_{IL}	LVTTL Low-level input voltage	GND	-	0.8	V
DDC PINS (SCL_SINK, SDA_SINK,SDA[2:1],SCL[2:1])					
$V_{I(DDC)}$	Input voltage	GND	-	5.5	V

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3.) ELECTRICAL CHARACTERISTICS

Over recommended operating conditions (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.(1)	MAX.	
Icc	Supply current	V_{IH}- = Vcc,V_{IL} = Vcc-0.4V,R_{VSADJ} = 4.64kΩ R_T = 50Ω,AVcc = 3.3V Am/Bm = 2.25 Gbps HDMI data pattern, m = 2,3,4 A1,/B1 = 225 MHz clock	-	120	150	mA
P_D	Power dissipation	V_{IH} = V_{cc},V_{IL} = Vcc-0.4V,R_{VSADJ} = 4.64kΩ R_T = 50Ω,AVcc = 3.3V Am/Bm = 2.25Gbps HDMI data pattern, m = 2,3,4 A1/B1 =255 MH_Z clock	-	450	600	mW
TMDS DIFFERENTIAL PINS (A/B;Y/Z)						
V_{OH}	Single-ended high-level output voltage	See Figure 5-2, AVcc = 3.3V, R_T = 50Ω	Avcc -200	-	Avcc-50	mV
V_{OL}	Single-ended low-level output voltage		Avcc -600	-	Avcc-400	mV
V_{SWING}	Single-ended low-level swing voltage		300	-	460	mV
$Vod_{(O)}$	Overshoot of output differential voltage		-	6%	15%	$2xV_{swing}$
$Vod_{(U)}$	Undershoot of output differential voltage		-	12%	25%	$2xV_{swing}$
$V_{OD(PP)}$	Steady state output differential voltage	See Figure 5-2, Am/Bm = 250 Mbps HDMI data pattern , m = 2,3,4 A1/B1 = 25 MHz clock	600	-	920	mVp-p
R_{INT}	Input termination resistance	V_{IN} = 2.9V	45	50	55	Ω
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		-	5	-	mV

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SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.(1)	MAX.	
DDC Input and output						
Tx						
V_{IH}	High-level input voltage		2.1	-	5.5	V
V_{IL}	Low-level input voltage		-0.3	-	0.35	V
$I_{IKT①}$	Input leak current,	VI=5.5V	-10	-	10	uA
$I_{IKT②}$	Input leak current,	VI=Vcc	-10	-	10	uA
I_{OHT}	High-level output current	VO=3.6V	-10	-	10	uA
I_{ILT}	Low-level input current	VIL=GND	-10	-	10	uA
V_{OLT}	Low-level output voltage	RL=4.7kΩ	0.43	0.5	0.57	V
V_{OLT}-V_{IL}	Low-level input voltage below output low-level voltage		20	100	190	mV
V_{IH}	High_level input voltage		2.4	-	5.5	V
V_{IL}	Low-level input voltage		-0.3	-	0.8	V
$I_{IKR①}$	Input leak current	VI=5.5V	-10	-	10	uA
$I_{IKR②}$	Input leak current	VI=Vcc	-10	-	10	uA
I_{OHR}	High-level output current	VO=3.6V	-10	-	10	uA
I_{ILR}	Low-level input current	VIL=GND	-10	-	10	uA
V_{OLR}	Low-level output voltage	Iout = 4mA	-	-	0.2	V
STATUS PINS (HPD 1, HPD 2,)						
$V_{OH(TTL)}$	TTL High –level output voltage	I_{OH} = -8mA	2.4	-	Vcc	V
$V_{OL(TTL)}$	TTL Low –level output voltage	I_{OL} = 8mA	0	-	0.4	V
CONTROL PINS (S1, S2)						
I_{IH}	High –level digital input current	V_{IH} = Vcc	-10	-	10	uA
I_{IL}	Low –level digital input current	V_{IL} = GND	-10	-	10	uA
STATUS PINS (HPD_SINK)						
I_{IH}	High –level digital input current	V_{IH} = 5.5V	10	50	100	uA
		V_{IH} = Vcc	5	30	80	uA
I_{IL}	Low –level digital input current	V_{IL} = GND	-10	-	10	uA

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SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.(1)	MAX.	
TMDS DIFFERENTIAL PINS (Y/Z)						
t_{PLH}	Propagation delay time low-high-level output	See Figure 5-2, AV_{CC} = 3.3V, R_T = 50Ω	-	480	-	ps
t_{PHL}	Propagation delay time low-high-level output		-	500	-	ps
t_r	Differential output signal rise time (20%-80%)		-	150	-	ps
t_f	Differential output signal fall time (20%-80%)		-	150	-	ps
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)		-	20	-	ps
$t_{sk(D)}$	Intra-pair differential skew, see Figure 5-3.		-	50	-	ps
$t_{sk(o)}$	Inter-pair channel-to-channel output skew(2)		-	50	-	ps
$t_{sk(pp)}$	Part to part skew(3)		-	400	-	ps
DDC I/O PINS (SCL, SCL_SINK, SDA, SDA_SINK)						
$t_{pdLHTR(DDC)}$	Propagation delay time, low-to-high-level output Tx to Rx	R_L = 4.7KΩ, C_L = 100pF	-	650	-	ns
$t_{pdHLTR(DDC)}$	Propagation delay time, high-to-low-level output Tx to Rx		-	200	-	ns
$t_{pdLHRT(DDC)}$	Propagation delay time, low-to-high-level output Rx to Tx	R_L = 1.67KΩ, C_L = 400pF	-	500	-	ns
$t_{pdHLRT(DDC)}$	Propagation delay time, high-to-low-level output Rx to Tx		-	350	-	ns
tr $Tx_{(DDC)}$	Tx output Rise time	R_L = 4.7KΩ, C_L = 100pF	-	800	-	ns
tf $Tx_{(DDC)}$	Tx output Fall time		-	150	-	ns
tr $Rx_{(DDC)}$	Rx output Rise time	R_L = 1.67KΩ, C_L = 400pF	-	950	-	ns
tf $Rx_{(DDC)}$	Rx output Fall time		-	50	-	ns
t_{sx}	Select to switch output		-	8	-	ns
t_{dis}	Disable time		-	5	-	ns
t_{en}	Enable time		-	7	-	ns
$t_{sx(DDC)}$	Switch time from SCLn to SCL_SINK	C_L=10pF	-	800	-	ns
C_{IO}	Input/output capacitance	V_I=0V		15		pF
STATUS PINS(HPD1,HPD2,HPD3)						
$t_{pdLH(HPD)}$	Propagation delay time, low-to-high-level output from HPD_SINK to HPDn(n=1,2)	C_L=10pF	-	5	-	ns
$t_{pdHL(HPD)}$	Propagation delay time, high-to-low-level output from HPD_SINK to HPDn(n=1,2)	C_L=10pF	-	5	-	ns
$t_{sx(HPD)}$	Switch time from port select to the latest valid status of HPD	C_L=10pF	-	8	-	ns

Note:

1. All typical values are at 25℃ and with a 3.3V supply.
2. $t_{sk(o)}$ is the magnitude of the difference in propagation delay times between any specified terminals of channel of a devices when inputs are tied together.
3. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of channel of two devices, or between channel 1 of two devices, when both devices operate with the same source, the same supply voltages, at the same temperature, and have identical packages and test circuits.

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●MEASUREMENT SYMBOL AND CIRCUIT

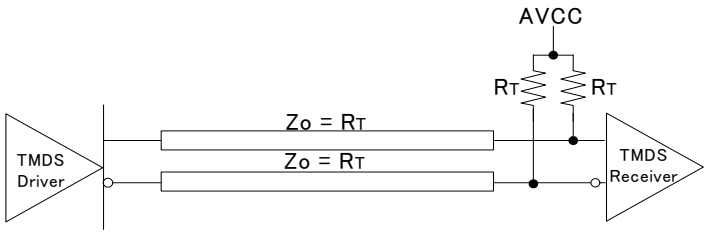
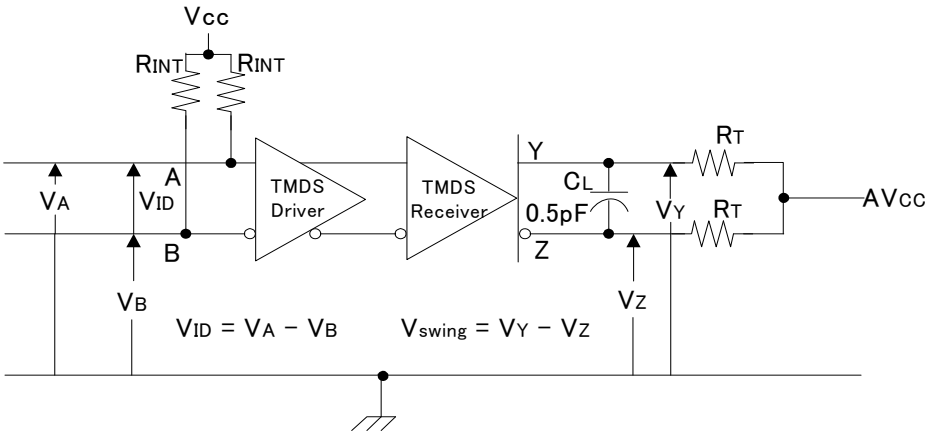


Figure 5-1 Termination for TMDS Output Driver



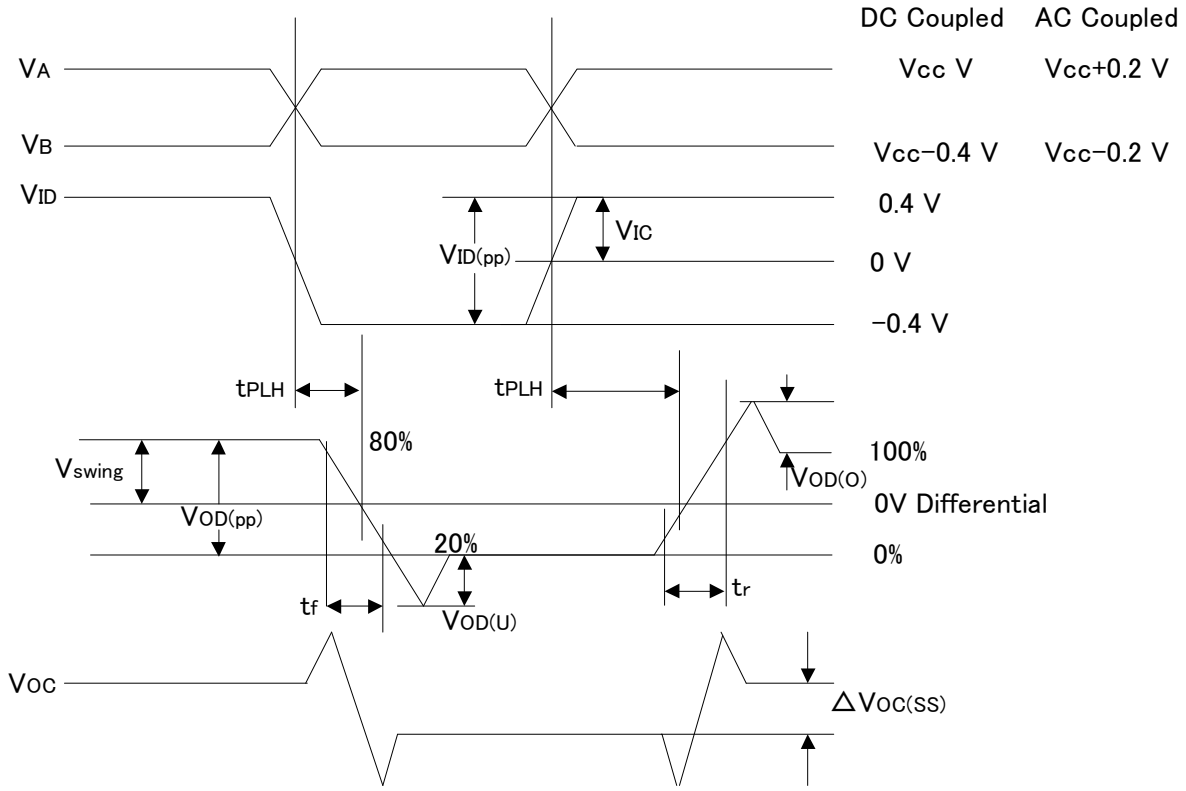


Figure 5-2. Timing Test Circuit and Definitions

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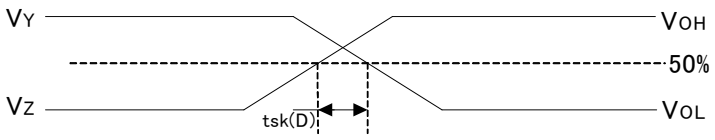

Figure 5-3 Definition of Intra-Pair Differential Skew

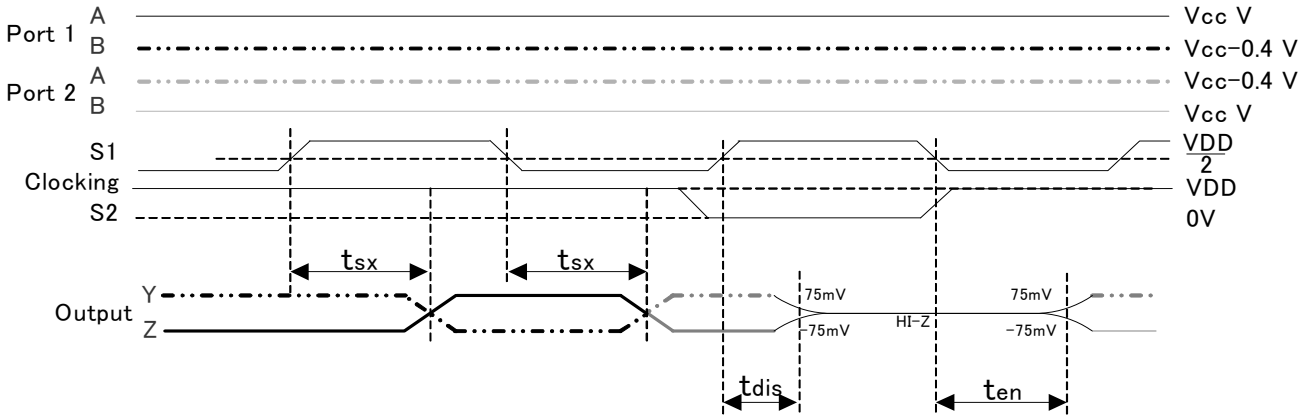

Figure 5-4 TMDS Outputs Control Timing Definitions

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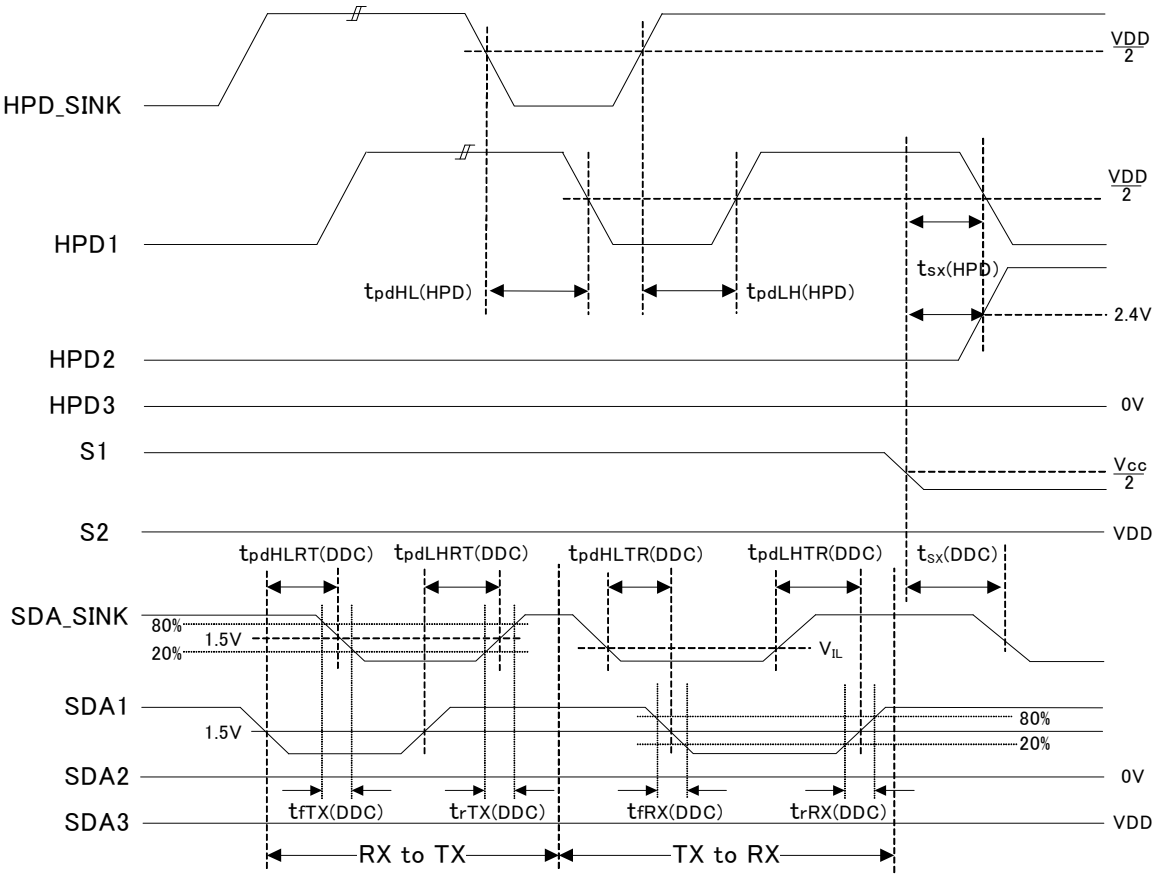

Figure 5-5 DDC and HPD Timing Definitions

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1). HPD_SINK Pull down resistance.

HPD_SINK is a 5V tolerant structure shown in Figure 6-1.
It needs some drive current to pull down HPD_SINK "H" to "L"(max10uA@HPD_SINK=2V).
So to pull down HPD_SINK, please use 10kΩ(or under 10kΩ) resistor.

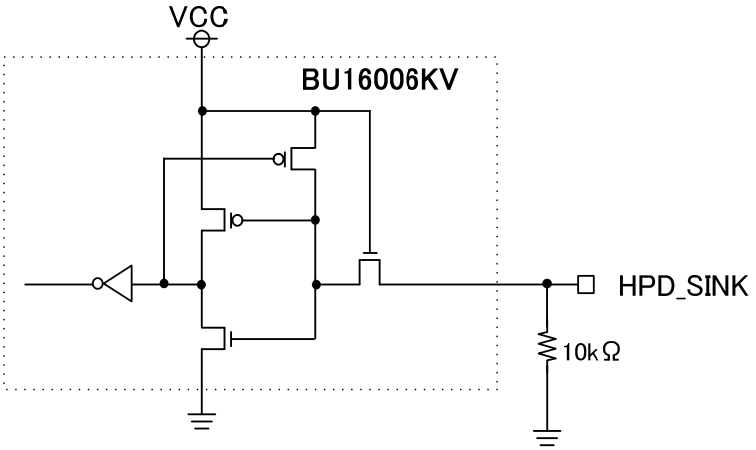

Figure 6-1 HPD SINK I/O schematic

2). About don't use terminal.
Unused TMDS input channel can be opened.

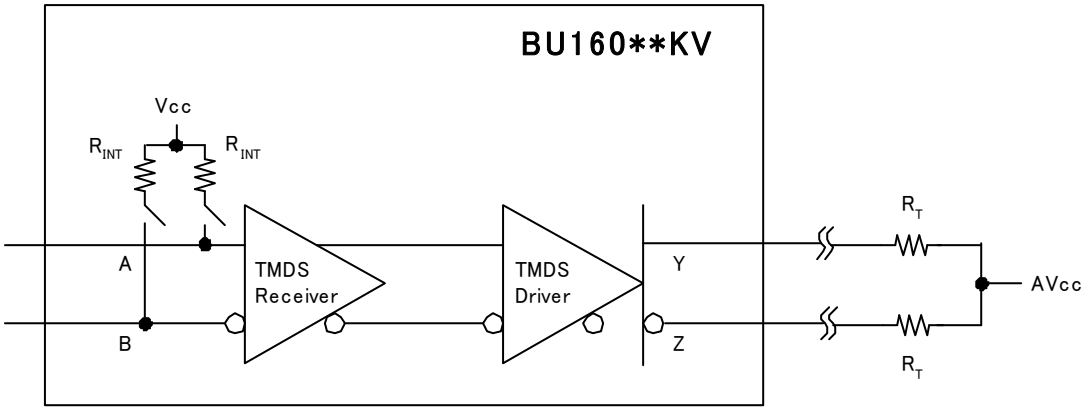

Figure 6-2 TMDS Input Fail-Safe Recommendation

Unused DDC Buffers of R side polled up to Vcc.

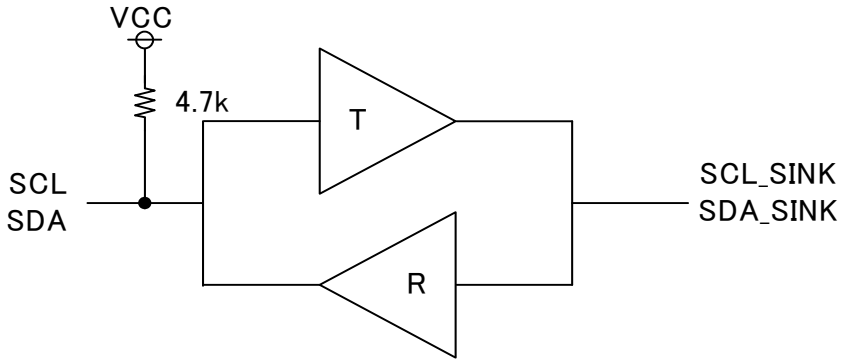

Figure 6-3 DDC Buffers in BU160KV**

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Open unused HPDn.

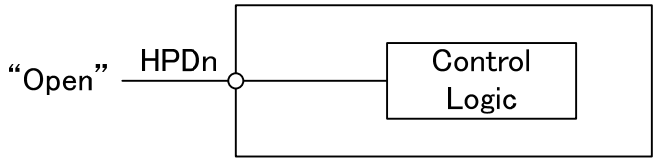

Figure 6-4 Open unused HPDn

3). About serial connect notice.
When HDMI sw output connect to other HDMI sw input like following application.
There is possibility that. 1080p(12bit) image isn't displayed. It's depend on receiver IC characteristic.
When system is required 1080p (12bit), Rohm doesn't recommend serial connect application.

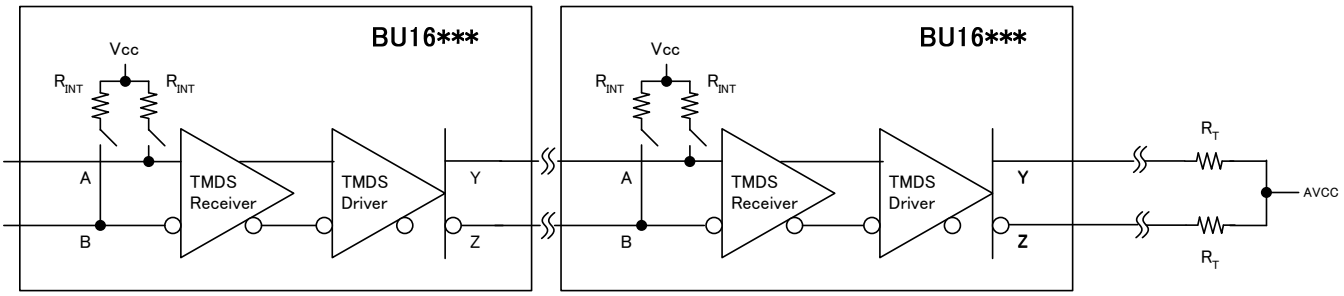

Figure 6-5 serial connect notice

4). Offset voltage appearance.
If differential input is opened, offset voltage appear at differential output OE is set to low to avoid it.

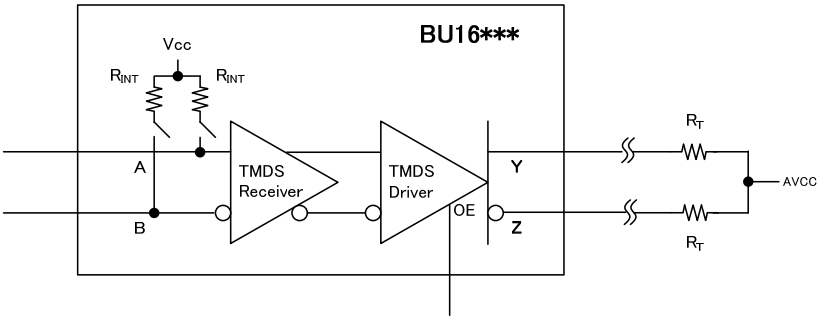

Figure 6-6 Offset voltage avoid

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5). Limitation of Master and slave direction.

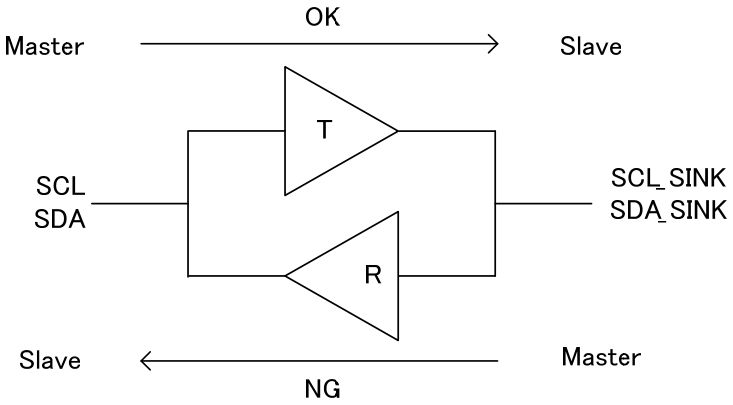

Figure 6-7 Limitation of Master and slave direction

6). Attention in use as repeater.

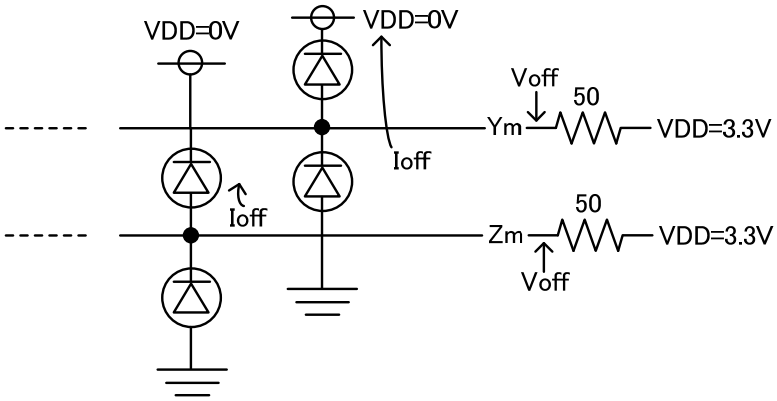

Figure 6-8 Ioff specification not meet to HDMI CTS

Depend on HDMI CTS, Voff must be less than VDD-10mV, but this IC not meet to CTS cause of Ioff.

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● **Ordering part number**

B	U	1	6	0	0	6		K	V	—	E	2

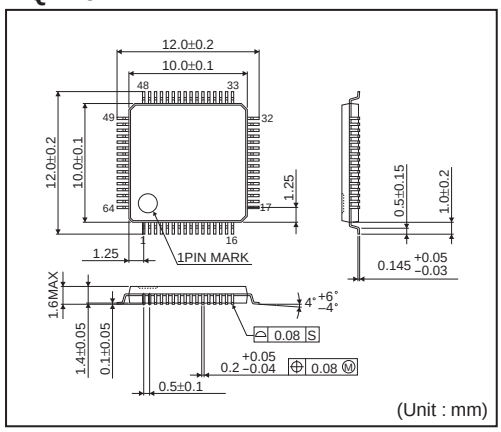
ROHM model name

Package type
VQFP64

Packaging and forming specification
E2 =Reel-shaped emboss taping

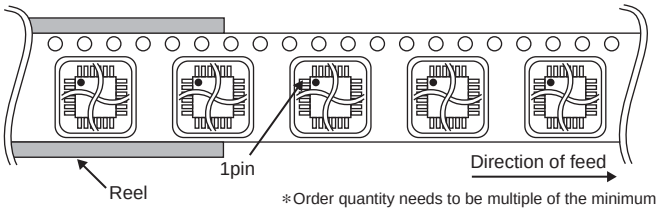
●Package specification

VQFP64



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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