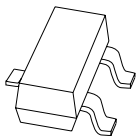


PESDxL2BT series

Low capacitance double bidirectional ESD protection diodes in SOT23

Rev. 02 — 25 August 2009 Product data sheet

1. Product profile

1.1 General description

Low capacitance double bidirectional ElectroStatic Discharge (ESD) protection diodes in a SOT23 small Surface Mounted Device (SMD) plastic package designed to protect two signal lines from the damage caused by ESD and other transients.

1.2 Features

- ESD protection of two lines
- Max. peak pulse power: P_{PP} = 350 W
- Low clamping voltage: V_{CL} = 26 V
- Small SMD plastic package
- Ultra low leakage current: I_{RM} < 90 nA
- ESD protection up to 23 kV
- IEC 61000-4-2, level 4 (ESD)
- IEC 61000-4-5 (surge); I_{PP} = 15 A

1.3 Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- Communication systems
- Portable electronics
- Subscriber Identity Module (SIM) card protection

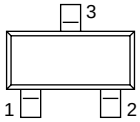
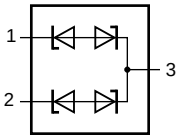
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage					
	PESD3V3L2BT		-	-	3.3	V
	PESD5V0L2BT		-	-	5.0	V
	PESD12VL2BT		-	-	12	V
	PESD15VL2BT		-	-	15	V
	PESD24VL2BT		-	-	24	V
C_d	diode capacitance	V_R = 0 V; f = 1 MHz				
	PESD3V3L2BT		-	101	-	pF
	PESD5V0L2BT		-	75	-	pF
	PESD12VL2BT		-	19	-	pF
	PESD15VL2BT		-	16	-	pF
	PESD24VL2BT		-	11	-	pF

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Symbol
1	cathode 1		
2	cathode 2		
3	double cathode		

006aaa155

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD3V3L2BT	-	plastic surface mounted package; 3 leads	SOT23
PESD5V0L2BT			
PESD12VL2BT			
PESD15VL2BT			
PESD24VL2BT			

4. Marking

Table 4. Marking codes

Type number	Marking code[1]
PESD3V3L2BT	V3*
PESD5V0L2BT	V4*
PESD12VL2BT	V5*
PESD15VL2BT	V6*
PESD24VL2BT	V7*

[1] * = -: made in Hong Kong
* = p: made in Hong Kong
* = t: made in Malaysia
* = W: made in China

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{PP}	peak pulse power	t_p = 8/20 µs	[1][2]			
	PESD3V3L2BT			-	350	W
	PESD5V0L2BT			-	350	W
	PESD12VL2BT			-	200	W
	PESD15VL2BT			-	200	W
	PESD24VL2BT			-	200	W
I_{PP}	peak pulse current	t_p = 8/20 µs	[1][2]			
	PESD3V3L2BT			-	15	A
	PESD5V0L2BT			-	13	A
	PESD12VL2BT			-	5	A
	PESD15VL2BT			-	5	A
	PESD24VL2BT			-	3	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			–65	+150	°C
T_{stg}	storage temperature			–65	+150	°C

[1] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC 61000-4-5.

[2] Measured from pin 1 to 3 or 2 to 3.

Table 6. ESD maximum ratings

Symbol	Parameter	Conditions		Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[1][2]			
	PESD3V3L2BT			-	30	kV
	PESD5V0L2BT					
	PESD12VL2BT					
	PESD15VL2BT					
	PESD24VL2BT			-	23	kV
	PESDxL2BT series	HBM MIL-STD883		-	10	kV

[1] Device stressed with ten non-repetitive ESD pulses.

[2] Measured from pin 1 to 3 or 2 to 3.

Table 7. ESD standards compliance

ESD Standard	Conditions
IEC 61000-4-2, level 4 (ESD)	> 15 kV (air); > 8 kV (contact)
HBM MIL-STD883, class 3	> 4 kV

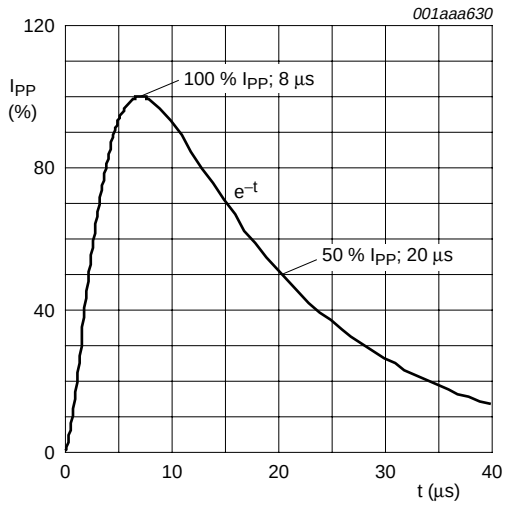


Fig 1. 8/20 µs pulse waveform according to IEC 61000-4-5

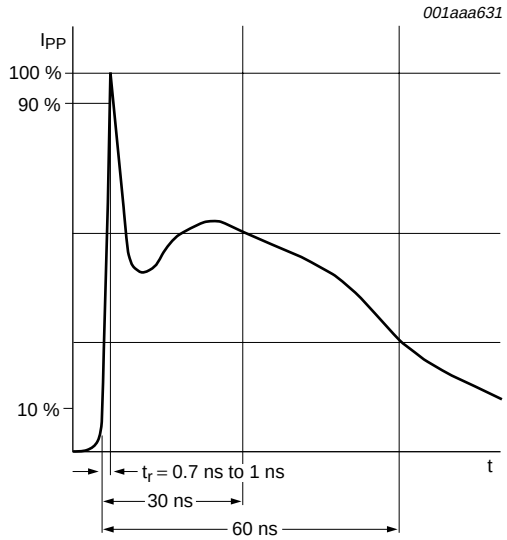


Fig 2. ESD pulse waveform according to IEC 61000-4-2

6. Characteristics

Table 8. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage					
	PESD3V3L2BT		-	-	3.3	V
	PESD5V0L2BT		-	-	5.0	V
	PESD12VL2BT		-	-	12	V
	PESD15VL2BT		-	-	15	V
	PESD24VL2BT		-	-	24	V
I_{RM}	reverse leakage current					
	PESD3V3L2BT	V_{RWM} = 3.3 V	-	0.09	2	µA
	PESD5V0L2BT	V_{RWM} = 5.0 V	-	0.01	1	µA
	PESD12VL2BT	V_{RWM} = 12 V	-	< 1	50	nA
	PESD15VL2BT	V_{RWM} = 15 V	-	< 1	50	nA
	PESD24VL2BT	V_{RWM} = 24 V	-	< 1	50	nA
V_{BR}	breakdown voltage	I_R = 5 mA				
	PESD3V3L2BT		5.8	6.4	6.9	V
	PESD5V0L2BT		7.0	7.6	8.2	V
	PESD12VL2BT		14.2	15.8	16.7	V
	PESD15VL2BT		17.1	18.8	20.3	V
	PESD24VL2BT		25.4	27.8	30.3	V
C_d	diode capacitance	V_R = 0 V; f = 1 MHz				
	PESD3V3L2BT		-	101	-	pF
	PESD5V0L2BT		-	75	-	pF
	PESD12VL2BT		-	19	-	pF
	PESD15VL2BT		-	16	-	pF
	PESD24VL2BT		-	11	-	pF
V_{CL}	clamping voltage	[1][2]				
	PESD3V3L2BT	I_{PP} = 1 A	-	-	8	V
		I_{PP} = 15 A	-	-	26	V
	PESD5V0L2BT	I_{PP} = 1 A	-	-	10	V
		I_{PP} = 13 A	-	-	28	V
	PESD12VL2BT	I_{PP} = 1 A	-	-	20	V
		I_{PP} = 5 A	-	-	37	V
	PESD15VL2BT	I_{PP} = 1 A	-	-	25	V
		I_{PP} = 5 A	-	-	44	V
	PESD24VL2BT	I_{PP} = 1 A	-	-	40	V
		I_{PP} = 3 A	-	-	70	V

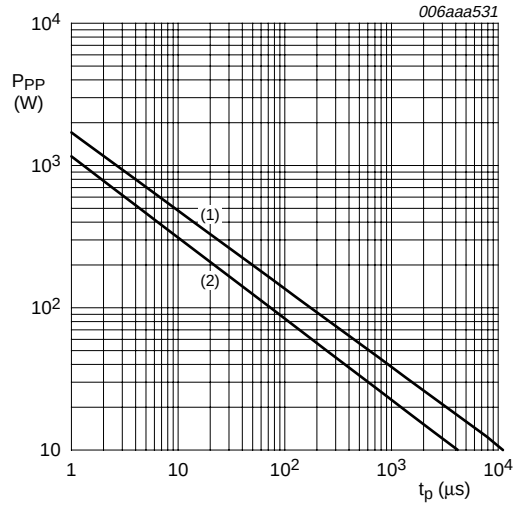
Table 8. Characteristics *...continued*

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
r_{dif}	differential resistance	I_R = 1 mA				
	PESD3V3L2BT		-	-	400	Ω
	PESD5V0L2BT		-	-	80	Ω
	PESD12VL2BT		-	-	200	Ω
	PESD15VL2BT		-	-	225	Ω
	PESD24VL2BT		-	-	300	Ω

[1] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[2] Measured from pin 1 to 3 or 2 to 3.



T_{amb} = 25 °C

(1) PESD3V3L2BT and PESD5V0L2BT

(2) PESD12VL2BT, PESD15VL2BT, PESD24VL2BT

Fig 3. Peak pulse power as a function of exponential pulse duration t_p; typical values

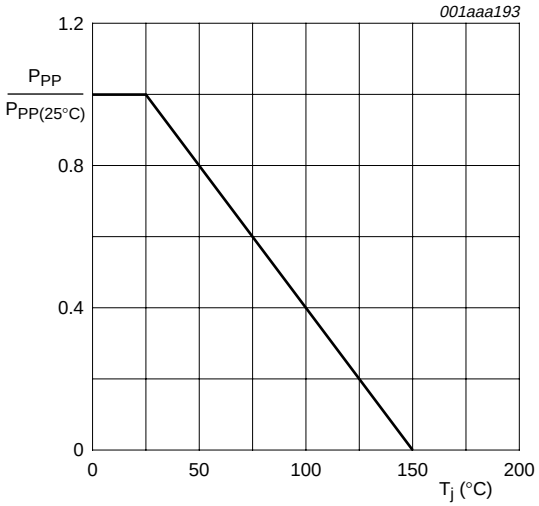
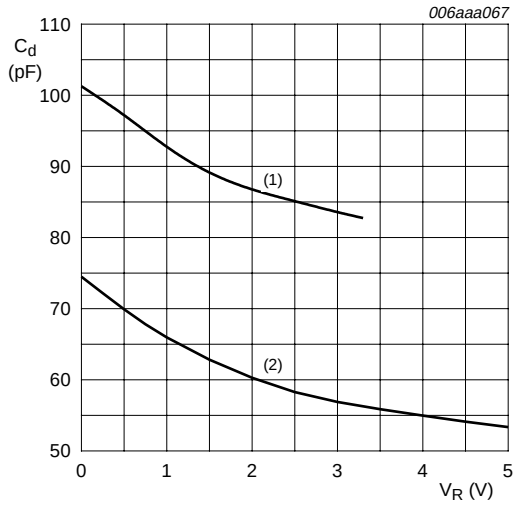


Fig 4. Relative variation of peak pulse power as a function of junction temperature; typical values

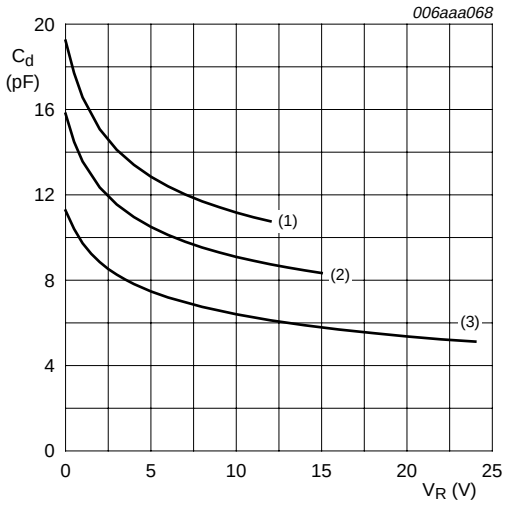


T_{amb} = 25 °C; f = 1 MHz

(1) PESD3V3L2BT

(2) PESD5V0L2BT

Fig 5. Diode capacitance as a function of reverse voltage; typical values



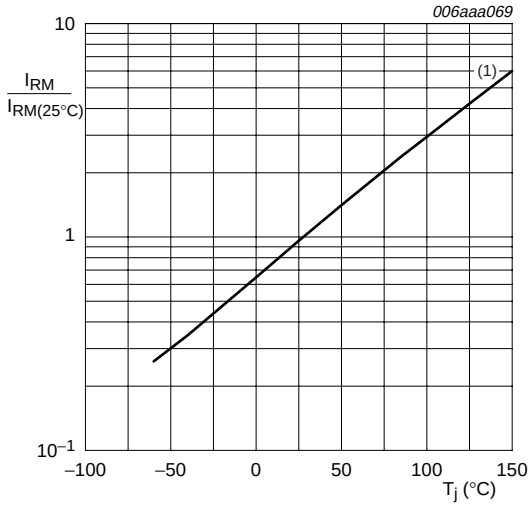
T_{amb} = 25 °C; f = 1 MHz

(1) PESD12VL2BT

(2) PESD15VL2BT

(3) PESD24VL2BT

Fig 6. Diode capacitance as a function of reverse voltage; typical values



(1) PESD3V3L2BT, PESD5V0L2BT

PESD12VL2BT, PESD15VL2BT and PESD24VL2BT: I_{RM} < 20 nA; T_j = 150 °C

Fig 7. Relative variation of reverse leakage current as a function of junction temperature; typical values

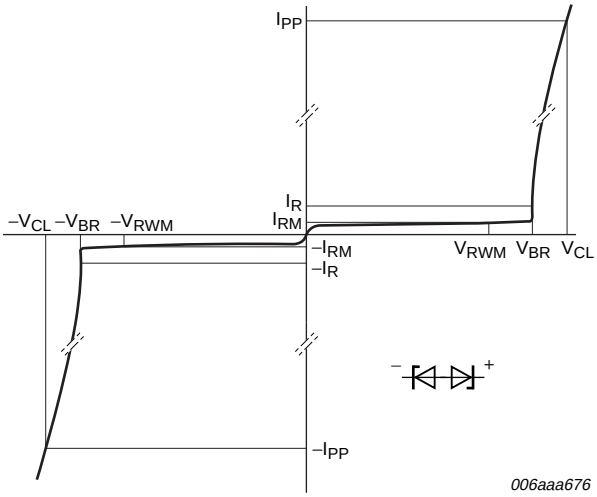


Fig 8. V-I characteristics for a bidirectional ESD protection diode

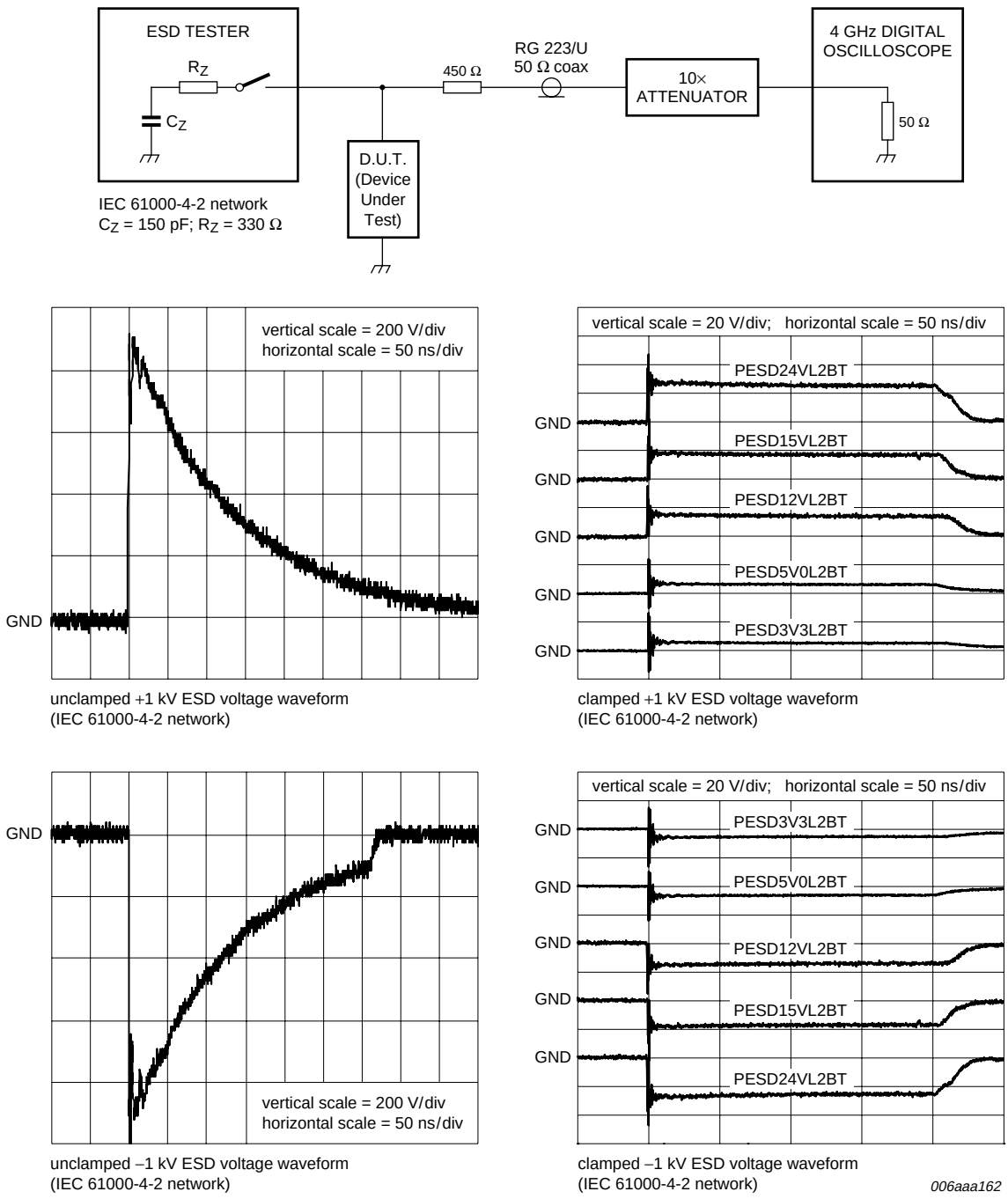


Fig 9. ESD clamping test setup and waveforms

7. Application information

The PESDxL2BT series is designed for the protection of two bidirectional signal lines from the damage caused by ESD and surge pulses. The PESDxL2BT series may be used on lines where the signal polarities are above and below ground. The PESDxL2BT series provides a surge capability of up to 350 W per line for an 8/20 μs waveform.

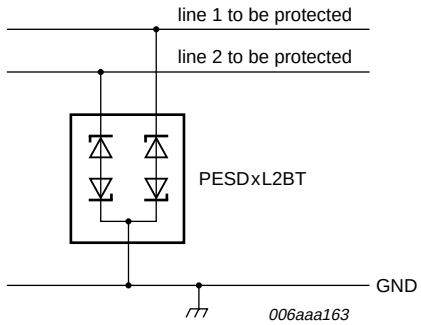


Fig 10. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the PESDxL2BT as close to the input terminal or connector as possible.
2. The path length between the PESDxL2BT and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

8. Package outline

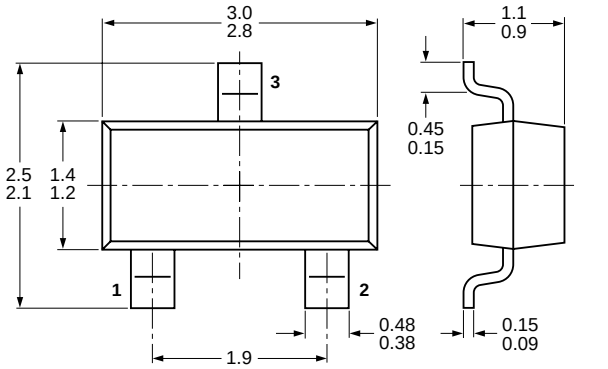


Fig 11. Package outline SOT23 (TO-236AB)

9. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packing quantity	
			3000	10000
PESD3V3L2BT	SOT23	4 mm pitch, 8 mm tape and reel	-215	-235
PESD5V0L2BT				
PESD12VL2BT				
PESD15VL2BT				
PESD24VL2BT				

[1] For further information and the availability of packing methods, see Section 12.

10. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PESDXL2BT_SER_2	20090825	Product data sheet	-	PESDXL2BT_SER_1
Modifications:	• This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content. • Table 2 “Pinning”: amended			
PESDXL2BT_SER_1	20051101	Product data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

11.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

11.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

11.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

12. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

13. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 25 August 2009

Document identifier: PESDXL2BT_SER_2