

- *TTL Compatible (3.3v)*
- *2 Packaging Styles*
- *Ultra Low Jitter*
- *Low Phase Noise*
- *Immediate Delivery*

**Part Numbering Example: CAM C 7 L Z - A5 B6 - XXX.XXXX TS**

CAM	C	7	L	Z	A5	B6	XXX.XXXX	TS
SERIES	OUTPUT	PACKAGE STYLE	VOLTAGE	PACKAGING OPTIONS	OPERATING TEMP.	STABILITY	FREQUENCY	TRI-STATE
CAM	C=HCMOS	1 = Full Size 4 = Half Size 5 = 5 X 3.2 Ceramic 7 = 5 X 7 Ceramic	L = 3.3 V S = 2.5 V	Blank = Bulk T = Tube Z = Tape and Reel	Blank = 0°C +70°C A5 = -20°C +70°C A7 = -40°C +85°C	B6 = ±100 ppm BP = ±50 ppm BR = ±25 ppm	1.000-200.000 MHz	TS = Tri-State

**Specifications:**

Description	Min	Typ	Max	Unit
<b>Frequency Range:</b> Programmable to Any Discrete Frequency	1.000		200.000	MHz
<b>Available Stability Options:</b>	-100 -50 -25		100 50 25	ppm ppm ppm
<b>Supply Voltage Options:</b> (1-133 MHz) (1-200 MHz)	2.25 3.0	2.5 3.3	2.75 3.6	V V
<b>Operating Temperature Range Options:</b>	0 -20 -40		+70 +70 +85	°C °C °C
<b>Storage Temperature:</b>	-55		+125	°C
Aging (PPM/Year) Ta=25C, Vdd=3.3V/2.5V			±5	
<b>Output Level:</b>	HCMOS			
<b>Packaging:</b>	Tape and Reel (1K per Reel) Tube			

**Operating Conditions:**

Description	Min	Max	Unit
Vdd Supply Voltage	2.25	3.6	V
Vdd Rise Time	100		µS
HCMOS Max Capacitive Load on outputs for CMOS levels Frequency: < 40 MHz Frequency: 40-200 MHz		30 15	pF pF



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Electrical Characteristics

Description	TEST CONDITIONS	Min	Typ	Max	Unit
<b>Input Characteristics (Pin 1):</b> V <sub>IL</sub> , Low-Level Input Voltage TO DISABLE OUTPUT	3.0–3.6V V <sub>dd</sub>			0.2V <sub>dd</sub>	V
V <sub>IH</sub> , High-Level Input Voltage TO ENABLE OUTPUT OR NO CONNECT	3.0–3.6V V <sub>dd</sub>	0.7V <sub>dd</sub>			V
I <sub>IL</sub> , Input Low Current I <sub>IH</sub> , Input High Current	V <sub>IN</sub> = 0V V <sub>IN</sub> = V <sub>dd</sub>			80 10	μA μA
<b>Output Characteristics:</b> V <sub>OL</sub> , Low-Level Output Voltage	3.0V–3.6V V <sub>dd</sub> , 8 mA I <sub>OL</sub>			0.4	V
V <sub>OHC</sub> MOS, High-level HCMOS Voltage	2.25V–3.6V V <sub>dd</sub> , -8 mA I <sub>OL</sub>	V <sub>dd</sub> -0.4			V V
<b>Power Supply Current:</b> (unloaded)	2.25–3.6 V <sub>dd</sub> , OUTPUT FREQ ≤ 200 MHz			35	mA
<b>Input Pull-Up Resistor:</b>	2.25–3.6V V <sub>dd</sub> , V <sub>IN</sub> = 0.7V	50	70	90	KΩ
<b>Tri-State Leakage Current:</b>	3.6V V <sub>dd</sub>		20		μA
<b>Output Enable Mode:</b>	Output is Tri-Stated				

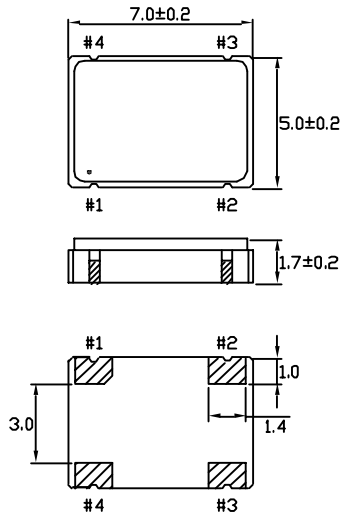
Output Clock Switching Characteristics

Description	TEST CONDITIONS	Min	Typ	Max	Unit
<b>Duty Cycle:</b> HCMOS @ V <sub>dd</sub> /2	2.25 V – 3.6V V <sub>dd</sub>	45		55	%
<b>Output Clock Rise/Fall:</b>	0.2–0.8V <sub>dd</sub> , 2.25–3.6 V <sub>dd</sub> , C <sub>L</sub> = 30 0.2–0.8V <sub>dd</sub> , 2.25–3.6 V <sub>dd</sub> , C <sub>L</sub> = 15			4.0 2.4	nS nS
<b>Start Up Time:</b>	From power on		3	10	mS
<b>RMS Period Jitter:</b>			10		pS
<b>RMS Integrated Jitter:</b>	12kHz to 20MHz		15		pS
<b>Phase Noise:</b>	@ 10kHz			-100	dBc/Hz



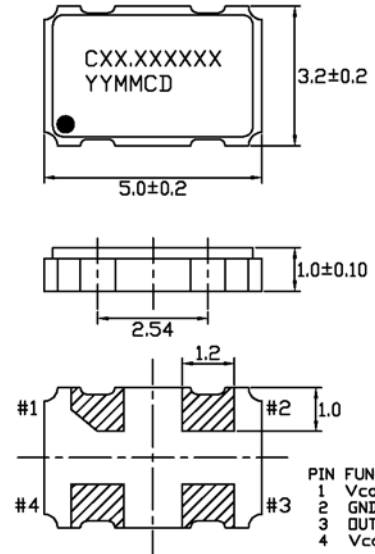
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**Style 7 5x7 Ceramic SMD**



**PIN FUNCTION**  
 1 CONTROL  
 2 GND  
 3 OUTPUT  
 4 Vdd

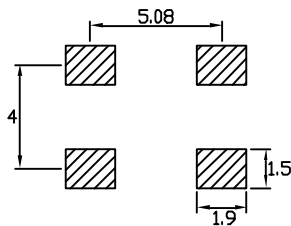
**Style 5 5x3.2 Ceramic SMD**



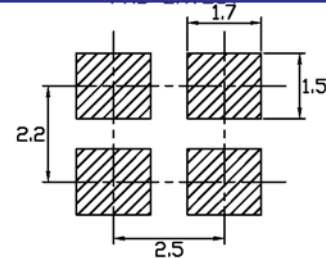
**PIN FUNCTION**  
 1 CONTROL  
 2 GND  
 3 OUTPUT  
 4 Vdd

**PIN FUNCTION**  
 1 Vcont  
 2 GND  
 3 OUT  
 4 Vcc

**Recommended Solder Pad Layout**



**Recommended Solder Pad Layout**



*Note: Bypass Vdd to GND with a 0.01µF capacitor*

