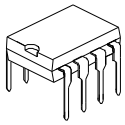
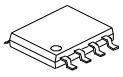
POWER FACTOR CORRECTION CONTROLLER OF CRITICAL DUCTING

DESCRIPTION

The SA7527 provides simple and high performance active power factor correction. The SA7527 is optimized for electronic ballasts and low power and high-density power supplies which require minimum board size, reduced external components and low power dissipation. Because the R/C filter is included in the current sense block, the external R/C filter is not necessary. Special circuitry has also been added to prevent no load runaway conditions. Regardless of the supply voltage, the output drive clamping circuit limits the overshoot of the power MOSFET gate drive. It greatly enhances the system reliability.



DIP-8-300-2.54



SOP-8-225-1.27

FEATURES

* Internal start-up timer
* Internal R/C filter eliminates the need for an external R/C filter
* Very precise adjustable output over voltage protection
* Zero current detector
* One quadrant multiplier
* Trimmed 1.5% internal band gap reference
* Under voltage lockout with 3V of hysteresis
* Totem pole output with high state clamp
* Low start-up and operating current
* 8-pin DIP or 8-pin SOP

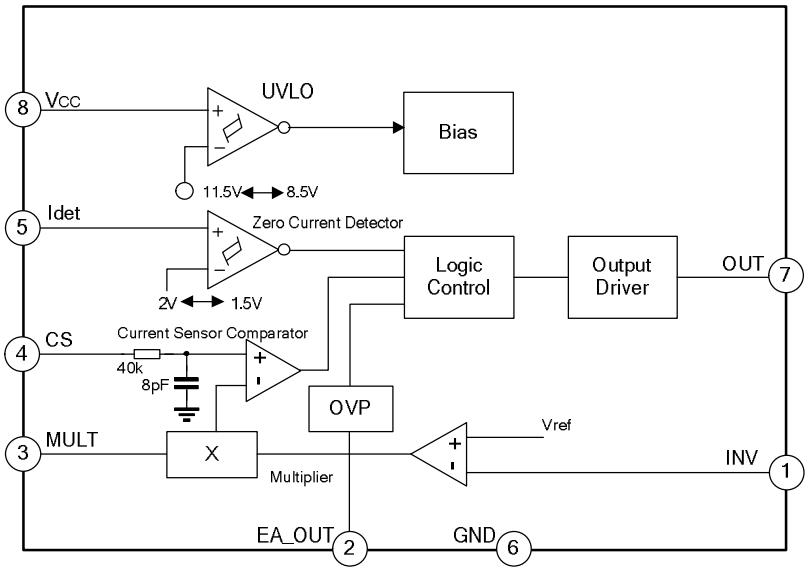
ORDERING INFORMATION

Device	Package
SA7527	DIP-8-300-2.54
SA7527S	SOP-8-225-1.27

APPLICATIONS

* Electronic ballast
* SMPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_{amb}=25°C)

Characteristics	Symbol	Rating	Unit
Supply Voltage	V_{CC}	30	V
Peak Drive Output Current	I_{OH}, I_{OL}	±500	mA
Driver Output Clamping Diodes V_O>V_{CC} or V_O<-0.3V	Iclamp	±10	mA
Detector Clamping Diodes	Idet	±10	mA
Error Amp, Multiplier And Comparator Input Voltage	Vin	-0.3 to 6	V
Operating Junction Temperature	Tj	150	°C
Operating Temperature Range	T_{opr}	-25 to 125	°C
Storage Temperature Range	T_{stg}	-65 to 150	°C
Power Dissipation	P_d	0.8	W

TEMPERATURE CHARACTERISTICS

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Temperature Stability For Reference Voltage (Vref)	ΔVref	--	20	--	mV
Temperature Stability For Multiplier Gain (K)	ΔK/ΔT	--	-0.2	--	%/°C

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, V_{CC}=14V, -25°C ≤T_{amb}≤125°C)

Characteristics	Symbol	Test condition	Min.	Typ.	Max.	Unit
Under Voltage Lockout Section						
Start Threshold Voltage	$V_{th\ (st)}$	V_{CC} increasing	10.5	11.5	12.5	V
UVLO Hysteresis	$H_{Y\ (st)}$	--	2	3	4	V
Supply Current Section						
Start-Up Supply Current	I_{st}	V_{CC}=Vth(st)-0.2	10	60	100	μA
Operating Supply Current	I_{CC}	Output not switching	--	3	6	mA
Operating Current OVP	$I_{CC(OVP)}$	Vinv=3V	--	1.7	4	mA
Dynamic Operating Supply Current	I_{DCC}	50kHz, Cl=1nF	--	4	8	mA
Error Amplifier Section						
Voltage Feedback Input Threshold	V_{ref}	Iref=0mA, Tamb=25°C	2.465	2.5	2.535	V
		-25≤Tamb≤125°C	2.44	2.5	2.56	V
Line Regulation	ΔV_{ref1}	14V≤VCC≤25V	--	0.1	10	mV
Temperature Stability Of Vref (note)	ΔV_{ref3}	-25≤Tamb≤125°C	--	20	--	mV
Input Bias Current	$I_{b(ea)}$	--	-0.5	--	0.5	μA
Output Source Current	I_{source}	Vm2=4V	-2	-4	--	mA
Output Sink Current	I_{sink}	Vm2=4V	2	4	--	mA
Output Upper Clamp Voltage (note)	$V_{eao(H)}$	Isource=0.1mA	--	6	--	V
Output Lower Clamp Voltage (note)	$V_{eao(L)}$	Isink=0.1mA	--	2.25	--	V

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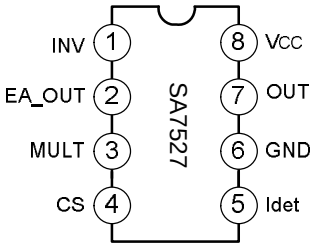
Characteristics	Symbol	Test condition	Min.	Typ.	Max.	Unit
Large Signal Open Loop G gain (note)	Gv	--	60	80	--	dB
Power Supply Rejection Ratio (note)	PSRR	14V≤VCC≤25V	60	80	--	dB
Unity Gain Bandwidth (note)	GBW	--	--	1	--	MHz
Slew Rate (note)	SR	--	--	0.6	--	V/μs
Multiplier Section						
Input Bias Current (pin3)	Ib(m)	--	-0.5	--	0.5	μA
M1 Input Voltage Range (pin3)	ΔVm1	--	0	--	3.8	V
M2 Input Voltage Range (pin2)	ΔV_{m2}	--	V_{ref}	--	V_{ref}+2.5	V
Multiplier Gain (note)	K	Vm1=1V, Vm2=3.5V	0.36	0.44	0.52	1/V
Maximum Multiplier Output Voltage	$V_{omax(m)}$	Vinv=0V, Vm1=4V	1.65	1.8	1.95	V
Temperature Stability Of K (note)	ΔK/ΔT	-25≤Tamb≤125°C	--	-0.2	--	%/°C
Current Sense Section						
Input Offset Voltage (note)	$V_{io(cs)}$	Vm1=0V, Vm2=2.2V	-10	3	10	mV
Input Bias Current	$I_{b(cs)}$	0V≤Vcs≤1.7V	-1	-0.1	1	μA
Current Sense Delay To Output (note)	td(cs)	--	--	200	500	ns
Zero Current Detect Section						
Input Voltage Threshold	$V_{th(det)}$	V_{det} increasing	1.7	2	2.3	V
Detect Hysteresis	$H_{Y(det)}$	--	0.2	0.5	0.8	V
Input Low Clamp Voltage	$V_{clamp(l)}$	Idet=-100μA	0.45	0.75	1	V
Input High Clamp Voltage	$V_{clamp(h)}$	Idet=3mA	6.5	7.2	7.9	V
Input Bias Current	$I_{b(det)}$	1V≤V_{det}≤5V	-1	-0.1	1	μA
Input High/Low Clamp Diode Current (note)	$I_{clamp(d)}$	--	--	--	±3	mA
Output Section						
Output Voltage High	V_{oh}	I_O=-10mA	10.5	11	--	V
Output Voltage Low	V_{oi}	I_O=10mA	--	0.8	1	V
Rising Time (note)	tr	Cl=1nF	--	130	200	ns
Falling Time (note)	tf	Cl=1nF	--	50	120	ns
Maximum Output Voltage	$V_{omax(o)}$	V_{CC}=20V, I_O=100μA	12	14	16	V
Output Voltage With UVLO Activated	$V_{omin(o)}$	V_{CC}=5V, I_O=100μA	--	--	1	V
Restart Timer Section						
Restart Time Delay	td(rst)	V_{m1}=1V, V_{m2}=3.5V	--	150	--	μs
Over Voltage Protection Section						
Soft OVP Detecting Current	I_{sovp}	--	25	30	35	μA
Dynamic OVP Detecting Current	I_{dovp}	--	35	40	45	μA
Static OVP Threshold Voltage	V_{ovp}	V_{inv}=2.7V	2.1	2.25	2.4	V

Note: These parameters, although guaranteed, are not 100% tested in production.

Multiplier gain: $k = \frac{pin4\_threshold}{Vm1x(Vm2 - Vref)} \cdots (Vm1 = Vpin3, Vm2 = Vpin2)$

PIN CONFIGURATIONS



PIN DESCRIPTIONS

Pin no.	Pin name	Description
1	INV	Inverting input of the error amplifier. The output of the boost converter should be resistively divided to 2.5V and connected to this pin.
2	EA_OUT	The output of the error amplifier. A feedback compensation network is placed between this pin and the INV pin.
3	MULT	Input to the multiplier stage. The full-wave rectified AC voltage is divided to less than 2V and is connected to this pin.
4	CS	Input of the PWM comparator. The MOSFET current is sensed by a resistor and the resulting voltage is applied to this pin. An internal R/C filter is included to reject any high frequency noise.
5	Idet	Zero current detection input.
6	GND	The ground potential of all the pins.
7	OUT	Gate driver output. The push pull output stage is able to drive the Power MOSFET with peak current of 500mA.
8	VCC	Supply voltage of driver and control circuits.

ELECTRICAL CHARACTERISTICS CURVES

Figure 1. Error Amplifier Output Voltage vs Current Sensing Threshold

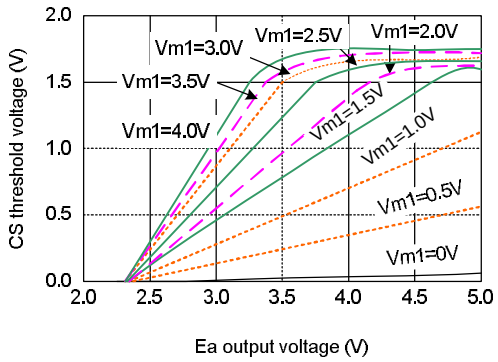


Figure 2. Multiplier Input Voltage vs Current Sensing Threshold

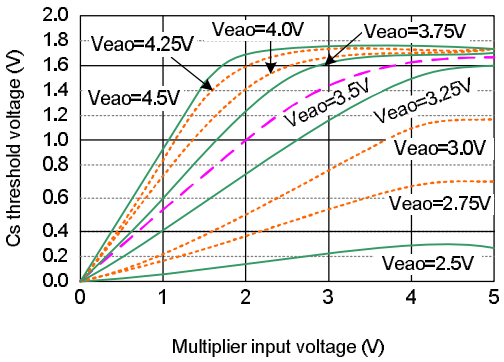


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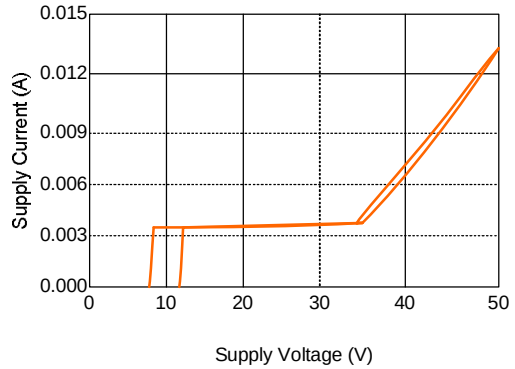
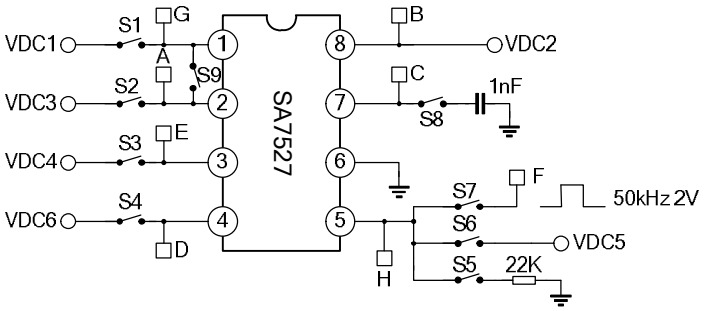
Figure 3. Supply Current vs Supply Voltage



TEST CIRCUIT



TEST SPECIFICATION (Unless otherwise specified, V_{DC2}=14V)

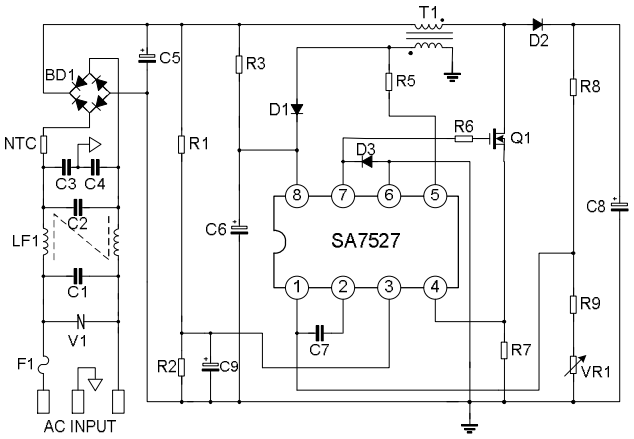
Parameter	Switches	Test conditions	Test point	Remark
$V_{th(st)}$	S2,S3,S4,S5	V_{DC3}=3,V_{DC4}=1,V_{DC6}=0	B	V_{DC2} increase
$H_{Y(st)}$	S2,S3,S4,S5	V_{DC3}=3,V_{DC4}=1,V_{DC6}=0	B	Following above, decrease the V_{DC2} until C level changed
$I_{(st)}$	S2,S3,S4,S5	V_{DC3}=3,V_{DC4}=1,V_{DC6}=0	B	V_{DC2}= $V_{th(st)}$-0.2
$I_{(cc)}$	S2,S3,S4,S5	V_{DC3}=3,V_{DC4}=1,V_{DC6}=0	B	--
$I_{cc(ovp)}$	S1	V_{DC1}=3	B	--
I_{dcc}	S1,S3,S4,S7,S8	V_{DC6}=0	B	Input 50kHz/2V square wave to F
V_{ref}	S9	--	G	
ΔV_{ref}	S9	--	G	V_{DC2}=14V、25V
$I_{b(ea)}$	S1	V_{DC1} change	G	--
$I_{(source)}$	S1,S2	V_{DC1}=0,V_{DC3}=4	A	--
$I_{(sink)}$	S1,S2	V_{DC1}=3,V_{DC3}=4	A	--
$V_{eao(H)}$	S1	V_{DC1}=0	A	The source current of A is 1mA
$V_{eao(L)}$	S1	V_{DC1}=3	A	The sink current of A is 1mA
$I_{b(m)}$	S3	--	E	V_{DC4}: 0~4V

(To be continued)

(Continued)

Parameter	Switches	Test conditions	Test point	Remark
ΔVm1	S1,S3,S4,S5	VDC1=2, initialize VDC4,VDC6 low level, enable C high level	E	Increasing the VDC6 and VDC4, enables the C changes until the VDC4 change do not affect the C level.
ΔVm2	S1,S2,S3,S4,S5	VDC1=2,VDC4=1, initialize VDC3, VDC6 low level, enable C high level.	A	Increasing the VDC6 and VDC3 level, enables the C changes until the VDC3 change do not affect the C level.
K	S1,S2,S3,S4	VDC1=2V,VDC3=3.5,VDC4=1V	--	Increase the VDC6 until C level changed. K=VDC6/(VDC3*VDC4)
Vomax	S1,S3,S4,S5	VDC1=2V, VDC4=4	D	Increase the VDC6 until C level changed.
Ib(cs)	S4	--	D	VDC6:0~1.7V
Vth(det)	S1,S2,S3,S4,S6	VDC1=2V, VDC3=3,VDC4=1, VDC6=0,	G	Increase the VDC5 until C level changed.
HY(det)	S1,S2,S3,S4,S6	VDC1=2V, VDC3=3,VDC4=1, VDC6=0,	G	Following above, the VDC5 decreases until C level changed.
Vclamp(L)	--	--	G	Input 100μA to G
Vclamp(H)	--	--	G	Output 3mA from G
Ib(det)	S6	--	G	VDC5:1~5V
Voh	S1,S2,S3,S4,S5	VDC1=2,VDC6=0	C	Output 10mA from C
Vol	S1,S2,S3,S4,S5	VDC1=2,VDC6=2	C	Input 10mA to C
tr	S1,S2,S3,S4,S7	VDC1=2,VDC6=0	C	Input 50kHz/2V square wave to F
tf	S1,S2,S3,S4,S7	VDC1=2,VDC6=0	C	Input 50kHz/2V square wave to F
Vomax(o)	S1,S2,S3,S4,S5	VDC1=2,VDC2=20	C	Output 100μA from C
Vomin(o)	S1,S2,S3,S4,S5	VDC1=2,VDC2=5	C	Output 100μA from C
td(rst)	S1,S2,S3,S5	VDC1=2,VDC3=3.5,VDC4=1	C	Input 10kHz, 10μs, 2V narrow pulse to D (note1)
Isovp	S1,S3,S4,S5	VDC1=2,VDC6=0	A	Input static current to A, and enables C low level.
Idovp	S1,S3,S4,S5	VDC1=2,VDC6=0	A	Input dynamic current to A, and enable C low level.
Vovp	S1,S2,S3,S4,S5	VDC1=2.7,VDC4=1,VDC6=0	A	Increase the VDC3 until C level changed.
tf	S1,S2,S3,S4,S7	VDC1=2,VDC6=0	C	Input 50kHz/2V square wave to F

TYPICAL APPLICATION CIRCUIT



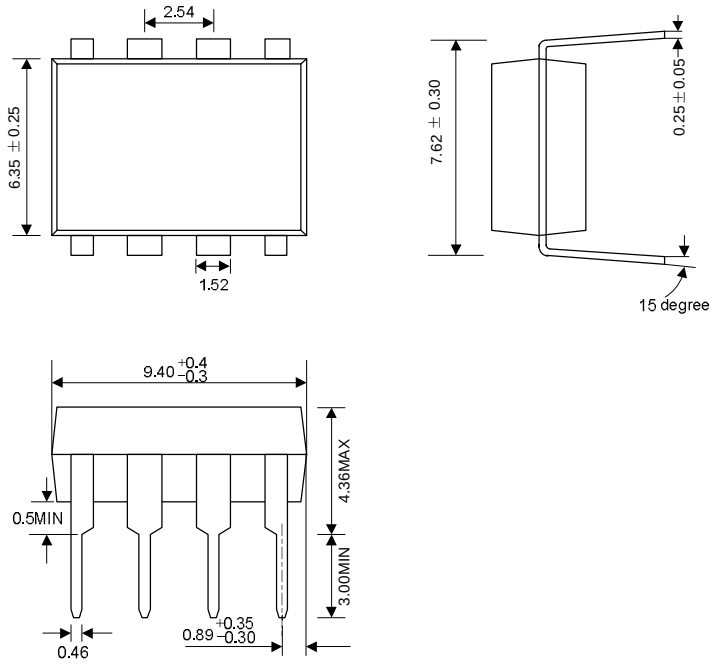
Note:The circuit and parameters are reference only, please set the parameters of the real application circuit based on the real test .

APPLICATION CIRCUIT COMPONENTS LIST

Part Number	Value	Note	Manufacturer
R1	1.8MΩ	1/4W	-
R2	18kΩ	1/4W	-
R3	120kΩ	1W	-
R5	22kΩ	1/4W	-
R6	10Ω	1/4W	-
R7	3.0Ω	1W	-
R8	1MΩ	1/4W	-
R9	6kΩ	1/4W	-
VR1	103	Variable resistor	-
C1	47nF, 275vac	Box-Cap	-
C2	100nF, 275vac	Box-Cap	-
C3,4	2200pF, 3000V	Y-Cap	-
C5	0.1μF, 630V	Miller-Cap	-
C6	47μF, 35V	Electrolytic	-
C7	1μF	MLCC	-
C8	22μF, 450V	Electrolytic	-
C9	1nF, 25V	Ceramic	-
BD1	600V/4A	Bridge Diode	-
D1,3	75V, 150mA	IN4148	-
D2	600V, 1A	BYV26C	-
LF1	45mH	Line Filter	-
T1	1.76mH(122T:10T)	EI2219	-
Q1	500V, 2.3A	FQPF4N50	Fairchild
F1	250V, 3A	Fuse	-
V1	470V	471	-
NTC	10Ω	10D09	-

PACKAGE OUTLINE

DIP-8-300-2.54 UNIT: mm



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