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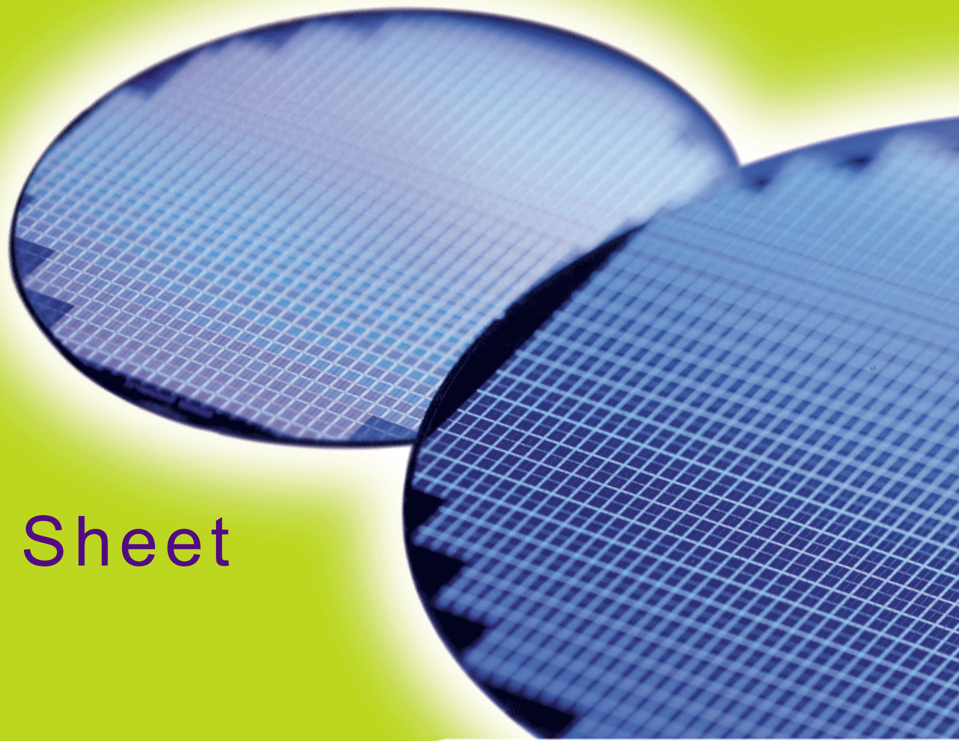
HYS64T32x00HDL–[25F/2.5/3/3S/3.7/5]–B
HYS64T64x20HDL–[25F/2.5/3/3S/3.7/5]–B
HYS64T128x21HDL–[25F/2.5/3/3S/3.7/5]–B

200 Pin Small-Outlined DDR2 SDRAMs Modules
DDR2 SDRAM
SO-DIMM SDRAM
RoHS Compliant



Internet Data Sheet

Rev. 1.1

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HYS64T32x00HDL–[25F/2.5/3/3S/3.7/5]–B, HYS64T64x20HDL–[25F/2.5/3/3S/3.7/5]–B, HYS64T128x21HDL–[25F/2.5/3/3S/3.7/5]–B **Revision History: 2006-10, Rev. 1.1**	
Page	**Subjects (major changes since last revision)**
All	Adapted internet edition
4	Added –25F Product Types; Added 6Layer –3S and –3.7 Product Types
70, 71, 72	Updated Package Outline Drawings
Previous Revision: 2005-09, Rev 1.01	
All	Qimonda update
15	Modified AC Timing Parameters
Previous Revision: 2005-06, Rev 1.0	

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1 Overview

This chapter gives an overview of the 200 Pin Small-Outlined DDR2 SDRAMs Modules product family and describes its main characteristics.

1.1 Features

- 200-Pin PC2–6400, PC2–5300, PC2–4200 and PC2–3200 DDR2 SDRAM memory modules for use as main memory when installed in systems such as mobile personal computers.
- 32M × 64, 64M × 64 and 128M × 64 module organization and 32M × 16, 64M × 8 chip organization
- 256MB, 512MB and 1GB modules built with 512-Mbit DDR2 SDRAMs in P-TFBGA-84 and P-TFBGA-60 chipsize packages
- Standard Double-Data-Rate-Two Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply
- All speed grades faster than DDR2–400 comply with DDR2–400 timing specifications.
- Programmable CAS Latencies (3, 4 ,5 and 6), Burst Length (8 & 4) and Burst Type
- Average Refresh Period 7.8 µs at a T_{CASE} lower than 85°C, 3.9µs between 85°C and 95°C.
- Auto Refresh (CBR) and Self Refresh
- Programmable self refresh rate via EMRS2 setting
- Programmable partial array refresh via EMRS2 settings
- DCC enabling via EMRS2 setting
- All inputs and outputs SSTL_1.8 compatible
- Off-Chip Driver Impedance Adjustment (OCD) and On-Die Termination (ODT)
- Serial Presence Detect with E^2PROM
- SO-DIMM Dimensions (nominal): 30 mm high, 67.60 mm wide
- Based on standard reference layouts Raw Card “A”, “C”,”E”
- RoHS compliant products[1)]

TABLE 1
Performance Table

Product Type Speed Code			**–25F**	**–2.5**	**–3**	**–3S**	**–3.7**	**–5**	**Unit**
Speed Grade			**PC2–6400 5–5–5**	**PC2–6400 6–6–6**	**PC2–5300 4–4–4**	**PC2–5300 5–5–5**	**PC2–4200 4–4–4**	**PC2–3200 3–3–3**	**—**
Max. Clock Frequency	@CL6	f_{CK6}	400	400	–	–	–	–	MHz
	@CL5	f_{CK5}	400	333	333	333	266	200	MHz
	@CL4	f_{CK4}	266	266	333	266	266	200	MHz
	@CL3	f_{CK3}	200	200	200	200	200	200	MHz
Min. RAS-CAS-Delay		t_{RCD}	12.5	15	12	15	15	15	ns
Min. Row Precharge Time		t_{RP}	12.5	15	12	15	15	15	ns
Min. Row Active Time		t_{RAS}	45	45	45	45	45	40	ns
Min. Row Cycle Time		t_{RC}	57.5	60	57	60	60	55	ns

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

1.2 Description

The Qimonda HYS64T[32/64/128]xxxHDL-[25F/2.5/3/3S/3.7/5]-B module family are small outline DIMM modules "SO-DIMMs" with 30 mm height based on DDR2 technology. DIMMs are available as non-ECC modules in 32M × 64 (256 MB), 64M × 64 (512 MB) and 128M × 64(1 GB) organization and density, intended for mounting into 200-pin connector sockets.

The memory array is designed with 512-Mbit Double-Data-Rate-Two (DDR2) Synchronous DRAMs. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and are write protected; the second 128 bytes are available to the customer.

TABLE 2
Ordering Information for RoHS Compliant Products

Product Type[1)]	Compliance Code[2)]	Description	SDRAM Technology
PC2–6400			
HYS64T32000HDL–25F–B	256 MB 1R×16 PC2–6400S–555–12–C0	1 Rank, Non-ECC	512 Mbit (×16)
HYS64T64020HDL–25F–B	512 MB 2R×16 PC2–6400S–555–12–A0	2 Rank, Non-ECC	512 Mbit (×16)
HYS64T128021HDL–25F–B	1 GB 2Rx8 PC2-6400S–555–12–E0	2 Rank, Non-ECC	512 Mbit (×8)
PC2–6400			
HYS64T32000HDL–2.5–B	256 MB 1R×16 PC2–6400S–666–12–C0	1 Rank, Non-ECC	512 Mbit (×16)
HYS64T64020HDL–2.5–B	512 MB 2R×16 PC2–6400S–666–12–A0	2 Rank, Non-ECC	512 Mbit (×16)
HYS64T128021HDL–2.5–B	1 GB 2Rx8 PC2-6400S–666–12–E0	2 Rank, Non-ECC	512 Mbit (×8)
PC2–5300			
HYS64T32000HDL–3–B	256 MB 1R×16 PC2–5300S–444–12–C0	1 Rank, Non-ECC	512 Mbit (×16)
HYS64T64020HDL–3–B	512 MB 1R×16 PC2–5300S–444–12–A0	2 Rank, Non-ECC	512 Mbit (×16)
HYS64T128021HDL–3–B	1 GB 2Rx8 PC2-5300S–444–12–E0	2 Rank, Non-ECC	512 Mbit (×8)
PC2–5300			
HYS64T32000HDL–3S–B HYS64T32900HDL–3S–B	256 MB 1R×16 PC2–5300S–555–12–C0	1 Rank, Non-ECC	512 Mbit (×16)
HYS64T64020HDL–3S–B HYS64T64920HDL–3S–B	512 MB 1R×16 PC2–5300S–555–12–A0	2 Rank, Non-ECC	512 Mbit (×16)
HYS64T128021HDL–3S–B HYS64T128921HDL–3S–B	1 GB 2Rx8 PC2-5300S–555–12–E0	2 Rank, Non-ECC	512 Mbit (×8)
PC2–4200			
HYS64T32000HDL–3.7–B HYS64T32900HDL–3.7–B	256 MB 1R×16 PC2–4200S–444–12–C0	1 Rank, Non-ECC	512 Mbit (×16)
HYS64T64020HDL–3.7–B HYS64T64920HDL–3.7–B	512 MB 1R×16 PC2–4200S–444–12–A0	2 Rank, Non-ECC	512 Mbit (×16)
HYS64T128021HDL–3.7–B HYS64T128921HDL–3.7–B	1 GB 2Rx8 PC2-4200S–444–12–E0	2 Rank, Non-ECC	512 Mbit (×8)

Product Type[1]	Compliance Code[2]	Description	SDRAM Technology
PC2–3200			
HYS64T32000HDL–5–B	256 MB 1R×16 PC2–3200S–333–12–C0	1 Rank, Non-ECC	512 Mbit (×16)
HYS64T64020HDL–5–B	512 MB 1R×16 PC2–3200S–333–12–A0	2 Rank, Non-ECC	512 Mbit (×16)
HYS64T128021HDL–5–B	1 GB 2Rx8 PC2-3200S–333–12–E0	2 Rank, Non-ECC	512 Mbit (×8)

1) All Product Type numbers end with a place code, designating the silicon die revision. Example: HYS64T64020HDL–3.7–B, indicating Rev. "B" dies are used for DDR2 SDRAM components. For all Qimonda DDR2 module and component nomenclature see **Chapter 6** of this data sheet.
2) The Compliance Code is printed on the module label and describes the speed grade, for example "PC2–4200S–444–12–A0", where 4200S means small-outlined unbuffered DIMM modules with 4.26 GB/sec Module Bandwidth and "444-12" means Column Address Strobe (CAS) latency = 4, Row Column Delay (RCD) latency = 4 and Row Precharge (RP) latency = 4 using the latest JEDEC SPD Revision 1.2 and produced on the Raw Card "A".

TABLE 3
Address Format

DIMM Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/column bits	Raw Card
256 MByte	32M × 64	1	Non-ECC	4	13/2/10	C
512 MByte	64M × 64	2	Non-ECC	8	13/2/10	A
1 GByte	128M × 64	2	Non-ECC	16	14/2/10	E

TABLE 4
Components on Modules

Product Type[1]	DRAM Components[1]	DRAM Density	DRAM Organisation	Note[2]
HYS64T32000HDL HYS64T32900HDL	HYB18T512160BF	512 Mbit	32M × 16	
HYS64T64020HDL HYS64T64920HDL	HYB18T512160BF	512 Mbit	32M × 16	
HYS64T128021HDL HYS64T128921HDL	HYB18T512800BF	512 Mbit	64M × 8	

1) Green Product
2) For a detailed description of all functionalities of the DRAM components on these modules see the component data sheet.

2 Chip Configuration

2.1 Chip Configuration

The chip configuration of the Small Outline DDR2 SDRAM DIMM is listed by function in **Table 5** (200 balls). The abbreviations used in columns Ball and Buffer Type are explained in **Table 6** and **Table 7** respectively. The Ball numbering is depicted in **Figure 1**.

TABLE 5
Chip Configuration of SO-DIMM

Ball No.	Name	Pin Type	Buffer Type	Function
Clock Signals				
30	CK0	I	SSTL	**Clock Signals 2:0, Complement Clock Signals 2:0**
164	CK1	I	SSTL	
32	$\overline{\text{CK0}}$	I	SSTL	
166	$\overline{\text{CK1}}$	I	SSTL	
79	CKE0	I	SSTL	**Clock Enable Rank 1:0**
80	CKE1	I	SSTL	*Note: 2 Ranks module*
	NC	NC	—	**Not Connected** *Note: 1-rank module*
Control Signals				
110	$\overline{\text{S0}}$	I	SSTL	**Chip Select Rank 1:0**
115	$\overline{\text{S1}}$	I	SSTL	
	NC	NC	—	**Not Connected** *Note: 1-rank module*
108	$\overline{\text{RAS}}$	I	SSTL	**Row Address Strobe**
113	$\overline{\text{CAS}}$	I	SSTL	**Column Address Strobe**
109	$\overline{\text{WE}}$	I	SSTL	**Write Enable**
Address Signals				
107	BA0	I	SSTL	**Bank Address Bus 2:0**
106	BA1	I	SSTL	
85	BA2	I	SSTL	**Bank Address Bus 2** Greater than 512Mb DDR2 SDRAMS
	NC	NC	SSTL	**Less than 1Gb DDR2 SDRAMS**

Ball No.	Name	Pin Type	Buffer Type	Function
102	A0	I	SSTL	**Address Bus 12:0**
101	A1	I	SSTL	
100	A2	I	SSTL	
99	A3	I	SSTL	
98	A4	I	SSTL	
97	A5	I	SSTL	
94	A6	I	SSTL	
92	A7	I	SSTL	
93	A8	I	SSTL	
91	A9	I	SSTL	
105	A10	I	SSTL	
	AP	I	SSTL	
90	A11	I	SSTL	
89	A12	I	SSTL	**Address Signal 12** *Note: Module based on 256 Mbit or larger dies*
116	A13	I	SSTL	**Address Signal 13** *Note: 1 Gbit based module*
	NC	NC	—	**Not Connected** *Note: Module based on 512 Mbit or smaller dies*
Data Signals				
5	DQ0	I/O	SSTL	**Data Bus 63:0** *Note: Data Input/Output Balls*
7	DQ1	I/O	SSTL	
17	DQ2	I/O	SSTL	
19	DQ3	I/O	SSTL	
4	DQ4	I/O	SSTL	
6	DQ5	I/O	SSTL	
14	DQ6	I/O	SSTL	
16	DQ7	I/O	SSTL	
23	DQ8	I/O	SSTL	
25	DQ9	I/O	SSTL	
35	DQ10	I/O	SSTL	
37	DQ11	I/O	SSTL	

Ball No.	Name	Pin Type	Buffer Type	Function
20	DQ12	I/O	SSTL	**Data Bus 63:0** Data Input/Output Balls
22	DQ13	I/O	SSTL	
36	DQ14	I/O	SSTL	
38	DQ15	I/O	SSTL	
43	DQ16	I/O	SSTL	
45	DQ17	I/O	SSTL	
55	DQ18	I/O	SSTL	
57	DQ19	I/O	SSTL	
44	DQ20	I/O	SSTL	
46	DQ21	I/O	SSTL	
56	DQ22	I/O	SSTL	
58	DQ23	I/O	SSTL	
61	DQ24	I/O	SSTL	
63	DQ25	I/O	SSTL	
73	DQ26	I/O	SSTL	
75	DQ27	I/O	SSTL	
62	DQ28	I/O	SSTL	
64	DQ29	I/O	SSTL	
74	DQ30	I/O	SSTL	
76	DQ31	I/O	SSTL	
123	DQ32	I/O	SSTL	
125	DQ33	I/O	SSTL	
135	DQ34	I/O	SSTL	
137	DQ35	I/O	SSTL	
124	DQ36	I/O	SSTL	
126	DQ37	I/O	SSTL	
134	DQ38	I/O	SSTL	
136	DQ39	I/O	SSTL	
141	DQ40	I/O	SSTL	
143	DQ41	I/O	SSTL	
151	DQ42	I/O	SSTL	
153	DQ43	I/O	SSTL	
140	DQ44	I/O	SSTL	
142	DQ45	I/O	SSTL	
152	DQ46	I/O	SSTL	
154	DQ47	I/O	SSTL	
157	DQ48	I/O	SSTL	
159	DQ49	I/O	SSTL	
173	DQ50	I/O	SSTL	
175	DQ51	I/O	SSTL	

Ball No.	Name	Pin Type	Buffer Type	Function
158	DQ52	I/O	SSTL	**Data Bus 63:0**
160	DQ53	I/O	SSTL	
174	DQ54	I/O	SSTL	
176	DQ55	I/O	SSTL	
179	DQ56	I/O	SSTL	
181	DQ57	I/O	SSTL	
189	DQ58	I/O	SSTL	
191	DQ59	I/O	SSTL	
180	DQ60	I/O	SSTL	
182	DQ61	I/O	SSTL	
192	DQ62	I/O	SSTL	
194	DQ63	I/O	SSTL	
Data Strobe Signals				
13	DQS0	I/O	SSTL	**Data Strobe Bus 7:0**
11	$\overline{DQS0}$	I/O	SSTL	
31	DQS1	I/O	SSTL	
29	$\overline{DQS1}$	I/O	SSTL	
51	DQS2	I/O	SSTL	
49	$\overline{DQS2}$	I/O	SSTL	
70	DQS3	I/O	SSTL	
68	$\overline{DQS3}$	I/O	SSTL	
131	DQS4	I/O	SSTL	
129	$\overline{DQS4}$	I/O	SSTL	
148	DQS5	I/O	SSTL	
146	$\overline{DQS5}$	I/O	SSTL	
169	DQS6	I/O	SSTL	
167	$\overline{DQS6}$	I/O	SSTL	
188	DQS7	I/O	SSTL	
186	$\overline{DQS7}$	I/O	SSTL	
Data Mask Signals				
10	DM0	I	SSTL	**Data Mask Bus 7:0**
26	DM1	I	SSTL	
52	DM2	I	SSTL	
67	DM3	I	SSTL	
130	DM4	I	SSTL	
147	DM5	I	SSTL	
170	DM6	I	SSTL	
185	DM7	I	SSTL	

Ball No.	Name	Pin Type	Buffer Type	Function
EEPROM				
197	SCL	I	CMOS	**Serial Bus Clock**
195	SDA	I/O	OD	**Serial Bus Data**
198	SA0	I	CMOS	**Serial Address Select Bus 2:0**
200	SA1	I	CMOS	
Power Supplies				
1	V_{REF}	AI	—	**I/O Reference Voltage**
199	V_{DDSPD}	PWR	—	**EEPROM Power Supply**
81,82,87,88,95,96,103,104, 111,112,117,118	V_{DD}	PWR	—	**Power Supply**
2,3,8,9,12,15,18,21,24,27,28, 33,34,39,40,41,42,47,48,53, 54,59,60,65,66,71,72,77,78, 121,122,127,128,132,133,138,13 9,144,145,149,150,155,156,, 161,162,165,171,172,177, 178,183,184,187,190,193,196	V_{SS}	GND	—	**Ground Plane**
Other Balls				
114	ODT0	I	SSTL	**On-Die Termination Control 1:0**
119	ODT1	I	SSTL	**On-Die Termination Control 1** *Note: 2 Rank modules*
	NC	NC	—	**Not Connected** *Note: 1 Rank modules*
50,69,83,84,120,163,168	NC	NC	—	**Not connected**

TABLE 6
Abbreviations for Ball Type

Abbreviation	Description
I	Standard input-only Ball. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

TABLE 7
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding ball has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

FIGURE 1

Chip Configuration SO-DIMM (200 Ball)

Front Side Pin	Signal	Back Side Pin	Signal
Pin 001	V_{REF}	Pin 002	V_{SS}
Pin 003	V_{SS}	Pin 004	DQ4
Pin 005	DQ0	Pin 006	DQ5
Pin 007	DQ1	Pin 008	V_{SS}
Pin 009	V_{SS}	Pin 010	DM0
Pin 011	$\overline{DQS0}$	Pin 012	V_{SS}
Pin 013	DQS0	Pin 014	DQ6
Pin 015	V_{SS}	Pin 016	DQ7
Pin 017	DQ2	Pin 018	V_{SS}
Pin 019	DQ3	Pin 020	DQ12
Pin 021	V_{SS}	Pin 022	DQ13
Pin 023	DQ8	Pin 024	V_{SS}
Pin 025	DQ9	Pin 026	DM1
Pin 027	V_{SS}	Pin 028	V_{SS}
Pin 029	$\overline{DQS1}$	Pin 030	CK0
Pin 031	DQS1	Pin 032	$\overline{CK0}$
Pin 033	V_{SS}	Pin 034	V_{SS}
Pin 035	DQ10	Pin 036	DQ14
Pin 037	DQ11	Pin 038	DQ15
Pin 039	V_{SS}	Pin 040	V_{SS}
Pin 041	V_{SS}	Pin 042	V_{SS}
Pin 043	DQ16	Pin 044	DQ20
Pin 045	DQ17	Pin 046	DQ21
Pin 047	V_{SS}	Pin 048	V_{SS}
Pin 049	$\overline{DQS2}$	Pin 050	NC/$\overline{EVENT}$
Pin 051	DQS2	Pin 052	DM2
Pin 053	V_{SS}	Pin 054	V_{SS}
Pin 055	DQ18	Pin 056	DQ22
Pin 057	DQ19	Pin 058	DQ23
Pin 059	V_{SS}	Pin 060	V_{SS}
Pin 061	DQ24	Pin 062	DQ28
Pin 063	DQ25	Pin 064	DQ29
Pin 065	V_{SS}	Pin 066	V_{SS}
Pin 067	DM3	Pin 068	$\overline{DQS3}$
Pin 069	NC	Pin 070	DQS3
Pin 071	V_{SS}	Pin 072	V_{SS}
Pin 073	DQ26	Pin 074	DQ30
Pin 075	DQ27	Pin 076	DQ31
Pin 077	V_{SS}	Pin 078	V_{SS}
Pin 079	CKE0	Pin 080	NC/CKE1
Pin 081	V_{DD}	Pin 082	V_{DD}
Pin 083	NC	Pin 084	NC
Pin 085	NC/BA2	Pin 086	NC/A14
Pin 087	V_{DD}	Pin 088	V_{DD}
Pin 089	A12	Pin 090	A11
Pin 091	A9	Pin 092	A7
Pin 093	A8	Pin 094	A6
Pin 095	V_{DD}	Pin 096	V_{DD}
Pin 097	A5	Pin 098	A4
Pin 099	A3	Pin 100	A2
Pin 101	A1	Pin 102	A0
Pin 103	V_{DD}	Pin 104	V_{DD}
Pin 105	A10/AP	Pin 106	BA1
Pin 107	BA0	Pin 108	$\overline{RAS}$
Pin 109	$\overline{WE}$	Pin 110	$\overline{S0}$
Pin 111	V_{DD}	Pin 112	V_{DD}
Pin 113	$\overline{CAS}$	Pin 114	ODT0
Pin 115	NC/$\overline{S1}$	Pin 116	NC/A13
Pin 117	V_{DD}	Pin 118	V_{DD}
Pin 119	NC/ODT1	Pin 120	NC
Pin 121	V_{SS}	Pin 122	V_{SS}
Pin 123	DQ32	Pin 124	DQ36
Pin 125	DQ33	Pin 126	DQ37
Pin 127	V_{SS}	Pin 128	V_{SS}
Pin 129	$\overline{DQS4}$	Pin 130	DM4
Pin 131	DQS4	Pin 132	V_{SS}
Pin 133	V_{SS}	Pin 134	DQ38
Pin 135	DQ34	Pin 136	DQ39
Pin 137	DQ35	Pin 138	V_{SS}
Pin 139	V_{SS}	Pin 140	DQ44
Pin 141	DQ40	Pin 142	DQ45
Pin 143	DQ41	Pin 144	V_{SS}
Pin 145	V_{SS}	Pin 146	$\overline{DQS5}$
Pin 147	DM5	Pin 148	DQS5
Pin 149	V_{SS}	Pin 150	V_{SS}
Pin 151	DQ42	Pin 152	DQ46
Pin 153	DQ43	Pin 154	DQ47
Pin 155	V_{SS}	Pin 156	V_{SS}
Pin 157	DQ48	Pin 158	DQ52
Pin 159	DQ49	Pin 160	DQ53
Pin 161	V_{SS}	Pin 162	V_{SS}
Pin 163	NC	Pin 164	CK1
Pin 165	V_{SS}	Pin 166	$\overline{CK1}$
Pin 167	$\overline{DQS6}$	Pin 168	V_{SS}
Pin 169	DQS6	Pin 170	DM6
Pin 171	V_{SS}	Pin 172	V_{SS}
Pin 173	DQ50	Pin 174	DQ54
Pin 175	DQ51	Pin 176	DQ55
Pin 177	V_{SS}	Pin 178	V_{SS}
Pin 179	DQ56	Pin 180	DQ60
Pin 181	DQ57	Pin 182	DQ61
Pin 183	V_{SS}	Pin 184	V_{SS}
Pin 185	DM7	Pin 186	$\overline{DQS7}$
Pin 187	V_{SS}	Pin 188	DQS7
Pin 189	DQ58	Pin 190	V_{SS}
Pin 191	DQ59	Pin 192	DQ62
Pin 193	V_{SS}	Pin 194	DQ63
Pin 195	SDA	Pin 196	V_{SS}
Pin 197	SCL	Pin 198	SA0
Pin 199	V_{DD}SPD	Pin 200	SA1

MPPT0140

3 Electrical Characteristics

This chapter lists the electrical characteristics.

3.1 Absolute Maximum Ratings

Caution is needed not to exceed absolute maximum ratings of the DRAM device listed in **Table 8** at any time.

TABLE 8
Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	–1.0	+2.3	V	1)
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	–0.5	+2.3	V	1)2)
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	–0.5	+2.3	V	1)2)
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.5	+2.3	V	1)
T_{STG}	Storage Temperature	–55	+100	°C	1)2)

1) When V_{DD} and V_{DDQ} and V_{DDL} are less than 500 mV; V_{REF} may be equal to or less than 300 mV.
2) Storage Temperature is the case surface temperature on the center/top side of the DRAM.

***Attention:** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

TABLE 9
DRAM Component Operating Temperature Range

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
T_{OPER}	Operating Temperature	0	95	°C	1)2)3)4)

1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
2) The operating temperature range are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.
3) Above 85 °C the Auto-Refresh command interval has to be reduced to t_{REFI}= 3.9 µs
4) When operating this product in the 85 °C to 95 °C TCASE temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to "1". When the High Temperature Self Refresh is enabled there is an increase of I_{DD6} by approximately 50%

3.2 DC Operating Conditions

This chapter contains the DC operating conditions tables.

TABLE 10
Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
Output Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	1)
Input Reference Voltage	V_{REF}	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	2)
SPD Supply Voltage	V_{DDSPD}	1.7	—	3.6	V	
DC Input Logic High	$V_{IH(DC)}$	V_{REF} + 0.125	—	V_{DDQ} + 0.3	V	
DC Input Logic Low	$V_{IL\ (DC)}$	– 0.30	—	V_{REF} – 0.125	V	
In / Output Leakage Current	I_L	– 5	—	5	µA	3)

1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}
2) Peak to peak AC noise on V_{REF} may not exceed ± 2% V_{REF} (DC). V_{REF} is also expected to track noise in V_{DDQ}.
3) Input voltage for any connector pin under test of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V; all other pins at 0 V. Current is per pin

TABLE 11
Operating Conditions

Parameter	Symbol	Values		Unit	Note
		Min.	Max.		
Operating temperature (ambient)	T_{OPR}	0	+65	°C	
DRAM Case Temperature	T_{CASE}	0	+95	°C	1)2)3)4)
Storage Temperature	T_{STG}	– 50	+100	°C	
Barometric Pressure (operating & storage)	P_{Bar}	+69	+105	kPa	5)
Operating Humidity (relative)	H_{OPR}	10	90	%	

1) DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs.
2) Within the DRAM Component Case Temperature Range all DRAM specifications will be supported
3) Above 85 °C DRAM Case Temperature the Auto-Refresh command interval has to be reduced to t_{REFI} = 3.9 µs
4) When operating this product in the 85 °C to 95 °C T_{CASE} temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to “1”. When the High Temperature Self Refresh is enabled there is an increase of I_{DD6} by approximately 50%.
5) Up to 3000 m.

3.3 Timing Characteristics

This chapter describes the AC characteristics.

3.3.1 Speed Grade Definitions

All Speed grades faster than DDR2-DDR400B comply with DDR2-DDR400B timing specifications(t_{CK} = 5ns with t_{RAS} = 40ns). Speed Grade Definition for DDR2–800 [**Table 12**], DDR2–667 [**Table 13**], DDR2–533C [**Table 14**] and DDR2–400 [**Table 15**]

TABLE 12
Speed Grade Definition Speed Bins for DDR2–800

Speed Grade			DDR2–800D		DDR2–800E		Unit	Note
QAG Sort Name			–2.5F		–2.5			
CAS-RCD-RP latencies			5–5–5		6–6–6		t_{CK}	
Parameter		Symbol	Min.	Max.	Min.	Max.	—	
Clock Frequency	@ CL = 3	t_{CK}	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	2.5	8	3	8	ns	1)2)3)4)
	@ CL = 6	t_{CK}	2.5	8	2.5	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70000	45	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	57.5	—	60	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	12.5	—	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	12.5	—	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0)
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

TABLE 13
Speed Grade Definition Speed Bins for DDR2–667

Speed Grade			**DDR2–667C**		**DDR2–667D**		**Unit**	**Note**
QAG Sort Name			**–3**		**–3S**			
CAS-RCD-RP latencies			**4–4–4**		**5–5–5**		t_{CK}	
Parameter		**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**—**	
Clock Frequency	@ CL = 3	t_{CK}	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3	8	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3	8	3	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70000	45	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	57	—	60	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	12	—	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	12	—	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) .
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

TABLE 14
Speed Grade Definition Speed Bins for DDR2–533C

Speed Grade			DDR2–533C		Unit	Note
QAG Sort Name			–3.7			
CAS-RCD-RP latencies			4–4–4		t_{CK}	
Parameter		Symbol	Min.	Max.	—	
Clock Frequency	@ CL = 3	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3.75	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	60	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0)
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

TABLE 15
Speed Grade Definition Speed Bins for DDR2-400B

Speed Grade			DDR2–400B		Unit	Note
QAG Sort Name			–5			
CAS-RCD-RP latencies			3–3–3		t_{CK}	
Parameter		**Symbol**	**Min.**	**Max.**	**—**	
Clock Frequency	@ CL = 3	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	5	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	40	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	55	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) .
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

3.3.2 Component AC Timing Parameters

Timing Parameters for DDR2–800 [**Table 16**], DDR2–667 [**Table 17**], DDR2–533C [**Table 18**] and DDR2–400 [**Table 19**]

TABLE 16
DRAM Component Timing Parameter by Speed Grade - DDR2–800

Parameter	Symbol	DDR2–800		Unit	Note[1)2)3)4)5)6)7)8)]
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–400	+400	ps	9)
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–350	+350	ps	9)
Average clock high pulse width	$t_{CH.AVG}$	0.48	0.52	$t_{CK.AVG}$	10)11)
Average clock low pulse width	$t_{CL.AVG}$	0.48	0.52	$t_{CK.AVG}$	10)11)
Average clock period	$t_{CK.AVG}$	2500	8000	ps	10)11)
DQ and DM input setup time	$t_{DS.BASE}$	50	—	ps	12)13)14)
DQ and DM input hold time	$t_{DH.BASE}$	125	—	ps	13)14)15)
Control & address input pulse width for each input	t_{IPW}	0.6	—	$t_{CK.AVG}$	
DQ and DM input pulse width for each input	t_{DIPW}	0.35	—	$t_{CK.AVG}$	
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	9)16)
DQS/$\overline{DQS}$ low-impedance time from CK / $\overline{CK}$	$t_{LZ.DQS}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	9)16)
DQ low impedance time from CK/$\overline{CK}$	$t_{LZ.DQ}$	2 x $t_{AC.MIN}$	$t_{AC.MAX}$	ps	9)16)
DQS-DQ skew for DQS & associated DQ signals	t_{DQSQ}	—	200	ps	17)
CK half pulse width	t_{HP}	Min($t_{CH.ABS}$, $t_{CL.ABS}$)	—	ps	18)
DQ hold skew factor	t_{QHS}	—	300	ps	19)
DQ/DQS output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—	ps	20)
Write command to DQS associated clock edges	WL	RL – 1		nCK	
DQS latching rising transition to associated clock edges	t_{DQSS}	– 0.25	+ 0.25	$t_{CK.AVG}$	21)
DQS input high pulse width	t_{DQSH}	0.35	—	$t_{CK.AVG}$	
DQS input low pulse width	t_{DQSL}	0.35	—	$t_{CK.AVG}$	
DQS falling edge to CK setup time	t_{DSS}	0.2	—	$t_{CK.AVG}$	21)
DQS falling edge hold time from CK	t_{DSH}	0.2	—	$t_{CK.AVG}$	21)
Write postamble	t_{WPST}	0.4	0.6	$t_{CK.AVG}$	
Write preamble	t_{WPRE}	0.35	—	$t_{CK.AVG}$	
Address and control input setup time	$t_{IS.BASE}$	175	—	ps	22)23)
Address and control input hold time	$t_{IH.BASE}$	250	—	ps	23)24)
Read preamble	t_{RPRE}	0.9	1.1	$t_{CK.AVG}$	25)26)
Read postamble	t_{RPST}	0.4	0.6	$t_{CK.AVG}$	25)27)
CAS to CAS command delay	t_{CCD}	2	—	nCK	
Write recovery time	t_{WR}	15	—	ns	1)
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{nRP}	—	nCK	28)29)
Internal write to read command delay	t_{WTR}	7.5	—	ns	1)30)

Parameter	Symbol	DDR2–800		Unit	Note[1)2)3)4)5)6)7)8)]
		Min.	Max.		
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	1)
Exit self-refresh to a non-read command	t_{XSNR}	t_{RFC} +10	—	ns	1)
Exit self-refresh to read command	t_{XSRD}	200	—	nCK	
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	nCK	
Exit power down to read command	t_{XARD}	2	—	nCK	
Exit active power-down mode to read command (slow exit, lower power)	t_{XARDS}	8 – AL	—	nCK	
CKE minimum pulse width (high and low pulse width)	t_{CKE}	3	—	nCK	31)
Mode register set command cycle time	t_{MRD}	2	—	nCK	
MRS command to ODT update delay	t_{MOD}	0	12	ns	1)
OCD drive mode output delay	t_{OIT}	0	12	ns	1)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{IS} + t_{CK.AVG} + t_{IH}$	—	ns	

1) For details and notes see the relevant Qimonda component data sheet
2) V_{DDQ} = 1.8 V ± 0.1V; V_{DD} = 1.8 V ± 0.1 V. See notes 5)6)7)8)
3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
5) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
7) The output timing reference voltage level is V_{TT}.
8) New units, '$t_{CK.AVG}$' and 'nCK', are introduced in DDR2–667 and DDR2–800. Unit '$t_{CK.AVG}$' represents the actual $t_{CK.AVG}$ of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2–400 and DDR2–533, 't_{CK}' is used for both concepts. Example: t_{XP} = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm + 2, even if (Tm + 2 - Tm) is 2 x $t_{CK.AVG}$ + $t_{ERR.2PER(Min)}$.
9) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{ERR(6-10per)}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{ERR(6-10PER).MIN}$ = – 272 ps and $t_{ERR(6-10PER).MAX}$ = + 293 ps, then $t_{DQSCK.MIN(DERATED)} = t_{DQSCK.MIN} - t_{ERR(6-10PER).MAX}$ = – 400 ps – 293 ps = – 693 ps and $t_{DQSCK.MAX(DERATED)} = t_{DQSCK.MAX} - t_{ERR(6-10PER).MIN}$ = 400 ps + 272 ps = + 672 ps. Similarly, $t_{LZ.DQ}$ for DDR2–667 derates to $t_{LZ.DQ.MIN(DERATED)}$ = - 900 ps – 293 ps = – 1193 ps and $t_{LZ.DQ.MAX(DERATED)}$ = 450 ps + 272 ps = + 722 ps. (Caution on the MIN/MAX usage!)
10) Input clock jitter spec parameter. These parameters are referred to as 'input clock jitter spec parameters' and these parameters apply to DDR2–667 and DDR2–800 only. The jitter specified is a random jitter meeting a Gaussian distribution.
11) These parameters are specified per their average values, however it is understood that the relationship between the average timing and the absolute instantaneous timing holds all the times (min. and max of SPEC values are to be used for calculations).
12) Input waveform timing t_{DS} with differential data strobe enabled MR[bit10] = 0, is referenced from the input signal crossing at the $V_{IH.AC}$ level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the $V_{IL.AC}$ level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{il(DC)MAX}$ and $V_{ih(DC)MIN}$. See **Figure 3**.
13) If t_{DS} or t_{DH} is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
14) These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS / $\overline{DQS}$) crossing.
15) Input waveform timing t_{DH} with differential data strobe enabled MR[bit10] = 0, is referenced from the differential data strobe crosspoint to the input signal crossing at the $V_{IH.DC}$ level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the $V_{IL.DC}$ level for a rising signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{IL.DC.MAX}$ and $V_{IH.DC.MIN}$. See **Figure 3**.

16) t_{HZ} and t_{LZ} transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (t_{HZ}), or begins driving (t_{LZ}) .
17) t_{DQSQ}: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS / $\overline{\text{DQS}}$ and associated DQ in any given cycle.
18) t_{HP} is the minimum of the absolute half period of the actual input clock. t_{HP} is an input parameter but not an input specification parameter. It is used in conjunction with t_{QHS} to derive the DRAM output timing t_{QH}. The value to be used for t_{QH} calculation is determined by the following equation; t_{HP} = MIN ($t_{CH.ABS}$, $t_{CL.ABS}$), where, $t_{CH.ABS}$ is the minimum of the actual instantaneous clock high time; $t_{CL.ABS}$ is the minimum of the actual instantaneous clock low time.
19) t_{QHS} accounts for: 1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual t_{HP} at the input is transferred to the output; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and pchannel to n-channel variation of the output drivers.
20) $t_{QH} = t_{HP} - t_{QHS}$, where: t_{HP} is the minimum of the absolute half period of the actual input clock; and t_{QHS} is the specification value under the max column. {The less half-pulse width distortion present, the larger the t_{QH} value is; and the larger the valid data eye will be.} Examples: 1) If the system provides t_{HP} of 1315 ps into a DDR2–667 SDRAM, the DRAM provides t_{QH} of 975 ps minimum. 2) If the system provides t_{HP} of 1420 ps into a DDR2–667 SDRAM, the DRAM provides t_{QH} of 1080 ps minimum.
21) These parameters are measured from a data strobe signal ((L/U/R)DQS / $\overline{\text{DQS}}$) crossing to its respective clock signal (CK / $\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$, etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
22) Input waveform timing is referenced from the input signal crossing at the $V_{IH.AC}$ level for a rising signal and $V_{IL.AC}$ for a falling signal applied to the device under test. See **Figure 4**.
23) These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK / $\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$, etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
24) Input waveform timing is referenced from the input signal crossing at the $V_{IL.DC}$ level for a rising signal and $V_{IH.DC}$ for a falling signal applied to the device under test. See **Figure 4**.
25) t_{RPST} end point and t_{RPRE} begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (t_{RPST}), or begins driving (t_{RPRE}). **Figure 2** shows a method to calculate these points when the device is no longer driving (t_{RPST}), or begins driving (t_{RPRE}) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.
26) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.PER}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.PER.MIN}$ = – 72 ps and $t_{JIT.PER.MAX}$ = + 93 ps, then $t_{RPRE.MIN(DERATED)} = t_{RPRE.MIN} + t_{JIT.PER.MIN}$ = 0.9 x $t_{CK.AVG}$ – 72 ps = + 2178 ps and $t_{RPRE.MAX(DERATED)} = t_{RPRE.MAX} + t_{JIT.PER.MAX}$ = 1.1 x $t_{CK.AVG}$ + 93 ps = + 2843 ps. (Caution on the MIN/MAX usage!).
27) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.DUTY}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.DUTY.MIN}$ = – 72 ps and $t_{JIT.DUTY.MAX}$ = + 93 ps, then $t_{RPST.MIN(DERATED)} = t_{RPST.MIN} + t_{JIT.DUTY.MIN}$ = 0.4 x $t_{CK.AVG}$ – 72 ps = + 928 ps and $t_{RPST.MAX(DERATED)} = t_{RPST.MAX} + t_{JIT.DUTY.MAX}$ = 0.6 x $t_{CK.AVG}$ + 93 ps = + 1592 ps. (Caution on the MIN/MAX usage!).
28) DAL = WR + RU{t_{RP}(ns) / t_{CK}(ns)}, where RU stands for round up. WR refers to the tWR parameter stored in the MRS. For t_{RP}, if the result of the division is not already an integer, round up to the next highest integer. t_{CK} refers to the application clock period. Example: For DDR2–533 at t_{CK} = 3.75 ns with t_{WR} programmed to 4 clocks. t_{DAL} = 4 + (15 ns / 3.75 ns) clocks = 4 + (4) clocks = 8 clocks.
29) $t_{DAL.nCK}$ = WR [nCK] + $t_{nRP.nCK}$ = WR + RU{t_{RP} [ps] / $t_{CK.AVG}$[ps] }, where WR is the value programmed in the EMR.
30) t_{WTR} is at lease two clocks (2 x t_{CK}) independent of operation frequency.
31) $t_{CKE.MIN}$ of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + 2 x t_{CK} + t_{IH}.

TABLE 17
DRAM Component Timing Parameter by Speed Grade - DDR2–667

Parameter	Symbol	DDR2–667		Unit	Note[1)2)3)4)5)6)7)8)]
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–450	+450	ps	9)
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–400	+400	ps	9)
Average clock high pulse width	$t_{CH.AVG}$	0.48	0.52	$t_{CK.AVG}$	10)11)
Average clock low pulse width	$t_{CL.AVG}$	0.48	0.52	$t_{CK.AVG}$	10)11)
Average clock period	$t_{CK.AVG}$	3000	8000	ps	
DQ and DM input setup time	$t_{DS.BASE}$	100	—	ps	12)13)14)
DQ and DM input hold time	$t_{DH.BASE}$	175	—	ps	13)14)15)
Control & address input pulse width for each input	t_{IPW}	0.6	—	$t_{CK.AVG}$	
DQ and DM input pulse width for each input	t_{DIPW}	0.35	—	$t_{CK.AVG}$	
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	9)16)
DQS/$\overline{DQS}$ low-impedance time from CK / $\overline{CK}$	$t_{LZ.DQS}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	9)16)
DQ low impedance time from CK/$\overline{CK}$	$t_{LZ.DQ}$	2 x $t_{AC.MIN}$	$t_{AC.MAX}$	ps	9)16)
DQS-DQ skew for DQS & associated DQ signals	t_{DQSQ}	—	240	ps	17)
CK half pulse width	t_{HP}	Min($t_{CH.ABS}$, $t_{CL.ABS}$)	—	ps	18)
DQ hold skew factor	t_{QHS}	—	340	ps	19)
DQ/DQS output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—	ps	20)
Write command to DQS associated clock edges	WL	RL–1		nCK	
DQS latching rising transition to associated clock edges	t_{DQSS}	– 0.25	+ 0.25	$t_{CK.AVG}$	21)
DQS input high pulse width	t_{DQSH}	0.35	—	$t_{CK.AVG}$	
DQS input low pulse width	t_{DQSL}	0.35	—	$t_{CK.AVG}$	
DQS falling edge to CK setup time	t_{DSS}	0.2	—	$t_{CK.AVG}$	21)
DQS falling edge hold time from CK	t_{DSH}	0.2	—	$t_{CK.AVG}$	21)
Write postamble	t_{WPST}	0.4	0.6	$t_{CK.AVG}$	
Write preamble	t_{WPRE}	0.35	—	$t_{CK.AVG}$	
Address and control input setup time	$t_{IS.BASE}$	200	—	ps	22)23)
Address and control input hold time	$t_{IH.BASE}$	275	—	ps	23)24)
Read preamble	t_{RPRE}	0.9	1.1	$t_{CK.AVG}$	25)26)
Read postamble	t_{RPST}	0.4	0.6	$t_{CK.AVG}$	25)27)
CAS to CAS command delay	t_{CCD}	2	—	nCK	
Write recovery time	t_{WR}	15	—	ns	1)
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{nRP}	—	nCK	28)29)
Internal write to read command delay	t_{WTR}	7.5	—	ns	1)30)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	1)
Exit self-refresh to a non-read command	t_{XSNR}	t_{RFC} +10	—	ns	1)
Exit self-refresh to read command	t_{XSRD}	200	—	nCK	

Parameter	Symbol	DDR2–667		Unit	Note[1)2)3)4)5)6)7)8)]
		Min.	Max.		
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	nCK	
Exit power down to read command	t_{XARD}	2	—	nCK	
Exit active power-down mode to read command (slow exit, lower power)	t_{XARDS}	7 – AL	—	nCK	
CKE minimum pulse width (high and low pulse width)	t_{CKE}	3	—	nCK	31)
Mode register set command cycle time	t_{MRD}	2	—	nCK	
MRS command to ODT update delay	t_{MOD}	0	12	ns	1)
OCD drive mode output delay	t_{OIT}	0	12	ns	1)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{IS} + t_{CK.AVG} + t_{IH}$	—	ns	

1) For details and notes see the relevant Qimonda component data sheet
2) V_{DDQ} = 1.8 V ± 0.1V; V_{DD} = 1.8 V ± 0.1 V. See notes 5)6)7)8)
3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
5) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
7) The output timing reference voltage level is V_{TT}.
8) New units, '$t_{CK.AVG}$' and 'nCK', are introduced in DDR2–667 and DDR2–800. Unit '$t_{CK.AVG}$' represents the actual $t_{CK.AVG}$ of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2–400 and DDR2–533, 't_{CK}' is used for both concepts. Example: t_{XP} = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm + 2, even if (Tm + 2 - Tm) is 2 x $t_{CK.AVG}$ + $t_{ERR.2PER(Min)}$.
9) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{ERR(6-10per)}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{ERR(6-10PER).MIN}$ = – 272 ps and $t_{ERR(6-10PER).MAX}$ = + 293 ps, then $t_{DQSCK.MIN(DERATED)} = t_{DQSCK.MIN} - t_{ERR(6-10PER).MAX}$ = – 400 ps – 293 ps = – 693 ps and $t_{DQSCK.MAX(DERATED)} = t_{DQSCK.MAX} - t_{ERR(6-10PER).MIN}$ = 400 ps + 272 ps = + 672 ps. Similarly, $t_{LZ.DQ}$ for DDR2–667 derates to $t_{LZ.DQ.MIN(DERATED)}$ = - 900 ps – 293 ps = – 1193 ps and $t_{LZ.DQ.MAX(DERATED)}$ = 450 ps + 272 ps = + 722 ps. (Caution on the MIN/MAX usage!)
10) Input clock jitter spec parameter. These parameters are referred to as 'input clock jitter spec parameters' and these parameters apply to DDR2–667 and DDR2–800 only. The jitter specified is a random jitter meeting a Gaussian distribution.
11) These parameters are specified per their average values, however it is understood that the relationship between the average timing and the absolute instantaneous timing holds all the times (min. and max of SPEC values are to be used for calculations).
12) Input waveform timing t_{DS} with differential data strobe enabled MR[bit10] = 0, is referenced from the input signal crossing at the $V_{IH.AC}$ level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the $V_{IL.AC}$ level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{il(DC)MAX}$ and $V_{ih(DC)MIN}$. See **Figure 3**.
13) If t_{DS} or t_{DH} is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
14) These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS / $\overline{DQS}$) crossing.
15) Input waveform timing t_{DH} with differential data strobe enabled MR[bit10] = 0, is referenced from the differential data strobe crosspoint to the input signal crossing at the $V_{IH.DC}$ level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the $V_{IL.DC}$ level for a rising signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{IL.DC.MAX}$ and $V_{IH.DC.MIN}$. See **Figure 3**.
16) t_{HZ} and t_{LZ} transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (t_{HZ}), or begins driving (t_{LZ}) .
17) t_{DQSQ}: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS / $\overline{DQS}$ and associated DQ in any given cycle.

18) t_{HP} is the minimum of the absolute half period of the actual input clock. t_{HP} is an input parameter but not an input specification parameter. It is used in conjunction with t_{QHS} to derive the DRAM output timing t_{QH}. The value to be used for t_{QH} calculation is determined by the following equation; t_{HP} = MIN ($t_{CH.ABS}$, $t_{CL.ABS}$), where, $t_{CH.ABS}$ is the minimum of the actual instantaneous clock high time; $t_{CL.ABS}$ is the minimum of the actual instantaneous clock low time.
19) t_{QHS} accounts for: 1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual t_{HP} at the input is transferred to the output; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and pchannel to n-channel variation of the output drivers.
20) $t_{QH} = t_{HP} – t_{QHS}$, where: t_{HP} is the minimum of the absolute half period of the actual input clock; and t_{QHS} is the specification value under the max column. {The less half-pulse width distortion present, the larger the t_{QH} value is; and the larger the valid data eye will be.} Examples: 1) If the system provides t_{HP} of 1315 ps into a DDR2–667 SDRAM, the DRAM provides t_{QH} of 975 ps minimum. 2) If the system provides t_{HP} of 1420 ps into a DDR2–667 SDRAM, the DRAM provides t_{QH} of 1080 ps minimum.
21) These parameters are measured from a data strobe signal ((L/U/R)DQS / $\overline{\text{DQS}}$) crossing to its respective clock signal (CK / $\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$, etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
22) Input waveform timing is referenced from the input signal crossing at the $V_{IH.AC}$ level for a rising signal and $V_{IL.AC}$ for a falling signal applied to the device under test. See **Figure 4**.
23) These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK / $\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$, etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
24) Input waveform timing is referenced from the input signal crossing at the $V_{IL.DC}$ level for a rising signal and $V_{IH.DC}$ for a falling signal applied to the device under test. See **Figure 4**.
25) t_{RPST} end point and t_{RPRE} begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (t_{RPST}), or begins driving (t_{RPRE}). **Figure 2** shows a method to calculate these points when the device is no longer driving (t_{RPST}), or begins driving (t_{RPRE}) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.
26) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.PER}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.PER.MIN}$ = – 72 ps and $t_{JIT.PER.MAX}$ = + 93 ps, then $t_{RPRE.MIN(DERATED)} = t_{RPRE.MIN} + t_{JIT.PER.MIN}$ = 0.9 x $t_{CK.AVG}$ – 72 ps = + 2178 ps and $t_{RPRE.MAX(DERATED)} = t_{RPRE.MAX} + t_{JIT.PER.MAX}$ = 1.1 x $t_{CK.AVG}$ + 93 ps = + 2843 ps. (Caution on the MIN/MAX usage!).
27) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.DUTY}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.DUTY.MIN}$ = – 72 ps and $t_{JIT.DUTY.MAX}$ = + 93 ps, then $t_{RPST.MIN(DERATED)} = t_{RPST.MIN} + t_{JIT.DUTY.MIN}$ = 0.4 x $t_{CK.AVG}$ – 72 ps = + 928 ps and $t_{RPST.MAX(DERATED)} = t_{RPST.MAX} + t_{JIT.DUTY.MAX}$ = 0.6 x $t_{CK.AVG}$ + 93 ps = + 1592 ps. (Caution on the MIN/MAX usage!).
28) DAL = WR + RU{t_{RP}(ns) / t_{CK}(ns)}, where RU stands for round up. WR refers to the tWR parameter stored in the MRS. For t_{RP}, if the result of the division is not already an integer, round up to the next highest integer. t_{CK} refers to the application clock period. Example: For DDR2–533 at t_{CK} = 3.75 ns with t_{WR} programmed to 4 clocks. t_{DAL} = 4 + (15 ns / 3.75 ns) clocks = 4 + (4) clocks = 8 clocks.
29) $t_{DAL.nCK}$ = WR [nCK] + $t_{nRP.nCK}$ = WR + RU{t_{RP} [ps] / $t_{CK.AVG}$[ps] }, where WR is the value programmed in the EMR.
30) t_{WTR} is at lease two clocks (2 x t_{CK}) independent of operation frequency.
31) $t_{CKE.MIN}$ of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + 2 x t_{CK} + t_{IH}.

FIGURE 2

Method for calculating transitions and endpoint

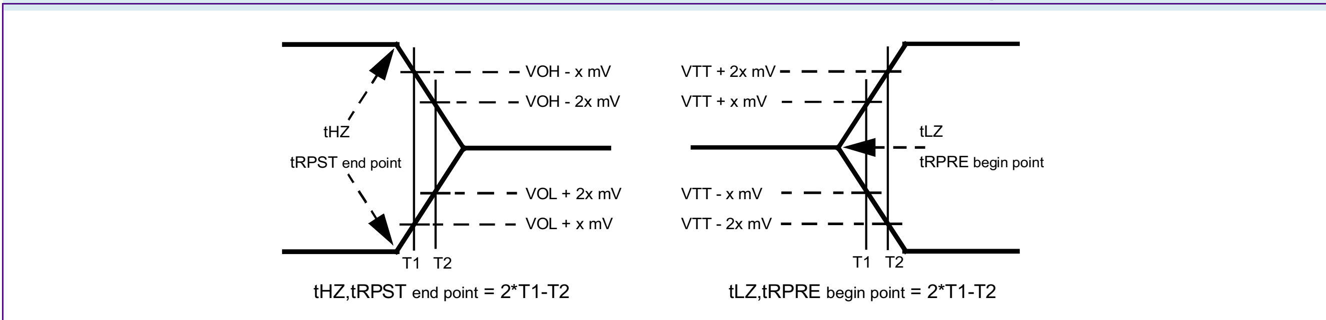

FIGURE 3

Differential input waveform timing - t_{DS} and t_{DS}

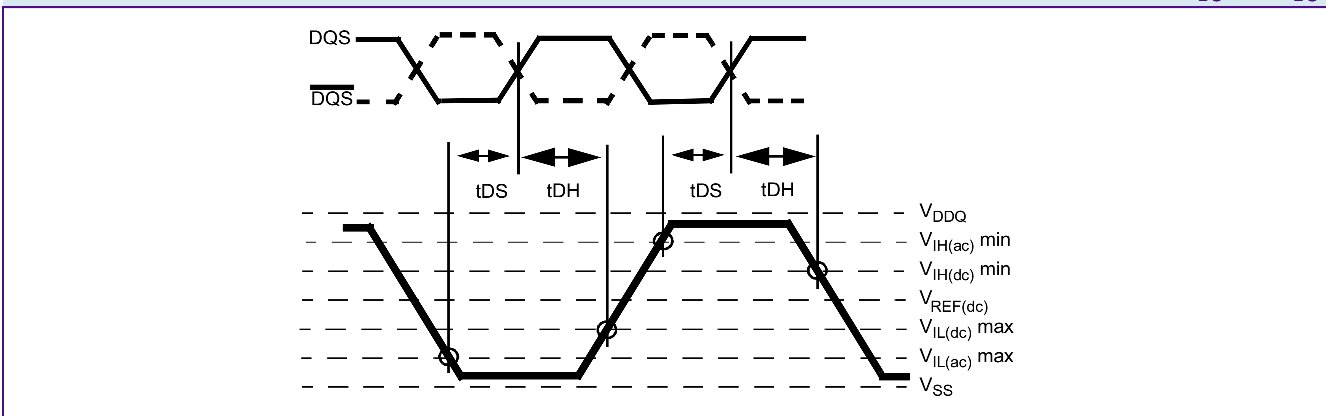

FIGURE 4

Differential input waveform timing - t_{IS} and t_{IH}

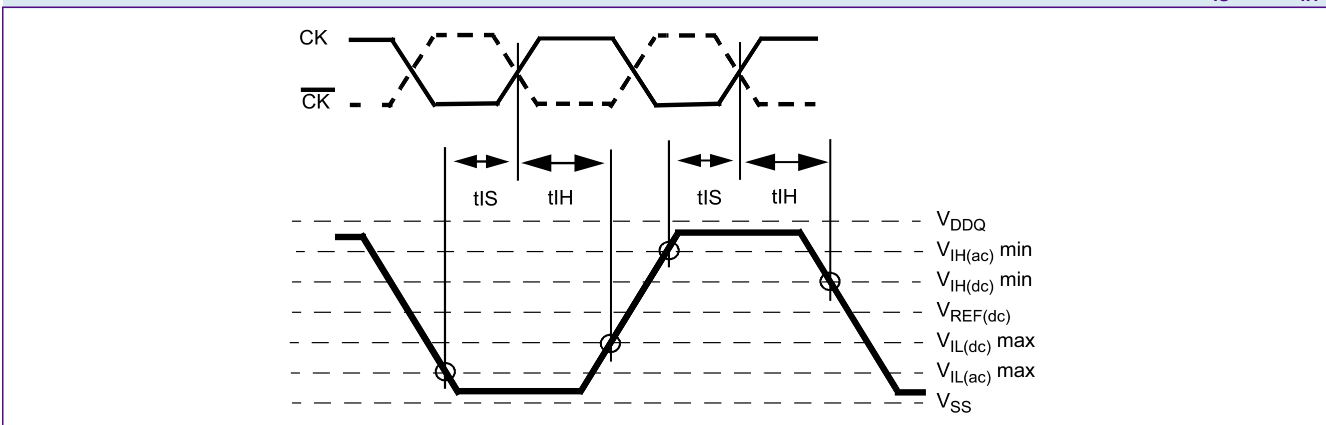

TABLE 18

DRAM Component Timing Parameter by Speed Grade - DDR2–533

Parameter	Symbol	DDR2–533		Unit	Note[1)2)3)4)5)6)7)]
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–500	+500	ps	
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	t_{CK}	
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	8)18)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$	—	ns	9)
DQ and DM input hold time (differential data strobe)	t_{DH}(base)	225	—	ps	10)
DQ and DM input hold time (single ended data strobe)	t_{DH1}(base)	–25	—	ps	11)
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–450	+450	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	300	ps	11)
Write command to 1st DQS latching transition	t_{DQSS}	– 0.25	+ 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	t_{DS}(base)	100	—	ps	11)
DQ and DM input setup time (single ended data strobe)	t_{DS1}(base)	–25	—	ps	11)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	
Clock half period	t_{HP}	MIN. ($t_{CL,}$ t_{CH})		—	12)
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	13)
Address and control input hold time	t_{IH}(base)	375	—	ps	11)
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	
Address and control input setup time	t_{IS}(base)	250	—	ps	11)
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	$2 \times t_{AC.MIN}$	$t_{AC.MAX}$	ps	14)
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	14)
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	ns	
Data output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—	—	
Data hold skew factor	t_{QHS}	—	400	ps	

Parameter	Symbol	DDR2–533		Unit	Note[1)2)3)4)5)6)7)]
		Min.	Max.		
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	14)15)
		—	3.9	µs	16)18)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	105	—	ns	17)
Precharge-All (4 banks) command period	t_{RP}	t_{RP} + 1t_{CK}	—	ns	
Precharge-All (8 banks) command period	t_{RP}	15 + 1t_{CK}	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	14)
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	14)
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	14)18)
		10	—	ns	16)20)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	
Write preamble	t_{WPRE}	0.25 x t_{CK}	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	19)
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}	—	t_{CK}	20)
Internal Write to Read command delay	t_{WTR}	7.5	—	ns	21)
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	22)
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	t_{CK}	22)
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	

1) For details and notes see the relevant Qimonda component data sheet
2) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ±0.1 V. See notes [5)6)7)8)]
3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) Timings are guaranteed with CK/$\overline{\text{CK}}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
5) The CK / $\overline{\text{CK}}$ input reference level (for timing reference to CK / $\overline{\text{CK}}$) is the point at which CK and $\overline{\text{CK}}$ cross. The DQS / $\overline{\text{DQS}}$, RDQS/ $\overline{\text{RDQS}}$, input reference level is the crosspoint when in differential strobe mode.
6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
7) The output timing reference voltage level is V_{TT}.
8) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MR.
9) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode.
10) For timing definition, refer to the Component data sheet.
11) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between DQS / $\overline{\text{DQS}}$ and associated DQ in any given cycle.
12) MIN (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).

13) The t_{HZ}, t_{RPST} and t_{LZ}, t_{RPRE} parameters are referenced to a specific voltage level, which specify when the device output is no longer driving (t_{HZ}, t_{RPST}), or begins driving (t_{LZ}, t_{RPRE}). t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions.These parameters are verified by design and characterization, but not subject to production test.
14) The Auto-Refresh command interval has be reduced to 3.9 µs when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
15) 0 °C≤ T_{CASE} ≤ 85 °C
16) 85 °C < T_{CASE} ≤ 95 °C
17) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
18) The t_{RRD} timing parameter depends on the page size of the DRAM organization. See **Table 2 "Ordering Information for RoHS Compliant Products" on Page 4**.
19) The maximum limit for the t_{WPST} parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
20) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where WR_{MIN}[cycles] = t_{WR}(ns)/t_{CK}(ns) rounded up to the next integer value. t_{DAL} = WR + (t_{RP}/t_{CK}). For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.
21) Minimum t_{WTR} is two clocks when operating the DDR2-SDRAM at frequencies ≤ 200 MHz.
22) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In "standard active power-down mode" (MR, A12 = "0") a fast power-down exit timing t_{XARD} can be used. In "low active power-down mode" (MR, A12 ="1") a slow power-down exit timing t_{XARDS} has to be satisfied.

TABLE 19
DRAM Component Timing Parameter by Speed Grade - DDR2-400

Parameter	Symbol	DDR2–400		Unit	Note[1)2)3)4)5)6)7)]
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–600	+600	ps	
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	t_{CK}	
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	8)22)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	t_{IS} + t_{CK} + t_{IH}	—	ns	9)
DQ and DM input hold time (differential data strobe)	t_{DH}(base)	275	—	ps	10)
DQ and DM input hold time (single ended data strobe)	t_{DH1}(base)	–25	—	ps	11)
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–500	+500	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	350	ps	11)
Write command to 1st DQS latching transition	t_{DQSS}	– 0.25	+ 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	t_{DS}(base)	150	—	ps	11)
DQ and DM input setup time (single ended data strobe)	t_{DS1}(base)	–25	—	ps	11)

Parameter	Symbol	DDR2–400		Unit	Note1)2)3)4)5)6)7)
		Min.	Max.		
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	
Clock half period	t_{HP}	MIN. ($t_{CL,}$ t_{CH})			12)
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	13)
Address and control input hold time	t_{IH}(base)	475	—	ps	11)
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	
Address and control input setup time	t_{IS}(base)	350	—	ps	11)
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	2 × $t_{AC.MIN}$	$t_{AC.MAX}$	ps	14)
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	14)
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	ns	
Data output hold time from DQS	t_{QH}	t_{HP} –t_{QHS}	—	—	
Data hold skew factor	t_{QHS}	—	450	ps	
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	14)15)
		—	3.9	µs	16)18)
Auto-Refresh to Active/Auto-Refresh command period		105	—	ns	17)
Precharge-All (4 banks) command period	t_{RP}	t_{RP} + 1t_{CK}	—	ns	
Precharge-All (8 banks) command period	t_{RP}	15 + 1t_{CK}	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	14)
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	14)
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	14)18)
		10	—	ns	16)20)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	
Write preamble	t_{WPRE}	0.25 x t_{CK}	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	19)
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}	—	t_{CK}	20)
Internal Write to Read command delay	t_{WTR}	10	—	ns	21)
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	22)
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	t_{CK}	22)
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	

1) For details and notes see the relevant Qimonda component data sheet
2) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ±0.1 V. See notes [5)6)7)8)]
3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
5) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS/ $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
7) The output timing reference voltage level is V_{TT}.
8) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MR.
9) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode.
10) For timing definition, refer to the Component data sheet.
11) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between DQS / $\overline{DQS}$ and associated DQ in any given cycle.
12) MIN (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).
13) The t_{HZ}, t_{RPST} and t_{LZ}, t_{RPRE} parameters are referenced to a specific voltage level, which specify when the device output is no longer driving (t_{HZ}, t_{RPST}), or begins driving (t_{LZ}, t_{RPRE}). t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions.These parameters are verified by design and characterization, but not subject to production test.
14) The Auto-Refresh command interval has be reduced to 3.9 µs when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
15) 0 °C≤ T_{CASE} ≤ 85 °C
16) 85 °C < T_{CASE} ≤ 95 °C
17) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
18) The t_{RRD} timing parameter depends on the page size of the DRAM organization. See **Table 2 "Ordering Information for RoHS Compliant Products" on Page 4**.
19) The maximum limit for the t_{WPST} parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
20) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where WR_{MIN}[cycles] = t_{WR}(ns)/t_{CK}(ns) rounded up to the next integer value. t_{DAL} = WR + (t_{RP}/t_{CK}). For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.
21) Minimum t_{WTR} is two clocks when operating the DDR2-SDRAM at frequencies ≤ 200 MHz.
22) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In "standard active power-down mode" (MR, A12 = "0") a fast power-down exit timing t_{XARD} can be used. In "low active power-down mode" (MR, A12 ="1") a slow power-down exit timing t_{XARDS} has to be satisfied.

3.3.3 ODT AC Electrical Characteristics

ODT AC Character. and Opeating Conditions: DDR2–667 &DDR2–800 [**Table 20**] and DDR2–533C & DDR2–400B [**Table 21**]

TABLE 20
ODT AC Character. and Operating Conditions for DDR2-667 & DDR2-800

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	nCK	1)
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.7 ns	ns	1)2)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	1)
t_{AOFD}	ODT turn-off delay	2.5	2.5	nCK	1)
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	1)3)

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 $t_{CK} + t_{AC.MAX}$ + 1 ns	ns	1)
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	nCK	1)
t_{AXPD}	ODT Power Down Exit Latency	8	—	nCK	1)

1) New units, '$t_{CK.AVG}$' and 'nCK', are introduced in DDR2-667 and DDR2-800. Unit '$t_{CK.AVG}$' represents the actual $t_{CK.AVG}$ of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2-400 and DDR2-533, 't_{CK}' is used for both concepts. Example: t_{XP} = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm + 2, even if (Tm + 2 - Tm) is 2 × $t_{CK.AVG}$+ $t_{EPR.2PER(MIN)}$.
2) ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from t_{AOND}, which is interpreted differently per speed bin. For DDR2-667/800, t_{AOND} is 2 clock cycles after the clock edge that registered a first ODT HIGH counting the actual input clock edges.
3) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}. Both are measured from t_{AOFD}, which is interpreted differently per speed bin. For DDR2-667/800,if $t_{CK.AVG}$ = 3 ns is assumed, t_{AOFD}= 1.5 ns (0.5 × 3 ns) after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edge.

TABLE 21
ODT AC Character. and Operating Conditions for DDR2-533 & DDR2-400

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 1 ns	ns	1)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 $t_{CK} + t_{AC.MAX}$ + 1 ns	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	2)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 $t_{CK} + t_{AC.MAX}$ + 1 ns	ns	
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}	
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}	

1) ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from t_{AOND}, which is interpreted differently per speed bin. For DDR2-400/533, t_{AOND} is 10 ns (= 2 x 5 ns) after the clock edge that registered a first ODT HIGH if t_{CK} = 5 ns.
2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}. Both are measured from t_{AOFD}, which is interpreted differently per speed bin. For DDR2-400/533, t_{AOFD} is 12.5 ns (= 2.5 x 5 ns) after the clock edge that registered a first ODT HIGH if t_{CK} = 5 ns.

3.4 I_{DD} Specifications and Conditions

List of tables defining I_{DD} Specifications and Conditions.

- **Table 22 "IDD Measurement Conditions" on Page 32**
- **Table 24 "IDD Specification for HYS64T[32/64/128]xxxHDL–[25F/2.5]–B" on Page 34**
- **Table 25 "IDD Specification for HYS64T[32/64/128]xxxHDL–[3/3S]–B" on Page 35**
- **Table 26 "IDD Specification for HYS64T[32/64/128]xxxHDL–[3.7/5]–B" on Page 36**

TABLE 22
I_{DD} Measurement Conditions

Parameter	Symbol	Note [1)2)3)4)5)]
Operating Current 0 One bank Active - Precharge; $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD0}	
Operating Current 1 One bank Active - Read - Precharge; I_{OUT} = 0 mA, BL = 4, $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, $t_{RCD} = t_{RCD.MIN}$, AL = 0, CL = CL_{MIN}; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD1}	6)
Precharge Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD2N}	
Precharge Power-Down Current Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2P}	
Precharge Quiet Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2Q}	
Active Standby Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD3N}	
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to LOW (Fast Power-down Exit);	$I_{DD3P(0)}$	
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to HIGH (Slow Power-down Exit);	$I_{DD3P(1)}$	
Operating Current - Burst Read All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CKMIN}$; $t_{RAS} = t_{RASMAX}$; $t_{RP} = t_{RPMIN}$; CKE is HIGH, CS is HIGH between valid commands; Address inputs are SWITCHING; Data bus inputs are SWITCHING; I_{OUT} = 0mA.	I_{DD4R}	6)
Operating Current - Burst Write All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MAX}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;	I_{DD4W}	
Burst Refresh Current $t_{CK} = t_{CK.MIN}$., Refresh command every $t_{RFC} = t_{RFC.MIN}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5B}	

Parameter	Symbol	Note 1)2)3)4)5)
Distributed Refresh Current $t_{CK} = t_{CK.MIN.}$, Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5D}	
Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. I_{DD6} current values are guaranteed up to T_{CASE} of 85 °C max.	I_{DD6}	
All Bank Interleave Read Current All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. I_{out} = 0 mA.	I_{DD7}	6)

1) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V
2) I_{DD} specifications are tested after the device is properly initialized and I_{DD} parameter are specified with ODT disabled.
3) Definitions for I_{DD} see **Table 23**
4) For two rank modules: for all active current measurements the other rank is in Precharge Power-Down Mode I_{DD2P}
5) For details and notes see the relevant Qimonda component data sheet
6) I_{DD1}, I_{DD4R} and I_{DD7} current measurements are defined with the outputs disabled (I_{OUT} = 0 mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.

TABLE 23
Definitions for I_{DD}

Parameter	Description
LOW	$V_{IN} \leq V_{IL(ac).MAX}$, HIGH is defined as $V_{IN} \geq V_{IH(ac).MIN}$
STABLE	Inputs are stable at a HIGH or LOW level
FLOATING	Inputs are $V_{REF} = V_{DDQ}$ /2
SWITCHING	Inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes

TABLE 24

I_{DD} Specification for HYS64T[32/64/128]xxxHDL–[25F/2.5]–B

Product Type	HYS64T32000HDL–25F–B	HYS64T64020HDL–25F–B	HYS64T128021HDL–25F–B	HYS64T32000HDL–2.5–B	HYS64T64020HDL–2.5–B	HYS64T128021HDL–2.5–B	Unit	Note[1]
Organization	256 MB	512 MB	1 GB	256 MB	512 MB	1 GB		
	1 Rank	2 Ranks	2 Ranks	1 Rank	2 Ranks	2 Ranks		
	×64	×64	×64	×64	×64	×64		
	–25F	–25F	–25F	–2.5	–2.5	–2.5		
Symbol	Max.	Max.	Max.	Max.	Max.	Max.		
I_{DD0}	420	448	728	400	428	696	mA	2)
I_{DD1}	480	508	856	460	488	820	mA	2)
I_{DD2P}	30	60	112	28	56	110	mA	3)
I_{DD2N}	205	410	820	200	408	820	mA	3)
I_{DD2Q}	180	360	720	180	360	720	mA	3)
$I_{DD3P(MRS=0)}$	160	312	624	156	310	620	mA	3)
$I_{DD3P(MRS=1)}$	40	72	144	40	70	140	mA	4)3)
I_{DD3N}	240	480	960	240	480	960	mA	5)3)
I_{DD4R}	720	750	1300	720	748	1300	mA	2)
I_{DD4W}	800	830	1300	800	828	1300	mA	2)
I_{DD5B}	580	610	1220	580	608	1220	mA	2)
I_{DD5D}	40	72	144	40	70	140	mA	3)6)
I_{DD6}	24	40	80	24	40	80	mA	3)6)
I_{DD7}	1060	1088	1416	1020	1048	1340	mA	2)

1) Calculated values from component data. ODT disabled. I_{DD1}, I_{DD4R}, and I_{DD7}, are defined with the outputs disabled.
2) The other rank is in I_{DD2P} Precharge Power-Down Current mode
3) Both ranks are in the same I_{DD} current mode
4) Fast: MRS(12)=0
5) Slow: MRS(12)=1
6) I_{DD5D} and I_{DD6} values are for 0°C ≤ T_{Case} ≤ 85°C

TABLE 25

I_{DD} Specification for HYS64T[32/64/128]xxxHDL–[3/3S]–B

Product Type	HYS64T32000HDL–3–B	HYS64T64020HDL–3–B	HYS64T128021HDL–3–B	HYS64T32000HDL–3S–B HYS64T32900HDL–3S–B	HYS64T64020HDL–3S–B HYS64T64920HDL–3S–B	HYS64T128021HDL–3S–B HYS64T128921HDL–3S–B	Unit	Note[1]
Organization	256 MB	512 MB	1 GB	256 MB	512 MB	1 GB		
	1 Rank	2 Ranks	2 Ranks	1 Rank	2 Ranks	2 Ranks		
	×64	×64	×64	×64	×64	×64		
	–3	–3	–3	–3S	–3S	–3S		
Symbol	Max.	Max.	Max.	Max.	Max.	Max.		
I_{DD0}	380	410	660	360	390	620	mA	2)
I_{DD1}	420	450	780	400	430	740	mA	2)
I_{DD2P}	30	60	110	30	60	110	mA	3)
I_{DD2N}	180	360	720	180	360	720	mA	3)
I_{DD2Q}	160	320	640	160	320	640	mA	3)
$I_{DD3P(MRS = 0)}$	130	260	530	130	260	530	mA	3)
$I_{DD3P(MRS = 1)}$	40	70	140	40	70	140	mA	4)3)
I_{DD3N}	200	400	800	200	400	800	mA	5)3)
I_{DD4R}	620	650	1100	620	650	1100	mA	2)
I_{DD4W}	680	710	1100	680	710	1100	mA	2)
I_{DD5B}	560	590	1180	560	590	1180	mA	2)
I_{DD5D}	40	70	140	40	70	140	mA	3)6)
I_{DD6}	20	40	80	20	40	80	mA	3)6)
I_{DD7}	1010	1040	1340	960	990	1270	mA	2)

1) Calculated values from component data. ODT disabled. I_{DD1}, I_{DD4R}, and I_{DD7}, are defined with the outputs disabled.
2) The other rank is in I_{DD2P} Precharge Power-Down Current mode
3) Both ranks are in the same I_{DD}current mode
4) Fast: MRS(12)=0
5) Slow: MRS(12)=1
6) I_{DD5D} and I_{DD6} values are for 0°C ≤ T_{Case} ≤ 85°C

TABLE 26
I_{DD} Specification for HYS64T[32/64/128]xxxHDL–[3.7/5]–B

Product Type	HYS64T32000HDL–3.7–B HYS64T32900HDL–3.7–B	HYS64T64020HDL–3.7–B HYS64T64920HDL–3.7–B	HYS64T128021HDL–3.7–B HYS64T128921HDL–3.7–B	HYS64T32000HDL–5–B	HYS64T64020HDL–5–B	HYS64T128021HDL–5–B	Unit	Note[1]
Organization	256 MB	512 MB	1 GB	256 MB	512 MB	1 GB		
	1 Rank	2 Ranks	2 Ranks	1 Rank	2 Ranks	2 Ranks		
	×64	×64	×64	×64	×64	×64		
	–3.7	–3.7	–3.7	–5	–5	–5		
Symbol	Max.	Max.	Max.	Max.	Max.	Max.		
I_{DD0}	320	350	580	300	330	540	mA	2)
I_{DD1}	360	390	660	330	360	620	mA	2)
I_{DD2P}	30	60	110	30	60	110	mA	3)
I_{DD2N}	150	300	610	140	270	540	mA	3)
I_{DD2Q}	140	280	560	130	260	510	mA	3)
$I_{DD3P(MRS = 0)}$	110	220	450	100	190	380	mA	3)
$I_{DD3P(MRS = 1)}$	40	70	140	40	70	140	mA	4)3)
I_{DD3N}	170	340	690	160	310	620	mA	5)3)
I_{DD4R}	520	550	940	460	490	820	mA	2)
I_{DD4W}	580	610	940	520	550	820	mA	2)
I_{DD5B}	520	550	1100	500	530	1060	mA	2)
I_{DD5D}	40	70	140	40	70	140	mA	3)6)
I_{DD6}	20	40	80	20	40	80	mA	3)6)
I_{DD7}	920	950	1220	880	910	1180	mA	2)

1) Calculated values from component data. ODT disabled. I_{DD1}, I_{DD4R}, and I_{DD7}, are defined with the outputs disabled.
2) The other rank is in I_{DD2P} Precharge Power-Down Current mode
3) Both ranks are in the same I_{DD} current mode
4) Fast: MRS(12)=0
5) Slow: MRS(12)=1
6) I_{DD5D} and I_{DD6} values are for 0°C ≤ T_{Case} ≤ 85°C

4 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

List of SPD Code Tables

- **Table 27 "SPD codes for PC2–6400 5–5–5" on Page 37**
- **Table 28 "SPD codes for PC2–6400 6–6–6" on Page 42**
- **Table 29 "SPD codes for PC2–5300 4–4–4" on Page 46**
- **Table 30 "SPD codes for PC2–5300 5–5–5" on Page 50**
- **Table 31 "SPD codes for PC2–4200 4–4–4" on Page 55**
- **Table 32 "SPD codes for PC2–5300 4–4–4" on Page 60**

TABLE 27
SPD codes for PC2–6400 5–5–5

Product Type		**HYS64T32000HDL–25F–B**	**HYS64T64020HDL–25F–B**	**HYS64T128021HDL–25F–B**
Organization		**256MB**	**512MB**	**1 GByte**
		×64	**×64**	**×64**
		1 Rank (×16)	**2 Ranks (×16)**	**2 Ranks (×8)**
Label Code		**PC2–6400S–555**	**PC2–6400S–555**	**PC2–6400S–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0D	0D	0E
4	Number of Column Addresses	0A	0A	0A
5	DIMM Rank and Stacking Information	60	61	61
6	Data Width	40	40	40
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	25	25	25
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	40	40	40

Product Type		HYS64T32000HDL–25F–B	HYS64T64020HDL–25F–B	HYS64T128021HDL–25F–B
Organization		256MB	512MB	1 GByte
		×64	×64	×64
		1 Rank (×16)	2 Ranks (×16)	2 Ranks (×8)
Label Code		PC2–6400S–555	PC2–6400S–555	PC2–6400S–555
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX
11	Error Correction Support (non-ECC, ECC)	00	00	00
12	Refresh Rate and Type	82	82	82
13	Primary SDRAM Width	10	10	08
14	Error Checking SDRAM Width	00	00	00
15	Not used	00	00	00
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04
18	Supported CAS Latencies	70	70	70
19	DIMM Mechanical Characteristics	01	01	01
20	DIMM Type Information	04	04	04
21	DIMM Attributes	00	00	00
22	Component Attributes	07	07	07
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	25	25	25
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	40	40	40
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	3D	3D	3D
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	50	50	50
27	$t_{RP.MIN}$ [ns]	32	32	32
28	$t_{RRD.MIN}$ [ns]	28	28	1E
29	$t_{RCD.MIN}$ [ns]	32	32	32
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D
31	Module Density per Rank	40	40	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	17	17	17
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	25	25	25
34	$t_{DS.MIN}$ [ns]	05	05	05
35	$t_{DH.MIN}$ [ns]	12	12	12
36	$t_{WR.MIN}$ [ns]	3C	3C	3C

Product Type		**HYS64T32000HDL–25F–B**	**HYS64T64020HDL–25F–B**	**HYS64T128021HDL–25F–B**
Organization		**256MB**	**512MB**	**1 GByte**
		×64	**×64**	**×64**
		1 Rank (×16)	**2 Ranks (×16)**	**2 Ranks (×8)**
Label Code		**PC2–6400S–555**	**PC2–6400S–555**	**PC2–6400S–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E
39	Analysis Characteristics	00	00	00
40	t_{RC} and t_{RFC} Extension	30	30	30
41	$t_{RC.MIN}$ [ns]	39	39	39
42	$t_{RFC.MIN}$ [ns]	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	14	14	14
45	$t_{QHS.MAX}$ [ns]	1E	1E	1E
46	PLL Relock Time	00	00	00
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	56	56	50
48	Psi(T-A) DRAM	7A	7A	7A
49	ΔT_0 (DT0)	7F	7F	5F
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	3B	3B	3B
51	ΔT_{2P} (DT2P)	36	36	36
52	ΔT_{3N} (DT3N)	2E	2E	2E
53	$\Delta T_{3P.fast}$ (DT3P fast)	5A	5A	5A
54	$\Delta T_{3P.slow}$ (DT3P slow)	2A	2A	2A
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	68	68	5A
56	ΔT_{5B} (DT5B)	22	22	22
57	ΔT_7 (DT7)	3D	3D	27
58	Psi(ca) PLL	00	00	00
59	Psi(ca) REG	00	00	00
60	ΔT_{PLL} (DTPLL)	00	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00
62	SPD Revision	12	12	12

Product Type		**HYS64T32000HDL–25F–B**	**HYS64T64020HDL–25F–B**	**HYS64T128021HDL–25F–B**
Organization		**256MB**	**512MB**	**1 GByte**
		×64	**×64**	**×64**
		1 Rank (×16)	**2 Ranks (×16)**	**2 Ranks (×8)**
Label Code		**PC2–6400S–555**	**PC2–6400S–555**	**PC2–6400S–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
63	Checksum of Bytes 0-62	54	55	3A
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F
66	Manufacturer’s JEDEC ID Code (3)	7F	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	36	36	36
74	Product Type, Char 2	34	34	34
75	Product Type, Char 3	54	54	54
76	Product Type, Char 4	33	36	31
77	Product Type, Char 5	32	34	32
78	Product Type, Char 6	30	30	38
79	Product Type, Char 7	30	32	30
80	Product Type, Char 8	30	30	32
81	Product Type, Char 9	48	48	31
82	Product Type, Char 10	44	44	48
83	Product Type, Char 11	4C	4C	44
84	Product Type, Char 12	32	32	4C
85	Product Type, Char 13	35	35	32
86	Product Type, Char 14	46	46	35
87	Product Type, Char 15	42	42	46
88	Product Type, Char 16	20	20	42

Product Type		HYS64T32000HDL–25F–B	HYS64T64020HDL–25F–B	HYS64T128021HDL–25F–B
Organization		**256MB**	**512MB**	**1 GByte**
		×64	**×64**	**×64**
		1 Rank (×16)	**2 Ranks (×16)**	**2 Ranks (×8)**
Label Code		**PC2–6400S–555**	**PC2–6400S–555**	**PC2–6400S–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
89	Product Type, Char 17	20	20	20
90	Product Type, Char 18	20	20	20
91	Module Revision Code	3x	3x	3x
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx
99 - 127	Not used	00	00	00
128 - 255	Blank for customer use	FF	FF	FF

TABLE 28
SPD codes for PC2–6400 6–6–6

Product Type		HYS64T32000HDL–2.5–B	HYS64T64020HDL–2.5–B	HYS64T128021HDL–2.5–B
Organization		**256MB**	**512MB**	**1 GByte**
		×64	**×64**	**×64**
		1 Rank (×16)	**2 Ranks (×16)**	**2 Ranks (×8)**
Label Code		**PC2–6400S–666**	**PC2–6400S–666**	**PC2–6400S–666**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0D	0D	0E
4	Number of Column Addresses	0A	0A	0A
5	DIMM Rank and Stacking Information	60	61	61
6	Data Width	40	40	40
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	25	25	25
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	40	40	40
11	Error Correction Support (non-ECC, ECC)	00	00	00
12	Refresh Rate and Type	82	82	82
13	Primary SDRAM Width	10	10	08
14	Error Checking SDRAM Width	00	00	00
15	Not used	00	00	00
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04
18	Supported CAS Latencies	70	70	70
19	DIMM Mechanical Characteristics	01	01	01
20	DIMM Type Information	04	04	04
21	DIMM Attributes	00	00	00
22	Component Attributes	07	07	07

Product Type		HYS64T32000HDL–2.5–B	HYS64T64020HDL–2.5–B	HYS64T128021HDL–2.5–B
Organization		**256MB**	**512MB**	**1 GByte**
		×64	**×64**	**×64**
		1 Rank (×16)	**2 Ranks (×16)**	**2 Ranks (×8)**
Label Code		**PC2–6400S–666**	**PC2–6400S–666**	**PC2–6400S–666**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	30	30	30
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	45	45	45
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	3D	3D	3D
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	50	50	50
27	$t_{RP.MIN}$ [ns]	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	28	28	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D
31	Module Density per Rank	40	40	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	17	17	17
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	25	25	25
34	$t_{DS.MIN}$ [ns]	05	05	05
35	$t_{DH.MIN}$ [ns]	12	12	12
36	$t_{WR.MIN}$ [ns]	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E
39	Analysis Characteristics	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C	3C
42	$t_{RFC.MIN}$ [ns]	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	14	14	14
45	$t_{QHS.MAX}$ [ns]	1E	1E	1E
46	PLL Relock Time	00	00	00
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	55	55	50
48	Psi(T-A) DRAM	72	72	7A

Product Type		**HYS64T32000HDL–2.5–B**	**HYS64T64020HDL–2.5–B**	**HYS64T128021HDL–2.5–B**
Organization		**256MB**	**512MB**	**1 GByte**
		×64	**×64**	**×64**
		1 Rank (×16)	**2 Ranks (×16)**	**2 Ranks (×8)**
Label Code		**PC2–6400S–666**	**PC2–6400S–666**	**PC2–6400S–666**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
49	ΔT_0 (DT0)	6F	6F	5B
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	37	37	3B
51	ΔT_{2P} (DT2P)	33	33	36
52	ΔT_{3N} (DT3N)	2B	2B	2E
53	$\Delta T_{3P.fast}$ (DT3P fast)	54	54	5A
54	$\Delta T_{3P.slow}$ (DT3P slow)	27	27	2A
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	62	62	5A
56	ΔT_{5B} (DT5B)	1F	1F	22
57	ΔT_7 (DT7)	37	37	25
58	Psi(ca) PLL	00	00	00
59	Psi(ca) REG	00	00	00
60	ΔT_{PLL} (DTPLL)	00	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00
62	SPD Revision	12	12	12
63	Checksum of Bytes 0-62	10	11	2B
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F
66	Manufacturer’s JEDEC ID Code (3)	7F	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	36	36	36
74	Product Type, Char 2	34	34	34

Product Type		**HYS64T32000HDL–2.5–B**	**HYS64T64020HDL–2.5–B**	**HYS64T128021HDL–2.5–B**
Organization		**256MB**	**512MB**	**1 GByte**
		×64	**×64**	**×64**
		1 Rank (×16)	**2 Ranks (×16)**	**2 Ranks (×8)**
Label Code		**PC2–6400S–666**	**PC2–6400S–666**	**PC2–6400S–666**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
75	Product Type, Char 3	54	54	54
76	Product Type, Char 4	33	36	31
77	Product Type, Char 5	32	34	32
78	Product Type, Char 6	30	30	38
79	Product Type, Char 7	30	32	30
80	Product Type, Char 8	30	30	32
81	Product Type, Char 9	48	48	31
82	Product Type, Char 10	44	44	48
83	Product Type, Char 11	4C	4C	44
84	Product Type, Char 12	32	32	4C
85	Product Type, Char 13	2E	2E	32
86	Product Type, Char 14	35	35	2E
87	Product Type, Char 15	42	42	35
88	Product Type, Char 16	20	20	42
89	Product Type, Char 17	20	20	20
90	Product Type, Char 18	20	20	20
91	Module Revision Code	4x	4x	4x
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx
99 - 127	Not used	00	00	00
128 - 255	Blank for customer use	FF	FF	FF

TABLE 29
SPD codes for PC2–5300 4–4–4

Product Type		HYS64T32000HDL–3–B	HYS64T64020HDL–3–B	HYS64T128021HDL–3–B
Organization		**256MB**	**512MB**	**1 GByte**
		×64	**×64**	**×64**
		1 Rank (×16)	**2 Ranks (×16)**	**2 Ranks (×8)**
Label Code		**PC2–5300S–444**	**PC2–5300S–444**	**PC2–5300S–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0D	0D	0E
4	Number of Column Addresses	0A	0A	0A
5	DIMM Rank and Stacking Information	60	61	61
6	Data Width	40	40	40
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	30	30	30
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	45	45	45
11	Error Correction Support (non-ECC, ECC)	00	00	00
12	Refresh Rate and Type	82	82	82
13	Primary SDRAM Width	10	10	08
14	Error Checking SDRAM Width	00	00	00
15	Not used	00	00	00
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04
18	Supported CAS Latencies	38	38	38
19	DIMM Mechanical Characteristics	01	01	01
20	DIMM Type Information	04	04	04
21	DIMM Attributes	00	00	00
22	Component Attributes	07	07	07
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	30	30	30

Product Type		**HYS64T32000HDL–3–B**	**HYS64T64020HDL–3–B**	**HYS64T128021HDL–3–B**
Organization		**256MB**	**512MB**	**1 GByte**
		×64	**×64**	**×64**
		1 Rank (×16)	**2 Ranks (×16)**	**2 Ranks (×8)**
Label Code		**PC2–5300S–444**	**PC2–5300S–444**	**PC2–5300S–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	45	45	45
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60
27	$t_{RP.MIN}$ [ns]	30	30	30
28	$t_{RRD.MIN}$ [ns]	28	28	1E
29	$t_{RCD.MIN}$ [ns]	30	30	30
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D
31	Module Density per Rank	40	40	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	20	20	20
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	27	27	27
34	$t_{DS.MIN}$ [ns]	10	10	10
35	$t_{DH.MIN}$ [ns]	17	17	17
36	$t_{WR.MIN}$ [ns]	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E
39	Analysis Characteristics	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00
41	$t_{RC.MIN}$ [ns]	39	39	39
42	$t_{RFC.MIN}$ [ns]	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	18	18	18
45	$t_{QHS.MAX}$ [ns]	22	22	22
46	PLL Relock Time	00	00	00
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	54	54	50
48	Psi(T-A) DRAM	72	72	7A
49	ΔT_0 (DT0)	67	67	53

Product Type		**HYS64T32000HDL–3–B**	**HYS64T64020HDL–3–B**	**HYS64T128021HDL–3–B**
Organization		**256MB**	**512MB**	**1 GByte**
		×64	**×64**	**×64**
		1 Rank (×16)	**2 Ranks (×16)**	**2 Ranks (×8)**
Label Code		**PC2–5300S–444**	**PC2–5300S–444**	**PC2–5300S–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	31	31	34
51	ΔT_{2P} (DT2P)	33	33	36
52	ΔT_{3N} (DT3N)	24	24	27
53	$\Delta T_{3P.fast}$ (DT3P fast)	47	47	4C
54	$\Delta T_{3P.slow}$ (DT3P slow)	27	27	2A
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	54	54	4C
56	ΔT_{5B} (DT5B)	1E	1E	20
57	ΔT_{7} (DT7)	37	37	25
58	Psi(ca) PLL	00	00	00
59	Psi(ca) REG	00	00	00
60	ΔT_{PLL} (DTPLL)	00	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00
62	SPD Revision	12	12	12
63	Checksum of Bytes 0-62	E1	E2	FA
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F
66	Manufacturer’s JEDEC ID Code (3)	7F	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	36	36	36
74	Product Type, Char 2	34	34	34
75	Product Type, Char 3	54	54	54

Product Type		**HYS64T32000HDL–3–B**	**HYS64T64020HDL–3–B**	**HYS64T128021HDL–3–B**
Organization		**256MB**	**512MB**	**1 GByte**
		×64	**×64**	**×64**
		1 Rank (×16)	**2 Ranks (×16)**	**2 Ranks (×8)**
Label Code		**PC2–5300S–444**	**PC2–5300S–444**	**PC2–5300S–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
76	Product Type, Char 4	33	36	31
77	Product Type, Char 5	32	34	32
78	Product Type, Char 6	30	30	38
79	Product Type, Char 7	30	32	30
80	Product Type, Char 8	30	30	32
81	Product Type, Char 9	48	48	31
82	Product Type, Char 10	44	44	48
83	Product Type, Char 11	4C	4C	44
84	Product Type, Char 12	33	33	4C
85	Product Type, Char 13	42	42	33
86	Product Type, Char 14	20	20	42
87	Product Type, Char 15	20	20	20
88	Product Type, Char 16	20	20	20
89	Product Type, Char 17	20	20	20
90	Product Type, Char 18	20	20	20
91	Module Revision Code	3x	3x	4x
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx
99 - 127	Not used	00	00	00
128 - 255	Blank for customer use	FF	FF	FF

TABLE 30
SPD codes for PC2–5300 5–5–5

Product Type		HYS64T32000HDL–3S–B	HYS64T32900HDL–3S–B	HYS64T64020HDL–3S–B	HYS64T64920HDL–3S–B	HYS64T128021HDL–3S–B	HYS64T128921HDL–3S–B
Organization		**256MB**	**256MB**	**512MB**	**512MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×64**	**×64**	**×64**	**×64**
		1 Rank (×16)	**1 Rank (×16)**	**2 Ranks (×16)**	**2 Ranks (×16)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–5300S–555**	**PC2–5300S–555**	**PC2–5300S–555**	**PC2–5300S–555**	**PC2–5300S–555**	**PC2–5300S–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08	08	08
3	Number of Row Addresses	0D	0D	0D	0D	0E	0E
4	Number of Column Addresses	0A	0A	0A	0A	0A	0A
5	DIMM Rank and Stacking Information	60	60	61	61	61	61
6	Data Width	40	40	40	40	40	40
7	Not used	00	00	00	00	00	00
8	Interface Voltage Level	05	05	05	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	30	30	30	30	30	30
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	45	45	45	45	45	45
11	Error Correction Support (non-ECC, ECC)	00	00	00	00	00	00
12	Refresh Rate and Type	82	82	82	82	82	82
13	Primary SDRAM Width	10	10	10	10	08	08
14	Error Checking SDRAM Width	00	00	00	00	00	00
15	Not used	00	00	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04	04	04
18	Supported CAS Latencies	38	38	38	38	38	38
19	DIMM Mechanical Characteristics	01	01	01	01	01	01

Product Type		HYS64T32000HDL–3S–B	HYS64T32900HDL–3S–B	HYS64T64020HDL–3S–B	HYS64T64920HDL–3S–B	HYS64T128021HDL–3S–B	HYS64T128921HDL–3S–B
Organization		**256MB**	**256MB**	**512MB**	**512MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×64**	**×64**	**×64**	**×64**
		1 Rank (×16)	**1 Rank (×16)**	**2 Ranks (×16)**	**2 Ranks (×16)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–5300S–555**	**PC2–5300S–555**	**PC2–5300S–555**	**PC2–5300S–555**	**PC2–5300S–555**	**PC2–5300S–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
20	DIMM Type Information	04	04	04	04	04	04
21	DIMM Attributes	00	00	00	00	00	00
22	Component Attributes	07	07	07	07	07	07
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	3D	3D	3D	3D	3D	3D
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	50	50	50	50	50	50
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	28	28	28	28	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D	2D	2D	2D
31	Module Density per Rank	40	40	40	40	80	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	20	20	20	20	20	20
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	27	27	27	27	27	27
34	$t_{DS.MIN}$ [ns]	10	10	10	10	10	10
35	$t_{DH.MIN}$ [ns]	17	17	17	17	17	17
36	$t_{WR.MIN}$ [ns]	3C	3C	3C	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00	00	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C	3C	3C	3C	3C
42	$t_{RFC.MIN}$ [ns]	69	69	69	69	69	69

Product Type		**HYS64T32000HDL–3S–B**	**HYS64T32900HDL–3S–B**	**HYS64T64020HDL–3S–B**	**HYS64T64920HDL–3S–B**	**HYS64T128021HDL–3S–B**	**HYS64T128921HDL–3S–B**
Organization		**256MB**	**256MB**	**512MB**	**512MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×64**	**×64**	**×64**	**×64**
		1 Rank (×16)	**1 Rank (×16)**	**2 Ranks (×16)**	**2 Ranks (×16)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–5300S–555**	**PC2–5300S–555**	**PC2–5300S–555**	**PC2–5300S–555**	**PC2–5300S–555**	**PC2–5300S–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
43	$t_{CK.MAX}$ [ns]	80	80	80	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	18	18	18	18	18	18
45	$t_{QHS.MAX}$ [ns]	22	22	22	22	22	22
46	PLL Relock Time	00	00	00	00	00	00
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	54	54	54	54	50	50
48	Psi(T-A) DRAM	72	72	72	72	7A	7A
49	ΔT_0 (DT0)	5F	5F	5F	5F	4B	4B
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	31	31	31	31	34	34
51	ΔT_{2P} (DT2P)	33	33	33	33	36	36
52	ΔT_{3N} (DT3N)	24	24	24	24	27	27
53	$\Delta T_{3P.fast}$ (DT3P fast)	47	47	47	47	4C	4C
54	$\Delta T_{3P.slow}$ (DT3P slow)	27	27	27	27	2A	2A
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	54	54	54	54	4C	4C
56	ΔT_{5B} (DT5B)	1E	1E	1E	1E	20	20
57	ΔT_7 (DT7)	34	34	34	34	23	23
58	Psi(ca) PLL	00	00	00	00	00	00
59	Psi(ca) REG	00	00	00	00	00	00
60	ΔT_{PLL} (DTPLL)	00	00	00	00	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00	00	00	00
62	SPD Revision	12	12	12	12	12	12
63	Checksum of Bytes 0-62	09	09	0A	0A	23	23
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F	7F	7F	7F

Product Type		HYS64T32000HDL–3S–B	HYS64T32900HDL–3S–B	HYS64T64020HDL–3S–B	HYS64T64920HDL–3S–B	HYS64T128021HDL–3S–B	HYS64T128921HDL–3S–B
Organization		**256MB**	**256MB**	**512MB**	**512MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×64**	**×64**	**×64**	**×64**
		1 Rank (×16)	**1 Rank (×16)**	**2 Ranks (×16)**	**2 Ranks (×16)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–5300S–555**	**PC2–5300S–555**	**PC2–5300S–555**	**PC2–5300S–555**	**PC2–5300S–555**	**PC2–5300S–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
66	Manufacturer’s JEDEC ID Code (3)	7F	7F	7F	7F	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F	7F	7F	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F	7F	7F	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51	51	51	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00	00	00	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx	xx	xx
73	Product Type, Char 1	36	36	36	36	36	36
74	Product Type, Char 2	34	34	34	34	34	34
75	Product Type, Char 3	54	54	54	54	54	54
76	Product Type, Char 4	33	33	36	36	31	31
77	Product Type, Char 5	32	32	34	34	32	32
78	Product Type, Char 6	30	39	30	39	38	38
79	Product Type, Char 7	30	30	32	32	30	39
80	Product Type, Char 8	30	30	30	30	32	32
81	Product Type, Char 9	48	48	48	48	31	31
82	Product Type, Char 10	44	44	44	44	48	48
83	Product Type, Char 11	4C	4C	4C	4C	44	44
84	Product Type, Char 12	33	33	33	33	4C	4C
85	Product Type, Char 13	53	53	53	53	33	33
86	Product Type, Char 14	42	42	42	42	53	53
87	Product Type, Char 15	20	20	20	20	42	42
88	Product Type, Char 16	20	20	20	20	20	20

Product Type		**HYS64T32000HDL–3S–B**	**HYS64T32900HDL–3S–B**	**HYS64T64020HDL–3S–B**	**HYS64T64920HDL–3S–B**	**HYS64T128021HDL–3S–B**	**HYS64T128921HDL–3S–B**
Organization		**256MB**	**256MB**	**512MB**	**512MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×64**	**×64**	**×64**	**×64**
		1 Rank (×16)	**1 Rank (×16)**	**2 Ranks (×16)**	**2 Ranks (×16)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–5300S–555**	**PC2–5300S–555**	**PC2–5300S–555**	**PC2–5300S–555**	**PC2–5300S–555**	**PC2–5300S–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
89	Product Type, Char 17	20	20	20	20	20	20
90	Product Type, Char 18	20	20	20	20	20	20
91	Module Revision Code	4x	2x	4x	2x	4x	2x
92	Test Program Revision Code	xx	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00	00	00
128 - 255	Blank for customer use	FF	FF	FF	FF	FF	FF

TABLE 31
SPD codes for PC2–4200 4–4–4

Product Type		HYS64T32000HDL–3.7–B	HYS64T32900HDL–3.7–B	HYS64T64020HDL–3.7–B	HYS64T64920HDL–3.7–B	HYS64T128021HDL–3.7–B	HYS64T128921HDL–3.7–B
Organization		256MB	256MB	512MB	512MB	1 GByte	1 GByte
		×64	×64	×64	×64	×64	×64
		1 Rank (×16)	1 Rank (×16)	2 Ranks (×16)	2 Ranks (×16)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2–4200S–444	PC2–4200S–444	PC2–4200S–444	PC2–4200S–444	PC2–4200S–444	PC2–4200S–444
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08	08	08
3	Number of Row Addresses	0D	0D	0D	0D	0E	0E
4	Number of Column Addresses	0A	0A	0A	0A	0A	0A
5	DIMM Rank and Stacking Information	60	60	61	61	61	61
6	Data Width	40	40	40	40	40	40
7	Not used	00	00	00	00	00	00
8	Interface Voltage Level	05	05	05	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	3D	3D	3D	3D	3D	3D
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	50	50	50	50	50	50
11	Error Correction Support (non-ECC, ECC)	00	00	00	00	00	00
12	Refresh Rate and Type	82	82	82	82	82	82
13	Primary SDRAM Width	10	10	10	10	08	08
14	Error Checking SDRAM Width	00	00	00	00	00	00
15	Not used	00	00	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04	04	04
18	Supported CAS Latencies	38	38	38	38	38	38
19	DIMM Mechanical Characteristics	01	01	01	01	01	01

Product Type		HYS64T32000HDL–3.7–B	HYS64T32900HDL–3.7–B	HYS64T64020HDL–3.7–B	HYS64T64920HDL–3.7–B	HYS64T128021HDL–3.7–B	HYS64T128921HDL–3.7–B
Organization		**256MB**	**256MB**	**512MB**	**512MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×64**	**×64**	**×64**	**×64**
		1 Rank (×16)	**1 Rank (×16)**	**2 Ranks (×16)**	**2 Ranks (×16)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
20	DIMM Type Information	04	04	04	04	04	04
21	DIMM Attributes	00	00	00	00	00	00
22	Component Attributes	07	07	07	07	07	07
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	3D	3D	3D	3D	3D	3D
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	50	50	50	50	50	50
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	28	28	28	28	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D	2D	2D	2D
31	Module Density per Rank	40	40	40	40	80	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	25	25	25	25	25	25
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	37	37	37	37	37	37
34	$t_{DS.MIN}$ [ns]	10	10	10	10	10	10
35	$t_{DH.MIN}$ [ns]	22	22	22	22	22	22
36	$t_{WR.MIN}$ [ns]	3C	3C	3C	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00	00	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C	3C	3C	3C	3C
42	$t_{RFC.MIN}$ [ns]	69	69	69	69	69	69

Product Type		**HYS64T32000HDL–3.7–B**	**HYS64T32900HDL–3.7–B**	**HYS64T64020HDL–3.7–B**	**HYS64T64920HDL–3.7–B**	**HYS64T128021HDL–3.7–B**	**HYS64T128921HDL–3.7–B**
Organization		**256MB**	**256MB**	**512MB**	**512MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×64**	**×64**	**×64**	**×64**
		1 Rank (×16)	**1 Rank (×16)**	**2 Ranks (×16)**	**2 Ranks (×16)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
43	$t_{CK.MAX}$ [ns]	80	80	80	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	1E	1E	1E	1E	1E	1E
45	$t_{QHS.MAX}$ [ns]	28	28	28	28	28	28
46	PLL Relock Time	00	00	00	00	00	00
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	54	54	54	54	50	50
48	Psi(T-A) DRAM	72	72	72	72	7A	7A
49	ΔT_0 (DT0)	53	53	53	53	43	43
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	29	29	29	29	2C	2C
51	ΔT_{2P} (DT2P)	33	33	33	33	36	36
52	ΔT_{3N} (DT3N)	1F	1F	1F	1F	21	21
53	$\Delta T_{3P.fast}$ (DT3P fast)	3D	3D	3D	3D	41	41
54	$\Delta T_{3P.slow}$ (DT3P slow)	27	27	27	27	2A	2A
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	46	46	46	46	40	40
56	ΔT_{5B} (DT5B)	1C	1C	1C	1C	1E	1E
57	ΔT_7 (DT7)	32	32	32	32	22	22
58	Psi(ca) PLL	00	00	00	00	00	00
59	Psi(ca) REG	00	00	00	00	00	00
60	ΔT_{PLL} (DTPLL)	00	00	00	00	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00	00	00	00
62	SPD Revision	12	12	12	12	12	12
63	Checksum of Bytes 0-62	18	18	19	19	37	37
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F	7F	7F	7F

Product Type		HYS64T32000HDL–3.7–B	HYS64T32900HDL–3.7–B	HYS64T64020HDL–3.7–B	HYS64T64920HDL–3.7–B	HYS64T128021HDL–3.7–B	HYS64T128921HDL–3.7–B
Organization		**256MB**	**256MB**	**512MB**	**512MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×64**	**×64**	**×64**	**×64**
		1 Rank (×16)	**1 Rank (×16)**	**2 Ranks (×16)**	**2 Ranks (×16)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
66	Manufacturer's JEDEC ID Code (3)	7F	7F	7F	7F	7F	7F
67	Manufacturer's JEDEC ID Code (4)	7F	7F	7F	7F	7F	7F
68	Manufacturer's JEDEC ID Code (5)	7F	7F	7F	7F	7F	7F
69	Manufacturer's JEDEC ID Code (6)	51	51	51	51	51	51
70	Manufacturer's JEDEC ID Code (7)	00	00	00	00	00	00
71	Manufacturer's JEDEC ID Code (8)	00	00	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx	xx	xx
73	Product Type, Char 1	36	36	36	36	36	36
74	Product Type, Char 2	34	34	34	34	34	34
75	Product Type, Char 3	54	54	54	54	54	54
76	Product Type, Char 4	33	33	36	36	31	31
77	Product Type, Char 5	32	32	34	34	32	32
78	Product Type, Char 6	30	39	30	39	38	38
79	Product Type, Char 7	30	30	32	32	30	39
80	Product Type, Char 8	30	30	30	30	32	32
81	Product Type, Char 9	48	48	48	48	31	31
82	Product Type, Char 10	44	44	44	44	48	48
83	Product Type, Char 11	4C	4C	4C	4C	44	44
84	Product Type, Char 12	33	33	33	33	4C	4C
85	Product Type, Char 13	2E	2E	2E	2E	33	33
86	Product Type, Char 14	37	37	37	37	2E	2E
87	Product Type, Char 15	42	42	42	42	37	37
88	Product Type, Char 16	20	20	20	20	42	42

Product Type		**HYS64T32000HDL–3.7–B**	**HYS64T32900HDL–3.7–B**	**HYS64T64020HDL–3.7–B**	**HYS64T64920HDL–3.7–B**	**HYS64T128021HDL–3.7–B**	**HYS64T128921HDL–3.7–B**
Organization		**256MB**	**256MB**	**512MB**	**512MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×64**	**×64**	**×64**	**×64**
		1 Rank (×16)	**1 Rank (×16)**	**2 Ranks (×16)**	**2 Ranks (×16)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
89	Product Type, Char 17	20	20	20	20	20	20
90	Product Type, Char 18	20	20	20	20	20	20
91	Module Revision Code	4x	2x	4x	2x	4x	2x
92	Test Program Revision Code	xx	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00	00	00
128 - 255	Blank for customer use	FF	FF	FF	FF	FF	FF

TABLE 32
SPD codes for PC2–5300 4–4–4

Product Type		HYS64T32000HDL–3–B	HYS64T64020HDL–3–B	HYS64T128021HDL–3–B
Organization		256MB	512MB	1 GByte
		×64	×64	×64
		1 Rank (×16)	2 Ranks (×16)	2 Ranks (×8)
Label Code		PC2–5300S–444	PC2–5300S–444	PC2–5300S–444
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0D	0D	0E
4	Number of Column Addresses	0A	0A	0A
5	DIMM Rank and Stacking Information	60	61	61
6	Data Width	40	40	40
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	30	30	30
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	45	45	45
11	Error Correction Support (non-ECC, ECC)	00	00	00
12	Refresh Rate and Type	82	82	82
13	Primary SDRAM Width	10	10	08
14	Error Checking SDRAM Width	00	00	00
15	Not used	00	00	00
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04
18	Supported CAS Latencies	38	38	38
19	DIMM Mechanical Characteristics	01	01	01
20	DIMM Type Information	04	04	04
21	DIMM Attributes	00	00	00
22	Component Attributes	07	07	07
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	30	30	30

Product Type		**HYS64T32000HDL–3–B**	**HYS64T64020HDL–3–B**	**HYS64T128021HDL–3–B**
Organization		**256MB**	**512MB**	**1 GByte**
		×64	**×64**	**×64**
		1 Rank (×16)	**2 Ranks (×16)**	**2 Ranks (×8)**
Label Code		**PC2–5300S–444**	**PC2–5300S–444**	**PC2–5300S–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	45	45	45
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60
27	$t_{RP.MIN}$ [ns]	30	30	30
28	$t_{RRD.MIN}$ [ns]	28	28	1E
29	$t_{RCD.MIN}$ [ns]	30	30	30
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D
31	Module Density per Rank	40	40	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	20	20	20
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	27	27	27
34	$t_{DS.MIN}$ [ns]	10	10	10
35	$t_{DH.MIN}$ [ns]	17	17	17
36	$t_{WR.MIN}$ [ns]	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E
39	Analysis Characteristics	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00
41	$t_{RC.MIN}$ [ns]	39	39	39
42	$t_{RFC.MIN}$ [ns]	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	18	18	18
45	$t_{QHS.MAX}$ [ns]	22	22	22
46	PLL Relock Time	00	00	00
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	54	54	50
48	Psi(T-A) DRAM	72	72	7A
49	ΔT_0 (DT0)	67	67	53

Product Type		HYS64T32000HDL–3–B	HYS64T64020HDL–3–B	HYS64T128021HDL–3–B
Organization		**256MB**	**512MB**	**1 GByte**
		×64	**×64**	**×64**
		1 Rank (×16)	**2 Ranks (×16)**	**2 Ranks (×8)**
Label Code		**PC2–5300S–444**	**PC2–5300S–444**	**PC2–5300S–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	31	31	34
51	ΔT_{2P} (DT2P)	33	33	36
52	ΔT_{3N} (DT3N)	24	24	27
53	$\Delta T_{3P.fast}$ (DT3P fast)	47	47	4C
54	$\Delta T_{3P.slow}$ (DT3P slow)	27	27	2A
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	54	54	4C
56	ΔT_{5B} (DT5B)	1E	1E	20
57	ΔT_{7} (DT7)	37	37	25
58	Psi(ca) PLL	00	00	00
59	Psi(ca) REG	00	00	00
60	ΔT_{PLL} (DTPLL)	00	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00
62	SPD Revision	12	12	12
63	Checksum of Bytes 0-62	E1	E2	FA
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F
66	Manufacturer’s JEDEC ID Code (3)	7F	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	36	36	36
74	Product Type, Char 2	34	34	34
75	Product Type, Char 3	54	54	54

Product Type		**HYS64T32000HDL–3–B**	**HYS64T64020HDL–3–B**	**HYS64T128021HDL–3–B**
Organization		**256MB**	**512MB**	**1 GByte**
		×64	**×64**	**×64**
		1 Rank (×16)	**2 Ranks (×16)**	**2 Ranks (×8)**
Label Code		**PC2–5300S–444**	**PC2–5300S–444**	**PC2–5300S–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
76	Product Type, Char 4	33	36	31
77	Product Type, Char 5	32	34	32
78	Product Type, Char 6	30	30	38
79	Product Type, Char 7	30	32	30
80	Product Type, Char 8	30	30	32
81	Product Type, Char 9	48	48	31
82	Product Type, Char 10	44	44	48
83	Product Type, Char 11	4C	4C	44
84	Product Type, Char 12	33	33	4C
85	Product Type, Char 13	42	42	33
86	Product Type, Char 14	20	20	42
87	Product Type, Char 15	20	20	20
88	Product Type, Char 16	20	20	20
89	Product Type, Char 17	20	20	20
90	Product Type, Char 18	20	20	20
91	Module Revision Code	3x	3x	4x
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx
99 - 127	Not used	00	00	00
128 - 255	Blank for customer use	FF	FF	FF

5 Package Outlines

This chapter contains the package outlines of the products.

FIGURE 5
Package Outline Raw Card A L-DIM-200-31

67.6
63.6 ±0.1
3.8 MAX.
30
1.8 ±0.05
4 ±0.1
Thermal Sensor optional
(2.15)
1
17.55 ±0.1
(2.45)
100
1±0.1
2.7 ±0.1
(1.5)
11.4 ±0.1
47.4 ±0.1
(1.8)
(2.45)
2.4 ±0.1
(2.15)
1±0.1
4 ±0.1
101
200
6 ±0.1
SPD
20 ±0.1
2 MIN.
Detail of contacts
0.25 -0.18
2.55
0.45 ±0.03
0.6 ±0.1
GLD09649

Notes

1. *Drawing according to ISO 8015*
2. *Dimensions in mm*
3. *General tolerances +/- 0.15*

FIGURE 6
Package Outline Raw Card C L-DIM-200-30

67.6
63.6 ±0.1
3.8 MAX.
1.8 ±0.05
4 ±0.1
IC2
30
(2.15)
1
17.55 ±0.1
Optional
(2.45)
100
1±0.1
2.7 ±0.1
(1.5)
11.4 ±0.1
47.4 ±0.1
(1.8)
(2.45)
2.4 ±0.1
(2.15)
1±0.1
4 ±0.1
101
200
6 ±0.1
20 ±0.1
IC1
2 MIN.
Detail of contacts
0.25 -0.18
2.55
0.45 ±0.03
0.6 ±0.1
Burnished, no burr allowed
GLD09648

Notes

1. *Drawing according to ISO 8015*
2. *Dimensions in mm*
3. *General tolerances +/- 0.15*

FIGURE 7
Package Outline L-DIM-200-36

Notes

1. *Drawing according to ISO 8015*
2. *Dimensions in mm*
3. *General tolerances +/- 0.15*

6 Product Type Nomenclature

Qimonda's nomenclature uses simple coding combined with some propriatory coding. **Table 33** provides examples for module and component product type number as well as the field number. The detailed field description together with possible values and coding explanation is listed for modules in **Table 34** and for components in **Table 35**.

TABLE 33
Nomenclature Fields and Examples

Example for	Field Number										
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
Micro-DIMM	HYS	64	T	64/128	0	2	0	K	M	–5	–A
DDR2 DRAM	HYB	18	T	512/1G	16		0	A	C	–5	

TABLE 34
DDR2 DIMM Nomenclature

Field	Description	Values	Coding
1	Qimonda Module Prefix	HYS	Constant
2	Module Data Width [bit]	64	Non-ECC
		72	ECC
3	DRAM Technology	T	DDR2
4	Memory Density per I/O [Mbit]; Module Density[1)]	32	256 MByte
		64	512 MByte
		128	1 GByte
		256	2 GByte
		512	4 GByte
5	Raw Card Generation	0 .. 9	Look up table
6	Number of Module Ranks	0, 2, 4	1, 2, 4
7	Product Variations	0 .. 9	Look up table
8	Package, Lead-Free Status	A .. Z	Look up table
9	Module Type	D	SO-**D**IMM
		M	**M**icro-DIMM
		R	**R**egistered
		U	**U**nbuffered
		F	**F**ully Buffered

Field	Description	Values	Coding
10	Speed Grade	–2.5F	PC2–6400 5–5–5
		–2.5	PC2–6400 6–6–6
		–3	PC2–5300 4–4–4
		–3S	PC2–5300 5–5–5
		–3.7	PC2–4200 4–4–4
		–5	PC2–3200 3–3–3
11	Die Revision	–A	First
		–B	Second

1) Multiplying “Memory Density per I/O” with “Module Data Width” and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column “Coding”.

TABLE 35
DDR2 DRAM Nomenclature

Field	Description	Values	Coding
1	Qimonda Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL_18
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	Look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	–25F	DDR2-800 5-5-5
		–2.5	DDR2-800 6-6-6
		–3	DDR2-667 4-4-4
		–3S	DDR2-667 5-5-5
		–3.7	DDR2-533 4-4-4
		–5	DDR2-400 3-3-3

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