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RF3334

IF LOW NOISE AMPLIFIER/MIXER

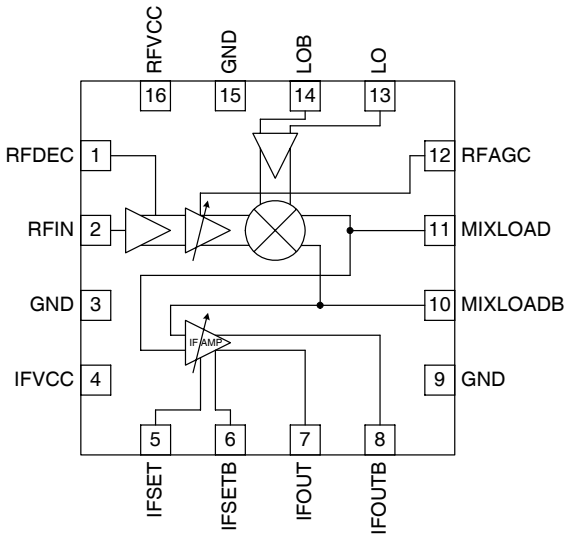
RoHS Compliant & Pb-Free Product
Package Style: QFN, 16-Pin, 4 x 4

Features

- 30dB RF Gain Control
- 40dB IF Gain Control
- 5dB Max. Noise Figure SSB
- LNA Input Internally Matched to 75Ω
- Single 5V Supply

Applications

- Cable Set Top Box
- General Purpose Downconverter
- Commercial and Consumer Systems



Functional Block Diagram

Product Description

The RF3334 is an IF LNA/Mixer suitable for downconversion of forward channel control data in a set-top box application. It consists of a single-ended 75Ω terminated LNA, followed by a differential gain control stage with 30dB of analog gain control and a double-balanced mixer. The mixer load is available via pins 10 and 11 should an external filter be required. The mixer output is connected to an IF amplifier that can be configured from 10dB to 40dB gain with an external resistor. The amplifier is capable of 6V pk-pk output into a 1kΩ load.

Ordering Information

RF3334	LNA Mixer
RF3334PCBA-41X	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☑ Si BiCMOS	☐ Si CMOS	
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to 7.0	V_{DC}
IF Input Level	500	mV_{pp}
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
DC Specifications					
Supply Voltage	4.75	5	5.25	V	
Supply Current	20	24		mA	
RFAGC Control Voltage	0.5		4.5	V	0.5V=Minimum Gain 4.5V=Maximum Gain
RFAGC Input Impedance		300		kΩ	
AC Specifications					
LNA+AGC+Mixer					
RF Frequency Range		0 to 700		MHz	On-chip signal path is DC-coupled, minimum frequency depends on external AC coupling components.
RF Input 3dB Bandwidth		700		MHz	On-chip signal path is DC-coupled, minimum frequency depends on external AC coupling components.
RF Input Impedance		75		Ω	
RF Input VSWR		1.4			At 100MHz
Mixer Output 3dB Bandwidth		100		MHz	Defined by on-chip first-order low-pass filter
Mixer Output Impedance		300		Ω	Differential
Mixer Output VSWR		1.2			At 100MHz
Maximum Gain	27	30		dB	RFAGC=4.5V
Minimum Gain		-2		dB	RFAGC=0.5V
Output 1dB Compression		90		dBμV(rms)	Maximum Gain
Input IP3, Maximum Gain		78		dBμV(rms)	LNA Input to Mixer Output
Input IP3, Minimum Gain		79		dBμV(rms)	LNA Input to Mixer Output
Noise Figure			5	dB	SSB, Cascaded LNA, AGC & Mixer

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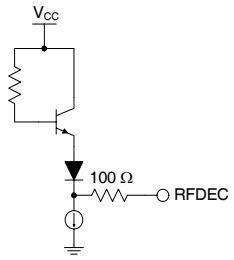
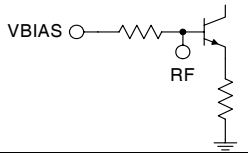
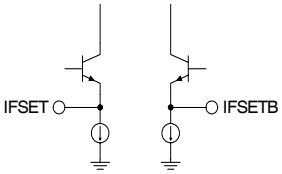
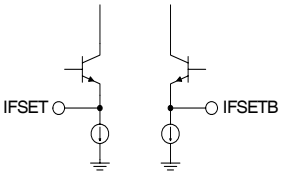
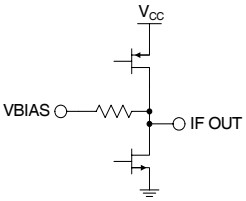
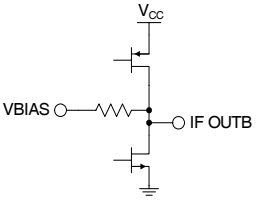
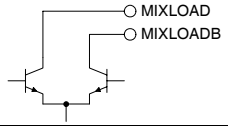
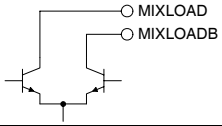
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
LO					
LO Frequency Range		0 to 800		MHz	
LO Input Impedance		75		Ω	Differential
LO Input VSWR		1.6:1			
LO Input Level	80			dBuV	
LO Bandwidth		800		MHz	
LO Rejection to RF Input		50		dB	
LO Rejection to Input of IF Amplifier		65		dB	
IF Amplifier					
IF Frequency Range		0 to 120		MHz	
Input Impedance		4000		Ω	Differential
Output Impedance		10		Ω	Differential
Differential Voltage Gain					
Gain Set Resistor=2500Ω		10		dB	R1=1kΩ
Gain Set Resistor=140Ω		31		dB	R1=1kΩ
Gain Set Resistor=5Ω		40		dB	R1=1kΩ
IF 3dB Bandwidth	140			MHz	Gain Set=5Ω
Equivalent Input Noise		1.5		μVrms	Gain Set=140Ω
Output Swing		6	8	V_{P-P}	Into 1kΩ load, at 50MHz
Output 1dB Compression		127		dBμV(rms)	Into 1kΩ load, at 50MHz
Output IP3		137		dBμV(rms)	Into 1kΩ load, at 50MHz
Thermal					V_{CC}=5.25V, VRFAGC=4.5V, I_{CC}=29mA, P_{DISS}=154mW
$Theta_{JC}$		65		°C/W	
Maximum Measured Junction Temperature at DC Bias Conditions		95		°C	T_{AMB}=+85°C

Pin	Function	Description	Interface Schematic
1	RFDEC	External decoupling capacitor for RF single-ended to differential converter.	
2	RF	LNA Input, Internally matched to 75Ω. Should be AC-coupled.	
3	GND	Ground.	
4	IFVCC	5V supply for IF section.	
5	IFSET	IF Gain select. The resistance between this pin and pin 6 (IFSETB) determines the gain of the IF amplifier. Maximum gain is achieved by placing a short circuit between the pins. Larger values of resistance will reduce the IF gain according to the following equation where R is the value of resistance between pins 5 and 6. IFGain=20log(1600/(R=75))15.	
6	IFSETB	Complementary IF Gain select.	
7	IFOUT	IF Amplifier Output. Differential output of the IF amplifier. The differential load across this pin and pin 8 (IFOUTB) should be 1kΩ or greater for optimal performance. The differential output impedance across this pin and pin 8 in 10Ω.	
8	IFOUTB	Complementary IF Amplifier Output.	
9	GND	Ground.	
10	MIXLOADB	Complementary Mixer load.	
11	MIXLOAD	Differential output of the RF mixer. A resonant load should be applied to this pin and pin 10 (MIXLOADB) that will act as a bandpass filter at the desired IF frequency. V_{CC} should be supplied to this pin via an inductor or a resistor. Use of a resistor will degrade intermodulation performance.	

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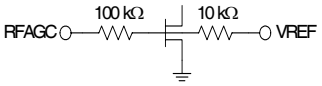
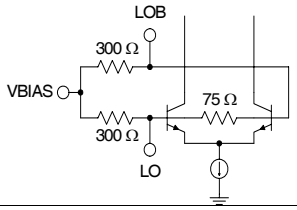
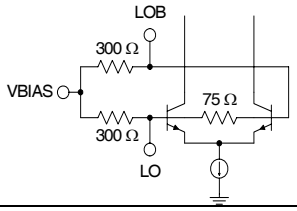
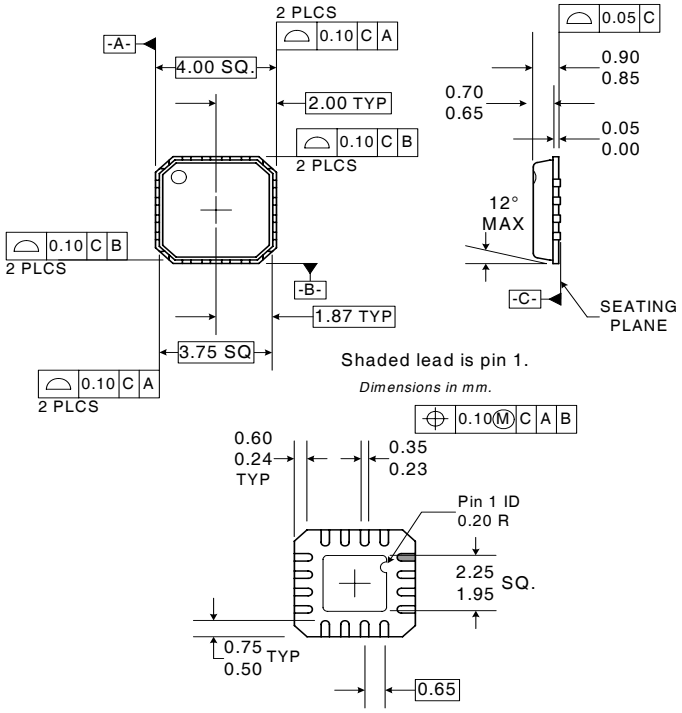
Pin	Function	Description	Interface Schematic
12	RFAGC	RF Gain select voltage input. The voltage applied to this pin sets the gain of the RF amplifier. The voltage applied to this pin should be between 0.5V and 4.5V. The RF gain characteristic is such that 0.5V yields a gain of -2dB and 4.5V yields a gain of +30dB as measured from the input of the LNA to the output of the mixer stage.	
13	LO	Differential LO Input. This pin and pin 14 (LOB) are the differential LO inputs. This input should be AC-coupled. The differential input impedance across pins 13 and 14 is 75Ω. The LO may be driven single ended but will require a higher drive level. If a single ended LO is applied, pin 14 should be AC-coupled to ground.	
14	LOB	Complementary LO Input. Should be AC-coupled.	
15	GND	Ground.	
16	RFVCC	5V supply for RF section.	
GND	Paddle	Backside of package should be connected to ground.	

Package Drawing



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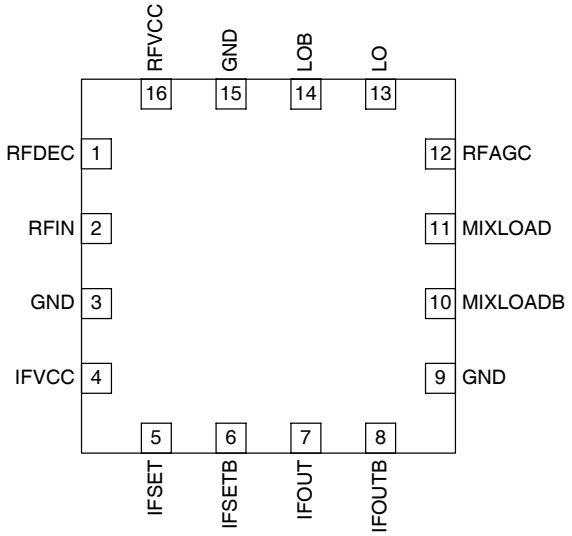
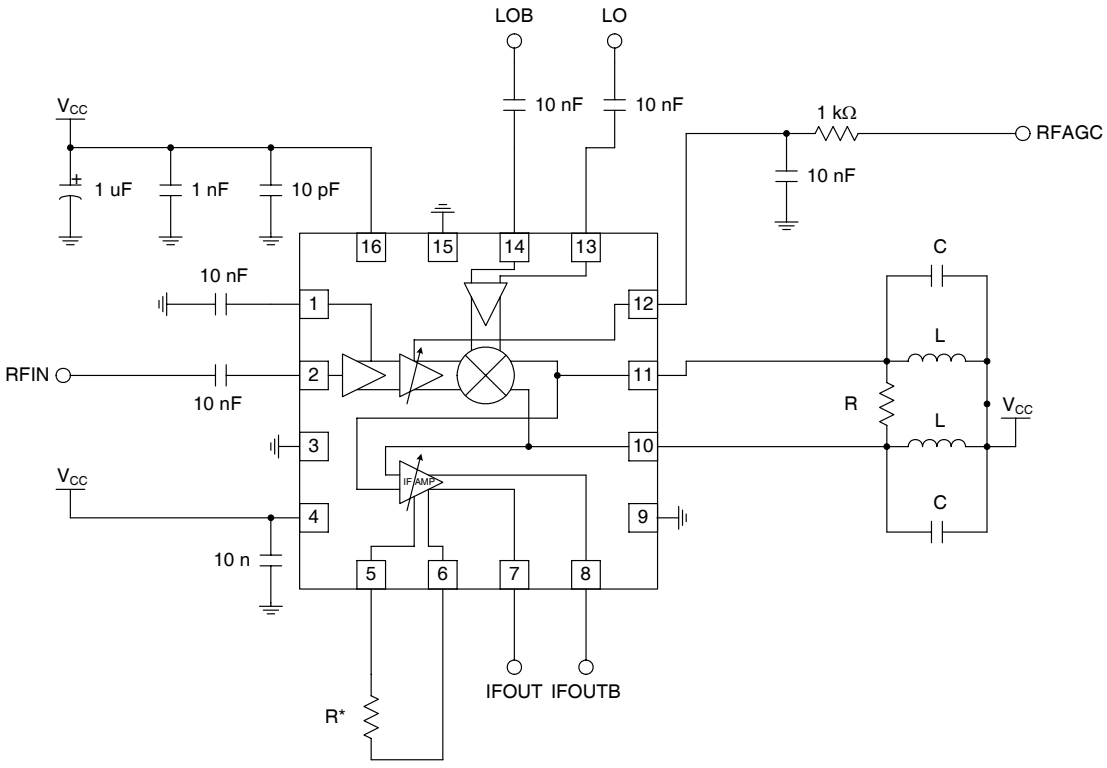
Pin-Out



Application Schematic



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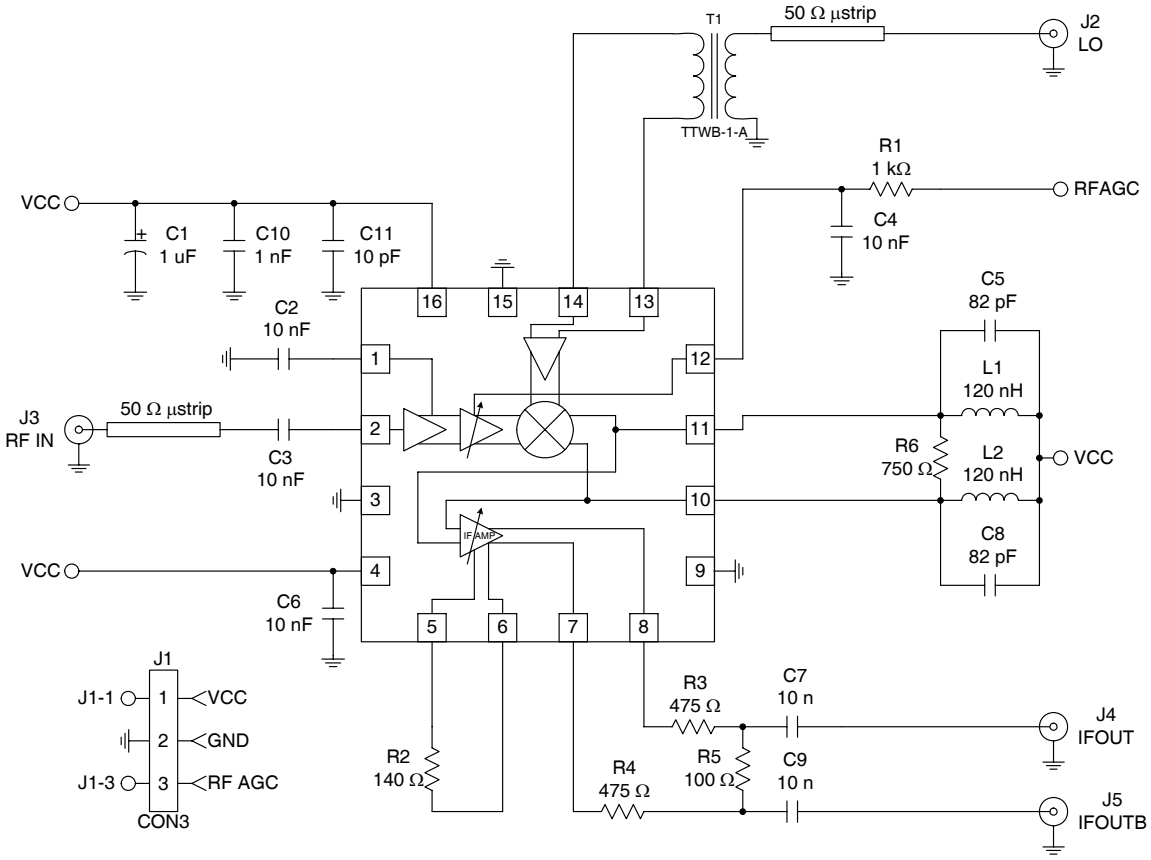
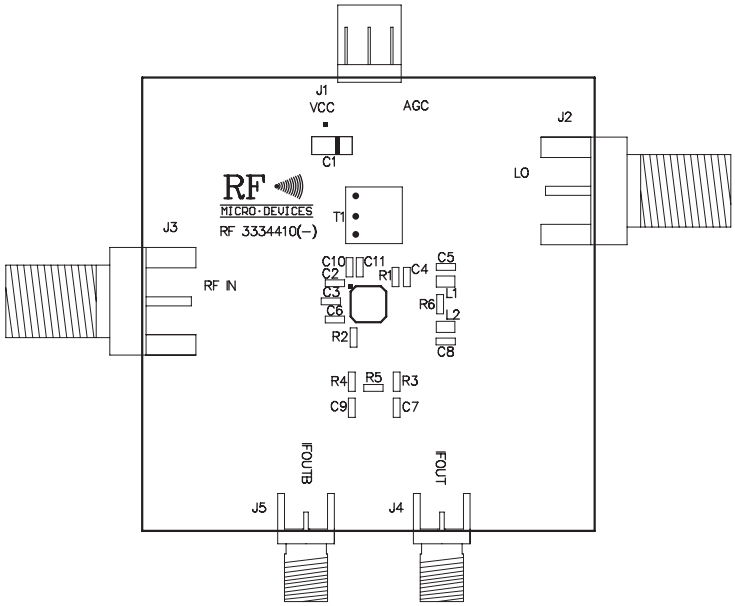
Evaluation Board Schematic

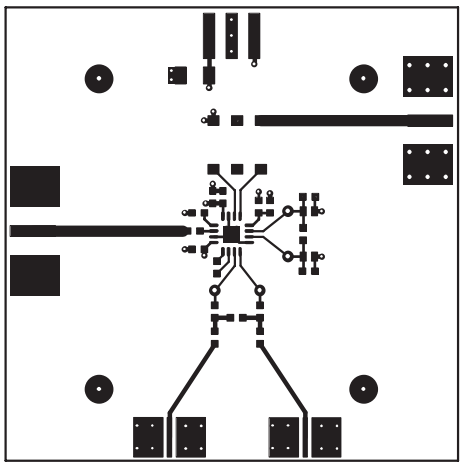


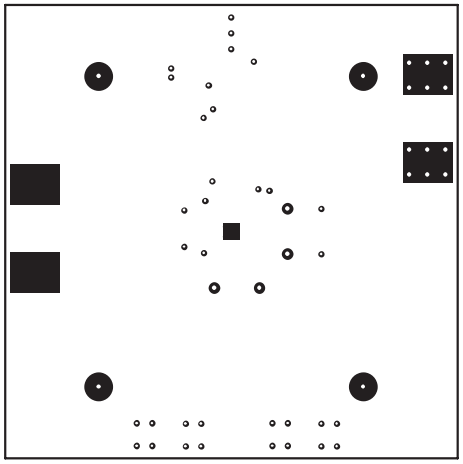
Evaluation Board Layout

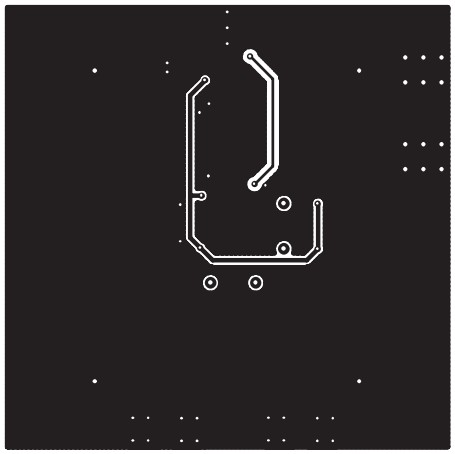
Board Size 2.0” x 2.0”

Board Thickness 0.032”, Board Material FR-4, Multi-layer









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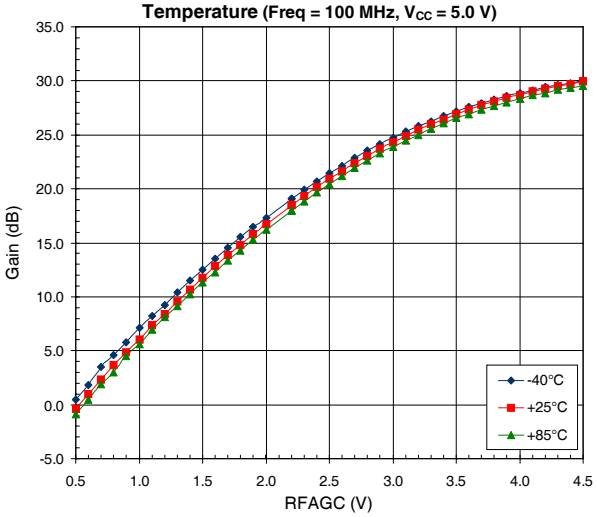
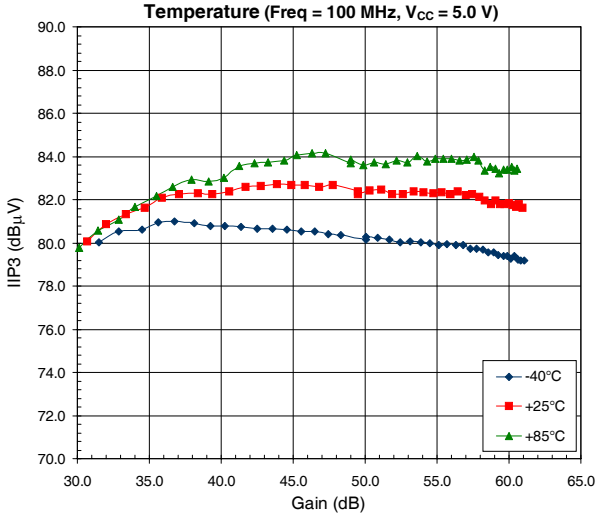
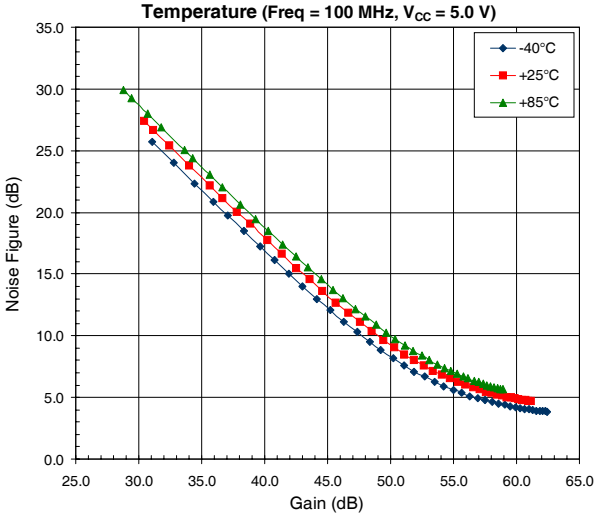
LNA + AGC + Mixer Gain versus Control Voltage over Temperature (Freq = 100 MHz, V_{CC} = 5.0 V)



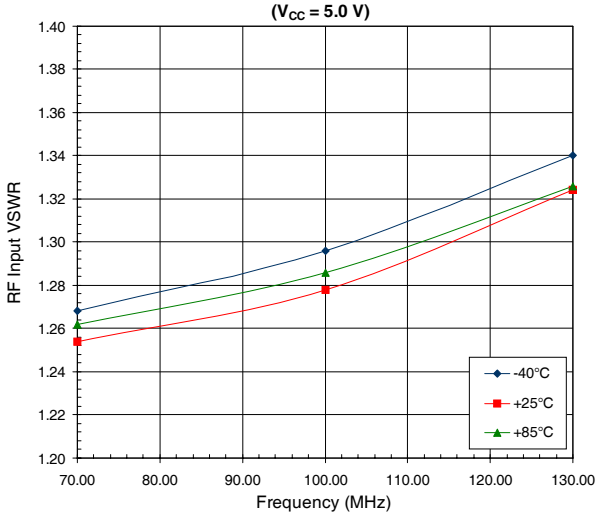
LNA + AGC + Mixer + IF AMP - IIP3 versus Gain over Temperature (Freq = 100 MHz, V_{CC} = 5.0 V)



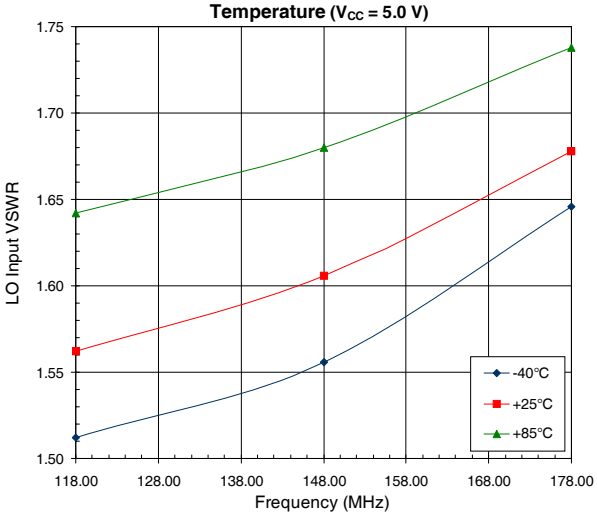
SSB, Cascaded Noise Figure versus Gain over Temperature (Freq = 100 MHz, V_{CC} = 5.0 V)



RF Input VSWR versus Frequency Across Temperature (V_{CC} = 5.0 V)



LO Input VSWR versus Temperature Across Temperature (V_{CC} = 5.0 V)



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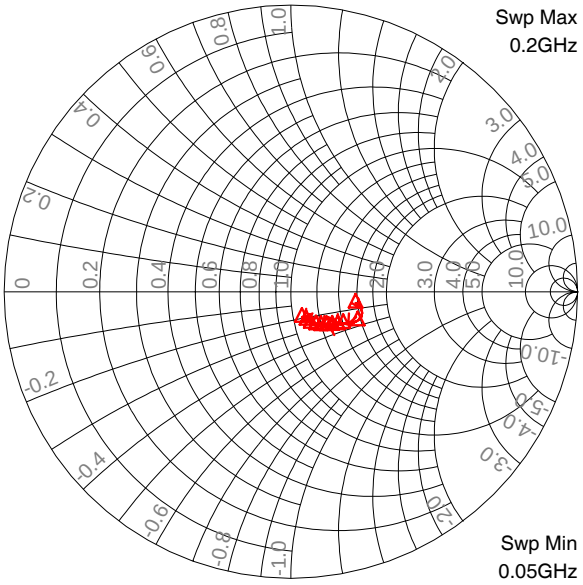
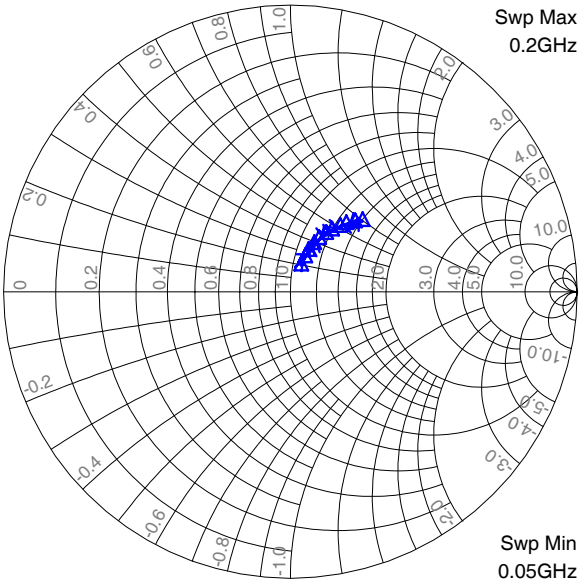
RF Input, Temp = +25°C



LO Input, Temp = +25°C



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PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Pattern

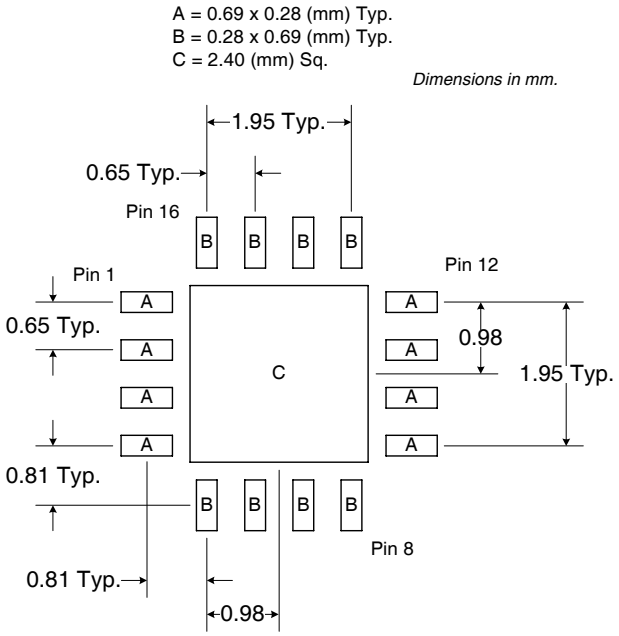

Figure 1. PCB Metal Land Pattern (Top View)

PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

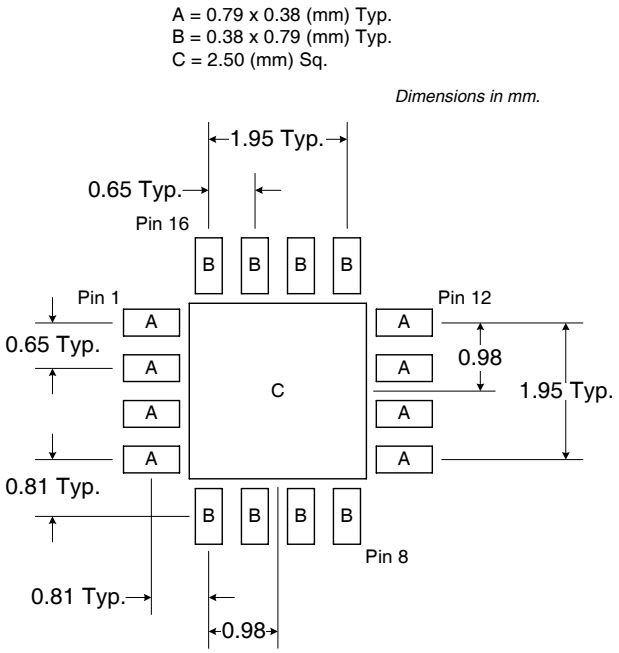

Figure 2. PCB Solder Mask Pattern (Top View)

Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

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