S29NS-J

128 Megabit (8 M x 16-Bit), 64 Megabit (4 M x 16-Bit), 32 Megabit (2 M x 16-Bit), and 16 Megabit (1 M x 16 Bit), 110 nm CMOS 1.8-Volt only Simultaneous Read/Write, Burst Mode Flash Memories

Data Sheet

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

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Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

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S29NS-J

128 Megabit (8 M x 16-Bit), 64 Megabit (4 M x 16-Bit), 32 Megabit (2 M x 16-Bit), and 16 Megabit (1 M x 16 Bit), 110 nm CMOS 1.8-Volt only Simultaneous Read/Write, Burst Mode Flash Memories

Data Sheet

Features

- **Single 1.8 volt read, program and erase (1.7 to 1.95 V)**
- **Multiplexed Data and Address for reduced I/O count**
  - A15–A0 multiplexed as DQ15–DQ0
  - Addresses are latched by AVD# control input when CE# low
- **Simultaneous Read/Write operation**
  - Data can be continuously read from one bank while executing erase/program functions in other bank
  - Zero latency between read and write operations
- **Read access times at 54 MHz (C_L=30 pF)**
  - Burst access times of 11/13.5 ns at industrial temperature range
  - Asynchronous random access times of 65/70 ns
  - Synchronous random access times of 71/87.5 ns
- **Burst Modes**
  - Continuous linear burst
  - 8/16/32 word linear burst with wrap around
  - 8/16/32 word linear burst without wrap around
- **Power dissipation (typical values, 8 bits switching, C_L = 30 pF)**
  - Burst Mode Read: 25 mA
  - Simultaneous Operation: 40 mA
  - Program/Erase: 15 mA
  - Standby mode: 9 µA
- **Sector Architecture**
  - Four 8 Kword sectors
  - Two hundred fifty-five (S29NS128J), one hundred twenty-seven (S29NS064J),sixty-three (S29NS032J), or thirty-one (S29NS016J) 32 Kword sectors
  - Four banks (see next page for sector count and size)
- **Sector Protection**
  - Software command sector locking
  - WP# protects the two highest sectors
  - All sectors locked when $A_{cc} = V_{IL}$
- **Handshaking feature**
  - Provides host system with minimum possible latency by monitoring RDY
- **Supports Common Flash Memory Interface (CFI)**
- **Software command set compatible with JEDEC 42.4 standards**
  - Backwards compatible with Am29F and Am29LV families
- **Manufactured on 110 nm process technology**
- **Embedded Algorithms**
  - Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Data# Polling**
  - Provides a software method of detecting program and erase operation completion
- **Erase Suspend/Resume**
  - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset input (RESET#)**
  - Hardware method to reset the device for reading array data
- **CMOS compatible inputs and outputs**
- **Package**
  - 48-ball Very Thin FBGA (S29NS128J)
  - 44-ball Very Thin FBGA (S29NS064J, S29NS032J, S29NS016J)
- **Cycling Endurance: 1 million cycles per sector typical**
- **Data Retention: 20 years typical**

General Description

The S29NS128J, S29NS064J, S29NS032J and S29NS016J are 128 Mbit, 64 Mbit, 32 Mbit and 16 Mbit 1.8 Volt-only, Simultaneous Read/Write, Burst Mode Flash memory devices, organized as 8,388,608, 4,194,304, 2,097,152 and 1,048,576. words of 16 bits each. These devices use a single V_{CC} of 1.7 to 1.95 V to read, program, and erase the memory array. A 12.0-volt A_{cc} may be used for faster program performance if desired. These devices can also be programmed in standard EPROM programmers.

The devices are offered at the following speeds:

Clock Speed	Burst Access (ns)	Synch. Initial Access (ns)	Asynchronous Initial Access (ns)	Output Loading
54 MHz	13.5	87.5	70	30 pF

The devices operate within the temperature range of –25 °C to +85 °C, and are offered Very Thin FBGA packages.

Simultaneous Read/Write Operations with Zero Latency

The Simultaneous Read/Write architecture divides the memory space into four banks. The device allows a host system to program or erase in one bank, then immediately and simultaneously read from another bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

The devices are structured as shown in the following tables:

S29NS128J			
Bank A Sectors		**Bank B, C & D Sectors**	
Quantity	**Size**	**Quantity**	**Size**
4	8 Kwords	64	32 Kwords
63	32 Kwords		
32 Mbits total		96 Mbits total	

S29NS064J			
Bank A Sectors		**Bank B, C & D Sectors**	
Quantity	**Size**	**Quantity**	**Size**
4	8 Kwords	32	32 Kwords
31	32 Kwords		
16 Mbits total		48 Mbits total	

S29NS032J			
Bank A Sectors		**Bank B, C & D Sectors**	
Quantity	**Size**	**Quantity**	**Size**
4	8 Kwords	16	32 Kwords
15	32 Kwords		
8 Mbits total		24 Mbits total	

S29NS016J			
Bank A Sectors		**Bank B, C & D Sectors**	
Quantity	**Size**	**Quantity**	**Size**
4	8 Kwords	8	32 Kwords
7	32 Kwords		
4 Mbits total		12 Mbits total	

The devices use Chip Enable (CE#), Write Enable (WE#), Address Valid (AVD#) and Output Enable (OE#) to control asynchronous read and write operations. For burst operations, the devices additionally require Ready (RDY) and Clock (CLK). This implementation allows easy interface with minimal glue logic to microprocessors/microcontrollers for high performance read operations.

The devices offer complete compatibility with the **JEDEC 42.4 single-power-supply Flash command set standard**. Commands are written to the command register using standard microprocessor write timings. Reading data out of the device are similar to reading from other Flash or EPROM devices.

The host system can detect whether a program or erase operation is complete by using the device **status bit** DQ7 (Data# Polling). After a program or erase cycle has been completed, the device automatically returns to reading array data.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The devices are fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The devices also offer three types of data protection at the sector level. The **sector**

lock/unlock command sequence disables or re-enables both program and erase operations in any sector. When at V_{IL}, **WP#** locks the highest two sectors. Finally, when $\mathbf{A_{cc}}$ is at V_{IL}, all sectors are locked.

The devices offer two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both modes.

Table of Contents

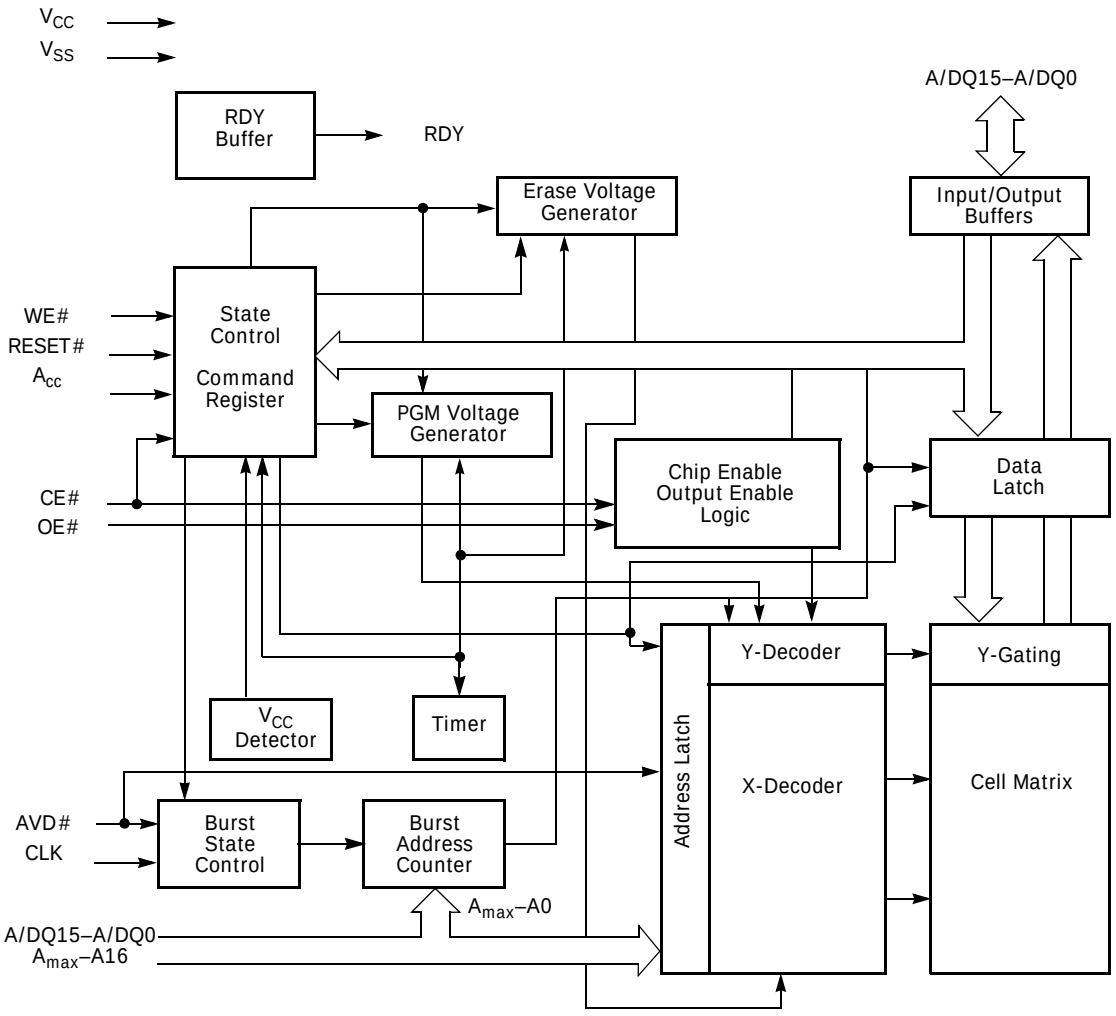
Figures

Tables

1. Product Selector Guide

Part Number	S29NS128J, S29NS064J, S29N032J, 29NS016J
Burst Frequency	**54 MHz**
Speed Option	**0L**
Max Initial Synchronous Access Time, ns (t_{IACC})	87.5
Max Burst Access Time, ns (t_{BACC})	13.5
Max Asynchronous Access Time, ns (t_{ACC})	70
Max CE# Access Time, ns (t_{CE})	
Max OE# Access Time, ns (t_{OE})	13.5

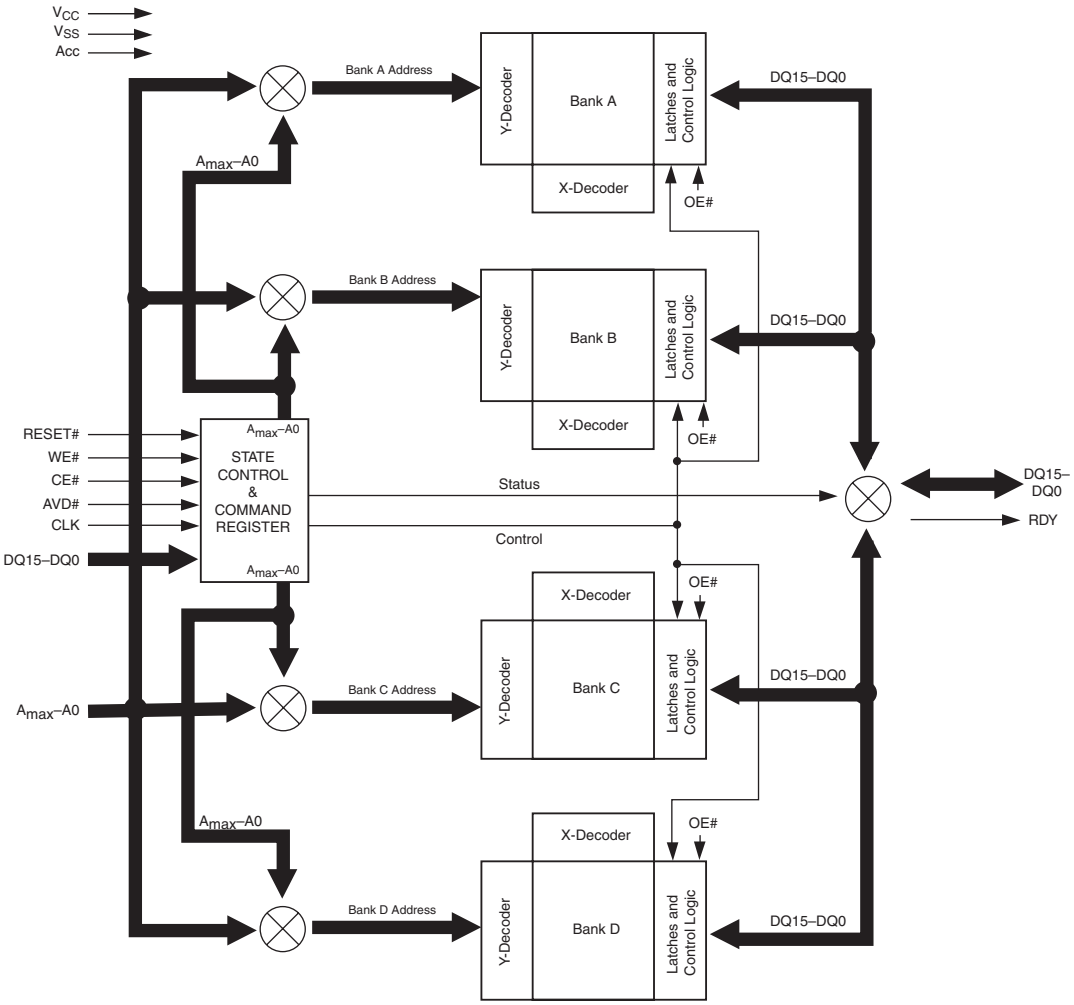
2. Block Diagram



Note:

1. *A_{max} indicates the highest order address bit.*

2.1 Block Diagram of Simultaneous Operation Circuit



Notes:

1. *A15–A0 are multiplexed with DQ15–DQ0.*
2. *Amax indicates the highest order address bit.*

3. Connection Diagrams

Figure 3.1 S29NS128J—48-Ball Very Thin FBGA (VDC048)

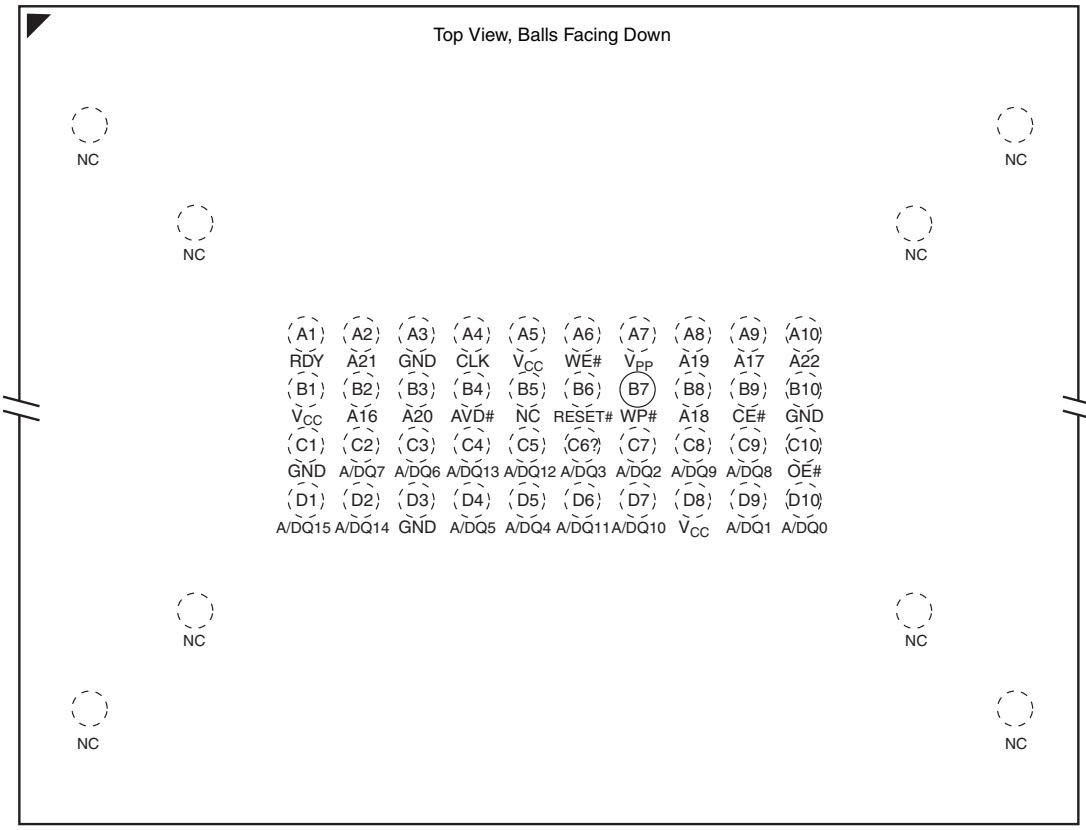


Figure 3.2 S29NS064J—44-Ball Very Thin FBGA (VDD044)

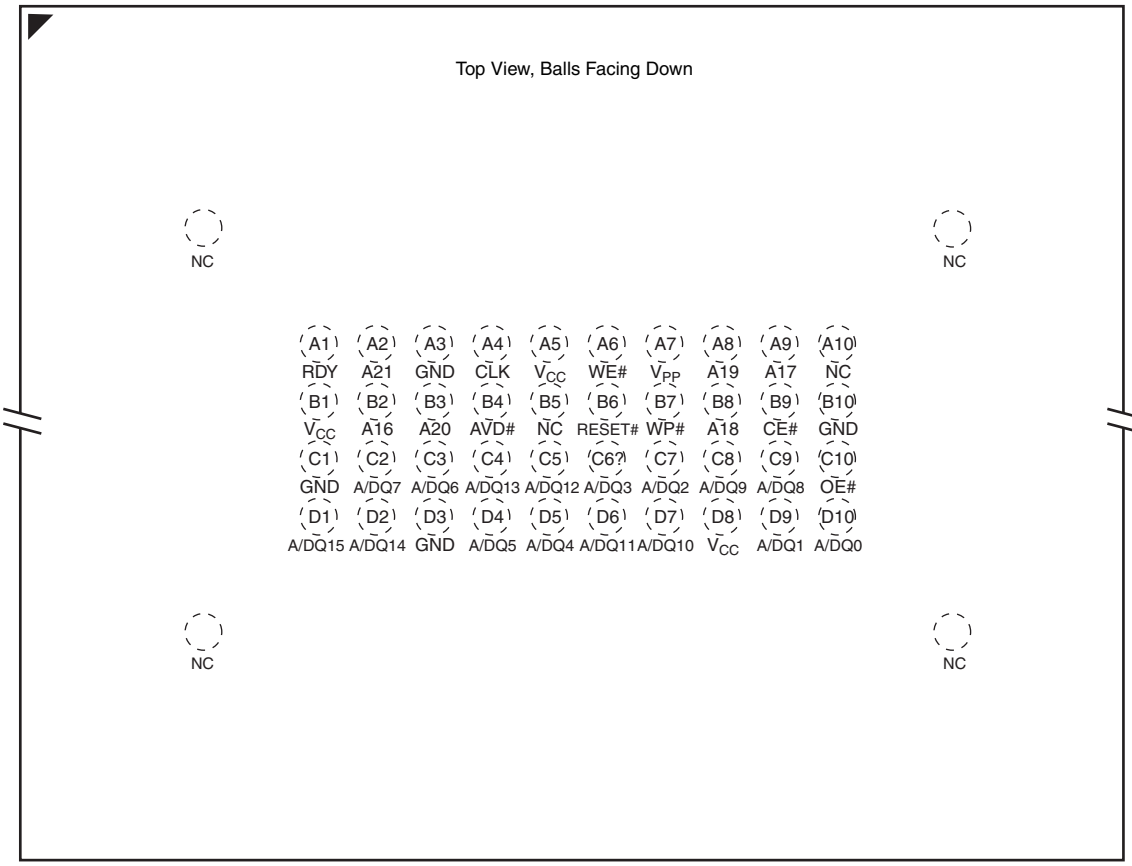


Figure 3.3 S29NS032J—44-Ball Very Thin FBGA (VDE044)

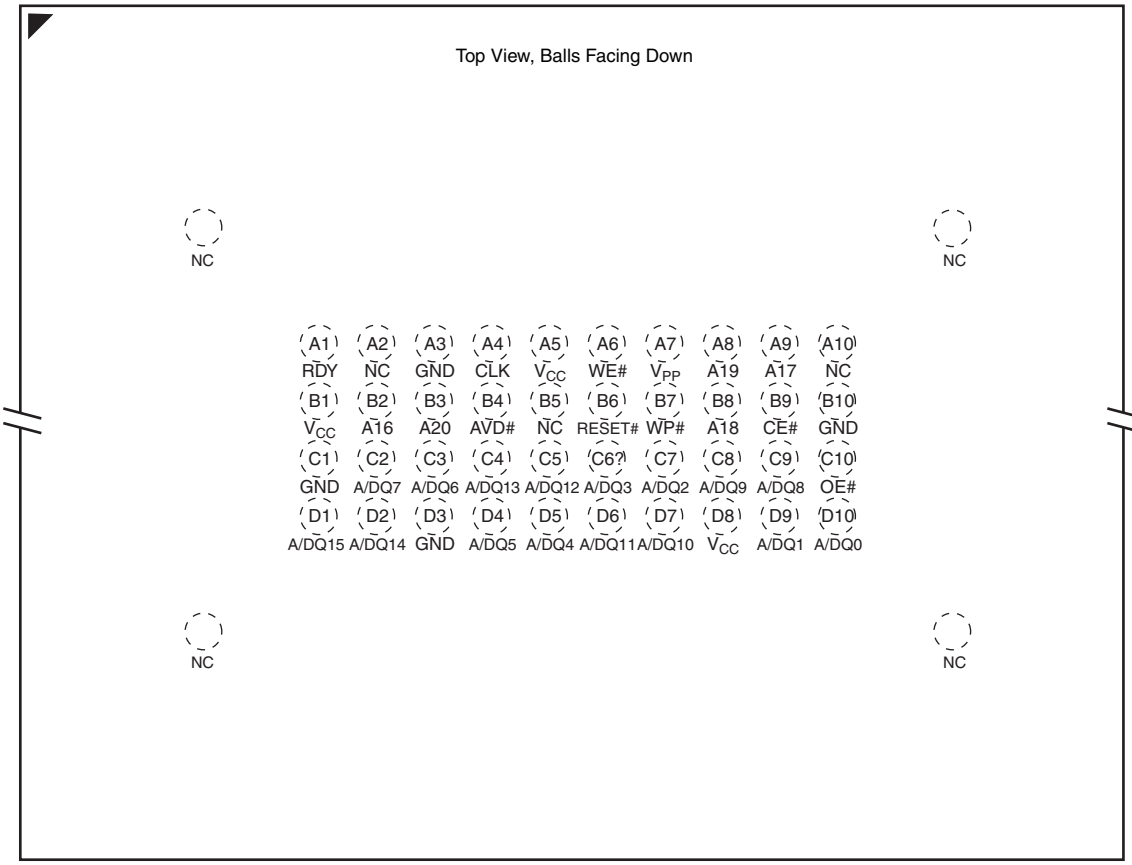
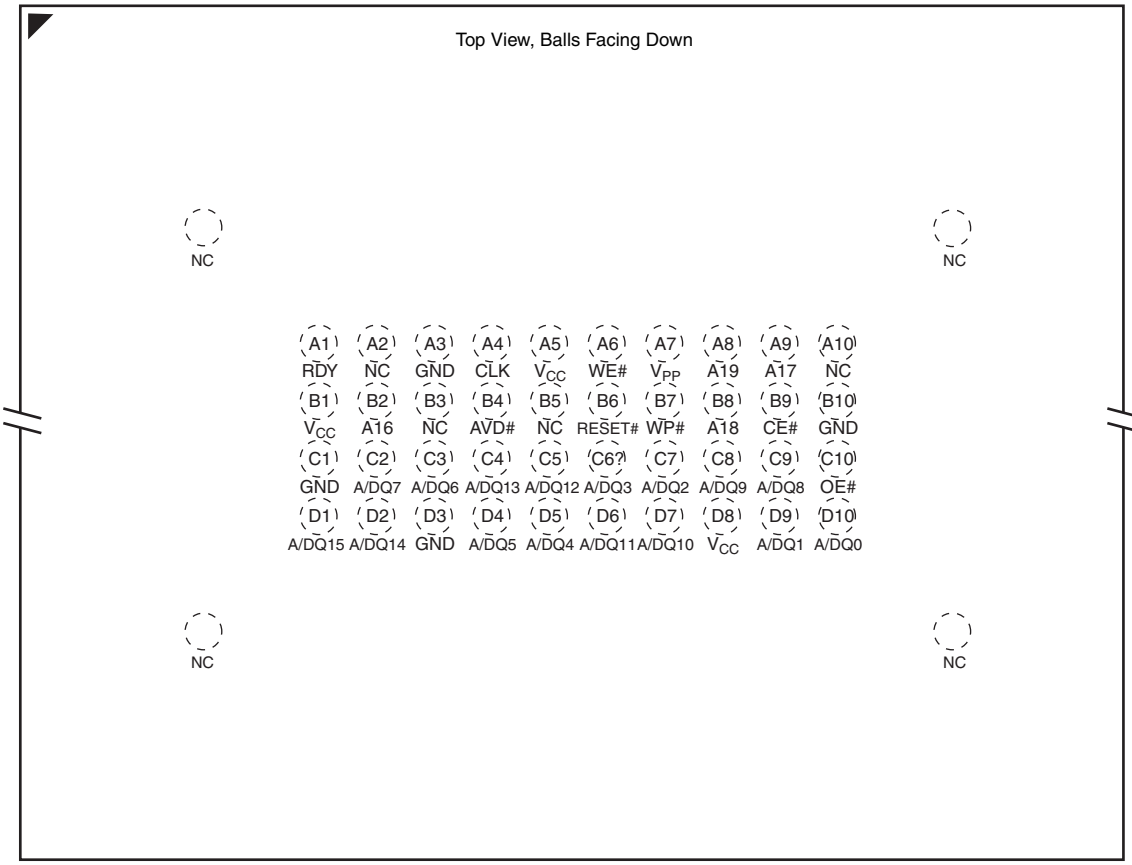


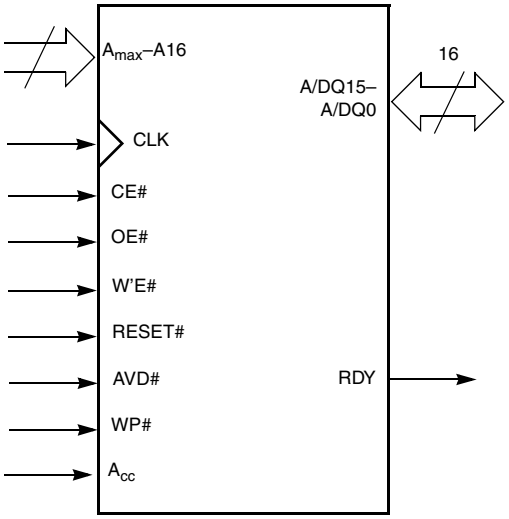
Figure 3.4 S29NS016J—44-Ball Very Thin FBGA (VDE044)



4. Input/Output Descriptions

Signal	Description
A22–A16	Address Inputs, S29NS128J
A21–A16	Address Inputs, S29NS064J
A20–A16	Address Inputs, S29NS032J
A19–A16	Address Inputs, S29NS016J
A/DQ15–A/DQ0	Multiplexed Address/Data input/output
CE#	Chip Enable Input. Asynchronous relative to CLK for the Burst mode.
OE#	Output Enable Input. Asynchronous relative to CLK for the Burst mode.
WE#	Write Enable Input.
V_{CC}	Device Power Supply (1.7 V–1.95 V).
GND	Ground
NC	No Connect; not connected internally
RDY	Ready output; indicates the status of the Burst read. V_{OL}= data invalid. V_{OH} = data valid.
CLK	The first rising edge of CLK in conjunction with AVD# low latches address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.
AVD#	Address Valid input. Indicates to device that the valid address is present on the address inputs (address bits A15–A0 are multiplexed, address bits A22–A16 are address only). V_{IL} = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. V_{IH}= device ignores address inputs
RESET#	Hardware reset input. V_{IL}= device resets and returns to reading array data
WP#	Hardware write protect input. V_{IL} = disables writes to SA257–258 (S29NS128J), SA129–130 (S29NS064J), SA65–66 (S29NS032J), or SA33-34 (S29NS016J). Should be at V_{IH} for all other conditions.
A_{cc}	At 12 V, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables program and erase functions. Should be at V_{IH} for all other conditions.

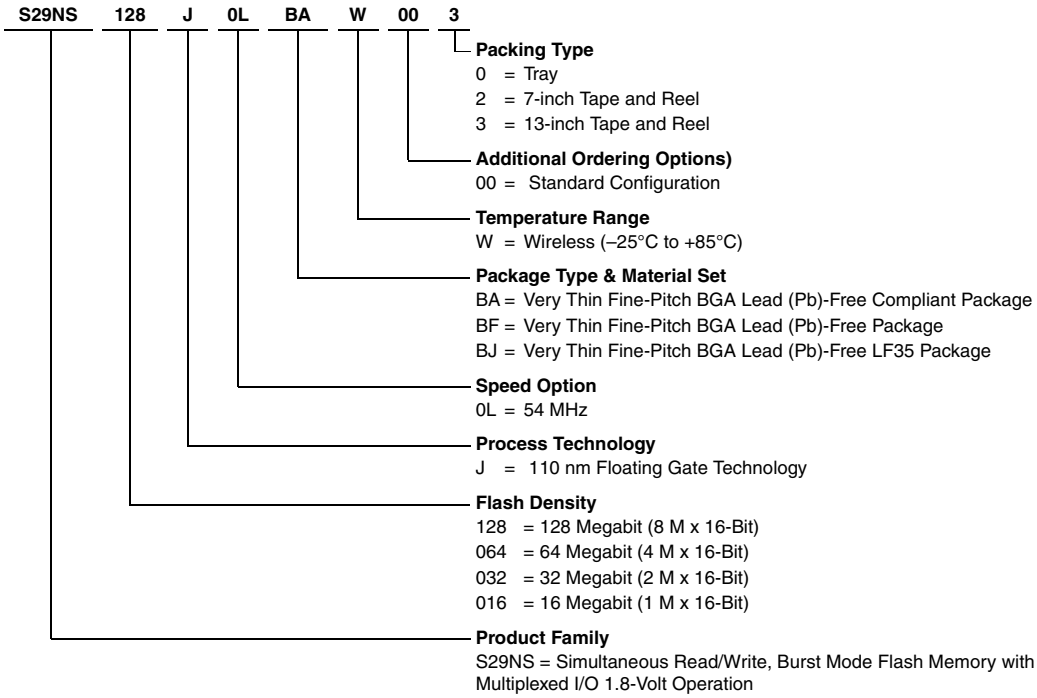
5. Logic Symbol



A_{max} indicates the highest order address bit.

6. Ordering Information

The ordering part number is formed by a valid combination of the following:



Valid Combinations

The following configurations are planned to be supported for this device. Contact your local Spansion sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Valid Combinations BGA Package					
Order Number	**Packing Type**	**Package Marking**	**Package**	**Density**	**Speed**
S29NS128J0LBAW00	0, 2 or 3	NS128J0LBAW00	Pb-Free Compliant	128	54 MHz
S29NS128J0LBJW00	0, 2 or 3	NS128J0LBJW00	Pb-free, LF35		
S29NS128J0LBFW00	0, 2 or 3	NS128J0LBFW00	Pb-free		
S29NS064J0LBAW00	0, 2 or 3	NS064J0LBAW00	Pb-Free Compliant	64	
S29NS064J0LBJW00	0, 2 or 3	NS064J0LBJW00	Pb-free, LF35		
S29NS064J0LBFW00	0, 2 or 3	NS064J0LBFW00	Pb-free		
S29NS032J0LBJW00	0, 2 or 3	NS032J0LBJW00	Pb-free, LF35	32	
S29NS032J0LBFW00	0, 2 or 3	NS032J0LBFW00	Pb-free		
S29NS016J0LBJW00	0, 2 or 3	NS016J0LBJW00	Pb-free, LF35	16	
S29NS016J0LBFW00	0, 2 or 3	NS016J0LBFW00	Pb-free		

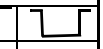
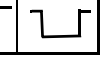
Note

For industrial temperature range, contact your local sales office.

7. Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 7.1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 7.1 Device Bus Operations

Operation	CE#	OE#	WE#	A_{max}–16	A/DQ15–0	RESET#	CLK	AVD#
Asynchronous Read	L	L	H	Addr In	I/O	H	L	
Write	L	H	L	Addr In	I/O	H	H/L	
Standby (CE#)	H	X	X	X	HIGH Z	H	H/L	X
Hardware Reset	X	X	X	X	HIGH Z	L	X	X
Burst Read Operations								
Load Starting Burst Address	L	H	H	Addr In	Addr In	H		
Advance Burst to next address with appropriate Data presented on the Data Bus	L	L	H	X	Burst Data Out	H		H
Terminate current Burst read cycle	H	X	H	X	HIGH Z	H		X
Terminate current Burst read cycle via RESET#	X	X	H	X	HIGH Z	L	X	X
Terminate current Burst read cycle and start new Burst read cycle	L	H	H	X	I/O	H		

Legend
L = Logic 0, H = Logic 1, X = Don't Care.

7.1 Requirements for Asynchronous Read Operation (Non-Burst)

To read data from the memory array, the system must assert a valid address on A/DQ15–A/DQ0 and A_{max}–A16, while AVD# and CE# are at V_{IL}. WE# should remain at V_{IH}. Note that CLK must remain at V_{IL} during asynchronous read operations. The rising edge of AVD# latches the address, after which the system can drive OE# to V_{IL}. The data will appear on A/DQ15–A/DQ0. (See Figure 14.5.) Since the memory array is divided into four banks, each bank remains enabled for read access until the command register contents are altered.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the outputs. The output enable access time (t_{OE}) is the delay from the falling edge of OE# to valid data at the output.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition.

7.2 Requirements for Synchronous (Burst) Read Operation

The device is capable of seven different burst read modes (see Table 8.9): continuous burst read; 8-, 16-, and 32-word linear burst reads with wrap around; and 8-, 16-, and 32-word linear burst reads without wrap around.

7.2.1 Continuous Burst

When the device first powers up, it is enabled for asynchronous read operation. The device will automatically be enabled for burst mode and addresses will be latched on the first rising edge on the CLK input, while AVD# is held low for one clock cycle. Prior to activating the clock signal, the system should determine how many wait states are desired for the initial word (t_{IACC}) of each burst session. The system would then write the Set Configuration Register command sequence.

The initial word is output t_{IACC} after the rising edge of the first CLK cycle. Subsequent words are output t_{BACC} after the rising edge of each successive clock cycle, which automatically increments the internal address counter. **Note that the device has a fixed internal address boundary that occurs every 64 words, starting at address 00003Fh. The transition from the highest address to 000000h is also a boundary**

crossing. During a boundary crossing, there is a two-cycle latency between the valid read at address 00003Eh and the valid read at address 00003Fh (or between addresses offset from these values by the same multiple of 64 words). RDY is deasserted during the two-cycle latency, and it is reasserted in the third cycle to indicate that the data at address 00003Fh (or offset from 3Fh by a multiple of 64 words) is ready. See Figure 14.13.

The device will continue to output continuous, sequential burst data, wrapping around to address 000000h after it reaches the highest addressable memory location, until the system asserts CE# high, RESET# low, or AVD# low in conjunction with a new address. See Table 7.1. The reset command does *not* terminate the burst read operation.

If the host system crosses the bank boundary while reading in burst mode, and the device is not programming or erasing, a two-cycle latency will occur as described above. If the host system crosses the bank boundary while the device is programming or erasing, the device will provide asynchronous read status information. The clock will be ignored. After the host has completed status reads, or the device has completed the program or erase operation, the host can restart a burst operation using a new address and AVD# pulse.

If the clock frequency is less than 6 MHz during a burst mode operation, additional latencies will occur. RDY indicates the length of the latency by pulsing low.

7.2.2 8-, 16-, and 32-Word Linear Burst with Wrap Around

These three modes are of the linear wrap around design, in which a fixed number of words are read from consecutive addresses. In each of these modes, the burst addresses read are determined by the group within which the starting address falls. The groups are sized according to the number of words read in a single burst sequence for a given mode (see Table 7.2.)

Table 7.2 Burst Address Groups

Mode	Group Size	Group Address Ranges
8-word	8 words	0-7h, 8-Fh, 10-17h, 18-1Fh...
16-word	16 words	0-Fh, 10-1Fh, 20-2Fh, 30-3Fh...
32-word	32 words	00-1Fh, 20-3Fh, 40-5Fh, 60-7Fh...

As an example: if the starting address in the 8-word mode is 39h, the address range to be read would be 38-3Fh, and the burst sequence would be 39-3A-3B-3C-3D-3E-3F-38h. The burst sequence begins with the starting address written to the device, but wraps back to the first address in the selected group. In a similar fashion, the 16-word and 32-word Linear Wrap modes begin their burst sequence on the starting address written to the device, and then wrap back to the first address in the selected address group. **Note that in these three burst read modes the address pointer does not cross the boundary that occurs every 64 words; thus, no wait states are inserted (except during the initial access).**

7.2.3 8-, 16-, and 32-Word Linear Burst without Wrap Around

In these modes, a fixed number of words (predefined as 8,16,or 32 words) are read from consecutive addresses starting with the initial word, which is written to the device. When the number of words has been read completely, the burst read operation stops and the RDY output goes low. There is no group limitation and is different from the Linear Burst with Wrap Around.

See Table 8.9 and Table 8.16 for the command of setting the 8-, 16-, and 32- Word Burst without Wrap Around.

As an example, for 8-word length Burst Read, if the starting address written to the device is 39h, the burst sequence would be 39-3A-3B-3C-3D-3E-3F-40h, and the read operation will be terminated at 40h. In a similar fashion, the 16-word and 32-word modes begin their burst sequence on the starting address written to the device, and Continuously Read to the predefined word length, 16 or 32 words.

The operation is similar to the Continuous Burst, but will stop the operation at fixed word length. It is possible the device crosses the fixed internal address boundary that occurs every 64 words during burst read; a latency occurs before data appears for the next address and RDY is pulsing low. If the host system crosses the bank boundary, the device will react in the same manner as in the Continuous Burst.

If the clock frequency is less than 6 MHz during a burst mode operation, additional latencies will occur. RDY indicates the length of the latency by pulsing low.

7.3 Programmable Wait State

The programmable wait state feature indicates to the device the number of additional clock cycles that must elapse after AVD# is driven active before data will be available. Upon power up, the device defaults to the maximum of seven total cycles. The total number of wait states is programmable from two to seven cycles.

The wait state command sequence requires three cycles; after the two unlock cycles, the third cycle address should be written according to the desired wait state as shown in Table 8.9. Address bits A11-A0 should be set to 555h, while addresses bits A17-A12 set the wait state. For further details, see Section 8.3, *Set Configuration Register Command Sequence* on page 36.

7.3.1 Handshaking Feature

The handshaking feature allows the host system to simply monitor the RDY signal from the device to determine when the initial word of burst data is ready to be read. The host system should use the wait state command sequence to set the number of wait states for optimal burst mode operation (03h for 54 MHz clock). The initial word of burst data is indicated by the rising edge of RDY after OE# goes low.

7.4 Simultaneous Read/Write Operations with Zero Latency

This device is capable of reading data from one bank of memory while programming or erasing in one of the other three banks of memory. An erase operation may also be suspended to read from or program to another location within the same bank (except the sector being erased). Figure 14.16 shows how read and write cycles may be initiated for simultaneous operation with zero latency. Refer to the Section 11., *DC Characteristics* on page 51 table for read-while-program and read-while-erase current specifications.

7.5 Writing Commands/Command Sequences

The device has inputs/outputs that accept both address and data information. To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive AVD# and CE# to V_{IL}, and OE# to V_{IH} when providing an address to the device, and drive WE# and CE# to V_{IL}, and OE# to V_{IH}. when writing commands or data.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 7 indicates the address space that each sector occupies. The device address space is divided into four banks: Bank A contains both 8 Kword boot sectors in addition to 32 Kword sectors, while Banks B, C, and D contain only 32 Kword sectors. A “bank address” is the address bits required to uniquely select a bank. Similarly, a “sector address” is the address bits required to uniquely select a sector.

Refer to the DC Characteristics table for write mode current specifications. The *AC Characteristics* section contains timing specification tables and timing diagrams for write operations.

7.5.1 Accelerated Program Operation

The device offers accelerated program operations through the A_{cc} input. This function is primarily intended to allow faster manufacturing throughput at the factory. If the system asserts V_{ID} on this input, the device automatically enters the aforementioned Unlock Bypass mode and uses the higher voltage on the input to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{ID} from the A_{cc} input returns the device to normal operation.

7.5.2 Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. See Section 7.5.2, *Autoselect Functions* on page 21 and Section 8.6, *Autoselect Command Sequence* on page 38 for more information.

7.6 Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# inputs are both held at V_{CC} ± 0.2 V. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in *DC Characteristics* represents the standby current specification.

7.7 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enters this mode when addresses remain stable for t_{ACC} + 60 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in *DC Characteristics* represents the automatic sleep mode current specification.

7.8 RESET#: Hardware Reset Input

The RESET# input provides a hardware method of resetting the device to reading array data. When RESET# is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all outputs, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.2 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}±0.2 V, the standby current will be greater.

RESET# may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the device requires a time of t_{READYW} (during Embedded Algorithms) before the device is ready to read data again. If RESET# is asserted when a program or erase operation is not executing, the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after RESET# returns to V_{IH}.

Refer to the *AC Characteristics* tables for RESET# parameters and to Figure 14.6 for the timing diagram.

7.8.1 V_{CC} Power-up and Power-down Sequencing

The device imposes no restrictions on V_{CC} power-up or power-down sequencing. Asserting RESET# to V_{IL} is required during the entire V_{CC} power sequence until the respective supplies reach their operating voltages. Once V_{CC} attains its operating voltage, de-assertion of RESET# to V_{IH} is permitted.

7.9 Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The outputs are placed in the high impedance state.

7.10 Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 8.16 for command definitions).

The device offers three types of data protection at the sector level:

- The sector lock/unlock command sequence disables or re-enables both program and erase operations in any sector.

- When WP# is at V_{IL},
  - SA257 and SA258 are locked (S29NS128J)
  - SA129 and SA130 are locked (S29NS064J)
  - SA65 and SA66 are locked (S29NS032J)
  - SA33 and SA34 are locked (S29NS016J)
- When A_{cc} is at V_{IL}, all sectors are locked.

7.11 WP# Boot Sector Protection

The WP# signal will be latched at a specific time in the embedded program or erase sequence. To prevent a write to the top two sectors, WP# must be asserted (WP#=V_{IL}) on the last write cycle of the embedded sequence (i.e., 4th write cycle in embedded program, 6th write cycle in embedded erase).

If using the Unlock Bypass feature: on the 2nd program cycle, after the Unlock Bypass command is written, the WP# signal must be asserted on the 2nd cycle.

If selecting multiple sectors for erasure: The WP# protection status is latched only on the 6th write cycle of the embedded sector erase command sequence when the first sector is selected. If additional sectors are selected for erasure, they are subject to the WP# status that was latched on the 6th write cycle of the command sequence.

The following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

7.11.1 Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control inputs to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

7.11.2 Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

7.11.3 Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

8. Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 8.1–8.4. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 8.1–8.4. The system must write the reset command to return the device to the autoselect mode.

For further information, please refer to the CFI Specification and CFI Publication 100, available through the World Wide Web at http://www.amd.com/flash/cfi. Alternatively, Contact your local Spansion sales office for copies of these documents.

Table 8.1 CFI Query Identification String

Addresses	Data				Description
	S29NS128J	S29NS064J	S29NS032J	S29NS016J	
10h 11h 12h	0051h 0052h 0059h				Query Unique ASCII string “QRY”
13h 14h	0002h 0000h				Primary OEM Command Set
15h 16h	0040h 0000h				Address for Primary Extended Table
17h 18h	0000h 0000h				Alternate OEM Command Set (00h = none exists)
19h 1Ah	0000h 0000h				Address for Alternate OEM Extended Table (00h = none exists)

Table 8.2 System Interface String

Addresses	Data				Description
	S29NS128J	S29NS064J	S29NS032J	S29NS016J	
1Bh	0017h				V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	0019h				V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	0000h				A_{cc} Min. voltage (00h = no A_{cc} pin present) Refer to 4Dh
1Eh	0000h				A_{cc} Max. voltage (00h = no A_{cc} pin present) Refer to 4Eh
1Fh	0003h				Typical timeout per single byte/word write 2^N µs
20h	0000h				Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	0009h				Typical timeout per individual block erase 2^N ms
22h	0000h				Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0005h				Max. timeout for byte/word write 2^N times typical
24h	0000h				Max. timeout for buffer write 2^N times typical
25h	0004h				Max. timeout per individual block erase 2^N times typical
26h	0000h				Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 8.3 Device Geometry Definition

Addresses	Data				Description
	S29NS128J	S29NS064J	S29NS032J	S29NS016J	
27h	0018h	0017h	0016h	0015h	Device Size = 2^N byte
28h 29h	0001h 0000h				Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	0000h 0000h				Max. number of bytes in multi-byte write = 2^N (00h = not supported)
2Ch	0002h				Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	00FEh 0000h 0000h 0001h	007Eh 0000h 0000h 0001h	003Eh 0000h 0000h 0001h	001Eh 0000h 0000h 0001h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	0003h 0000h 0040h 0000h				Erase Block Region 2 Information
35h 36h 37h 38h	0000h 0000h 0000h 0000h				Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h				Erase Block Region 4 Information

Table 8.4 Primary Vendor-Specific Extended Query (Sheet 1 of 2)

Addresses	Data				Description
	S29NS128J	S29NS064J	S29NS032J	S29NS016J	
40h 41h 42h	0050h 0052h 0049h				Query-unique ASCII string “PRI”
43h	0031h				Major version number, ASCII
44h	0033h				Minor version number, ASCII
45h	0000h				Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Silicon Revision Number (Bits 7-2)
46h	0002h				Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0001h				Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0000h				Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0005h				Sector Protect/Unprotect scheme 05 = 29BDS/N128 mode
4Ah	00C0h	0060h	0030h	0018h	Simultaneous Operation Number of Sectors in all banks except boot bank
4Bh	0001h				Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0000h				Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	00B5h				ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	00C5h				ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	0003h				Top/Bottom Boot Sector Flag 0001h = Top/Middle Boot Device, 0002h = Bottom Boot Device, 03h = Top Boot Device
50h	0000h				Program Suspend. 00h = not supported
57h	0004h				Bank Organization: X = Number of banks

Table 8.4 Primary Vendor-Specific Extended Query (Sheet 2 of 2)

Addresses	Data				Description
	S29NS128J	S29NS064J	S29NS032J	S29NS016J	
58h	0040h	0020h	0010h	0008h	Bank D Region Information. X = Number of sectors in bank
59h	0040h	0020h	0010h	0008h	Bank C Region Information. X = Number of sectors in bank
5Ah	0040h	0020h	0010h	0008h	Bank B Region Information. X = Number of sectors in bank
5Bh	0043h	0023h	0013h	0008h	Bank A Region Information. X = Number of sectors in bank
5Ch	0002h				Process Technology. 00h = 230 nm, 01h = 170 nm, 02h = 130 nm/110 nm

Table 8.5 Sector Address Table, S29NS128J (Sheet 1 of 4)

	Sector	Sector Size	Address Range	Sector	Sector Size	Address Range
Bank D	SA0	32 Kwords	000000h–007FFFh	SA32	32 Kwords	100000h–107FFFh
	SA1	32 Kwords	008000h–00FFFFh	SA33	32 Kwords	108000h–10FFFFh
	SA2	32 Kwords	010000h–017FFFh	SA34	32 Kwords	110000h–117FFFh
	SA3	32 Kwords	018000h–01FFFFh	SA35	32 Kwords	118000h–11FFFFh
	SA4	32 Kwords	020000h–027FFFh	SA36	32 Kwords	120000h–127FFFh
	SA5	32 Kwords	028000h–02FFFFh	SA37	32 Kwords	128000h–12FFFFh
	SA6	32 Kwords	030000h–037FFFh	SA38	32 Kwords	130000h–137FFFh
	SA7	32 Kwords	038000h–03FFFFh	SA39	32 Kwords	138000h–13FFFFh
	SA8	32 Kwords	040000h–047FFFh	SA40	32 Kwords	140000h–147FFFh
	SA9	32 Kwords	048000h–04FFFFh	SA41	32 Kwords	148000h–14FFFFh
	SA10	32 Kwords	050000h–057FFFh	SA42	32 Kwords	150000h–157FFFh
	SA11	32 Kwords	058000h–05FFFFh	SA43	32 Kwords	158000h–15FFFFh
	SA12	32 Kwords	060000h–067FFFh	SA44	32 Kwords	160000h–167FFFh
	SA13	32 Kwords	068000h–06FFFFh	SA45	32 Kwords	168000h–16FFFFh
	SA14	32 Kwords	070000h–077FFFh	SA46	32 Kwords	170000h–177FFFh
	SA15	32 Kwords	078000h–07FFFFh	SA47	32 Kwords	178000h–17FFFFh
	SA16	32 Kwords	080000h–087FFFh	SA48	32 Kwords	180000h–187FFFh
	SA17	32 Kwords	088000h–08FFFFh	SA49	32 Kwords	188000h–18FFFFh
	SA18	32 Kwords	090000h–097FFFh	SA50	32 Kwords	190000h–197FFFh
	SA19	32 Kwords	098000h–09FFFFh	SA51	32 Kwords	198000h–19FFFFh
	SA20	32 Kwords	0A0000h–0A7FFFh	SA52	32 Kwords	1A0000h–1A7FFFh
	SA21	32 Kwords	0A8000h–0AFFFFh	SA53	32 Kwords	1A8000h–1AFFFFh
	SA22	32 Kwords	0B0000h–0B7FFFh	SA54	32 Kwords	1B0000h–1B7FFFh
	SA23	32 Kwords	0B8000h–0BFFFFh	SA55	32 Kwords	1B8000h–1BFFFFh
	SA24	32 Kwords	0C0000h–0C7FFFh	SA56	32 Kwords	1C0000h–1C7FFFh
	SA25	32 Kwords	0C8000h–0CFFFFh	SA57	32 Kwords	1C8000h–1CFFFFh
	SA26	32 Kwords	0D0000h–0D7FFFh	SA58	32 Kwords	1D0000h–1D7FFFh
	SA27	32 Kwords	0D8000h–0DFFFFh	SA59	32 Kwords	1D8000h–1DFFFFh
	SA28	32 Kwords	0E0000h–0E7FFFh	SA60	32 Kwords	1E0000h–1E7FFFh
	SA29	32 Kwords	0E8000h–0EFFFFh	SA61	32 Kwords	1E8000h–1EFFFFh
	SA30	32 Kwords	0F0000h–0F7FFFh	SA62	32 Kwords	1F0000h–1F7FFFh
	SA31	32 Kwords	0F8000h–0FFFFFh	SA63	32 Kwords	1F8000h–1FFFFFh

Table 8.5 Sector Address Table, S29NS128J (Sheet 2 of 4)

	Sector	Sector Size	Address Range	Sector	Sector Size	Address Range
Bank C	SA64	32 Kwords	200000h–207FFFh	SA96	32 Kwords	300000h–307FFFh
	SA65	32 Kwords	208000h–20FFFFh	SA97	32 Kwords	308000h–30FFFFh
	SA66	32 Kwords	210000h–217FFFh	SA98	32 Kwords	310000h–317FFFh
	SA67	32 Kwords	218000h–21FFFFh	SA99	32 Kwords	318000h–31FFFFh
	SA68	32 Kwords	220000h–227FFFh	SA100	32 Kwords	320000h–327FFFh
	SA69	32 Kwords	228000h–22FFFFh	SA101	32 Kwords	328000h–32FFFFh
	SA70	32 Kwords	230000h–237FFFh	SA102	32 Kwords	330000h–337FFFh
	SA71	32 Kwords	238000h–23FFFFh	SA103	32 Kwords	338000h–33FFFFh
	SA72	32 Kwords	240000h–247FFFh	SA104	32 Kwords	340000h–347FFFh
	SA73	32 Kwords	248000h–24FFFFh	SA105	32 Kwords	348000h–34FFFFh
	SA74	32 Kwords	250000h–257FFFh	SA106	32 Kwords	350000h–357FFFh
	SA75	32 Kwords	258000h–25FFFFh	SA107	32 Kwords	358000h–35FFFFh
	SA76	32 Kwords	260000h–267FFFh	SA108	32 Kwords	360000h–367FFFh
	SA77	32 Kwords	268000h–26FFFFh	SA109	32 Kwords	368000h–36FFFFh
	SA78	32 Kwords	270000h–277FFFh	SA110	32 Kwords	370000h–377FFFh
	SA79	32 Kwords	278000h–27FFFFh	SA111	32 Kwords	378000h–37FFFFh
	SA80	32 Kwords	280000h–287FFFh	SA112	32 Kwords	380000h–387FFFh
	SA81	32 Kwords	288000h–28FFFFh	SA113	32 Kwords	388000h–38FFFFh
	SA82	32 Kwords	290000h–297FFFh	SA114	32 Kwords	390000h–397FFFh
	SA83	32 Kwords	298000h–29FFFFh	SA115	32 Kwords	398000h–39FFFFh
	SA84	32 Kwords	2A0000h–2A7FFFh	SA116	32 Kwords	3A0000h–3A7FFFh
	SA85	32 Kwords	2A8000h–2AFFFFh	SA117	32 Kwords	3A8000h–3AFFFFh
	SA86	32 Kwords	2B0000h–2B7FFFh	SA118	32 Kwords	3B0000h–3B7FFFh
	SA87	32 Kwords	2B8000h–2BFFFFh	SA119	32 Kwords	3B8000h–3BFFFFh
	SA88	32 Kwords	2C0000h–2C7FFFh	SA120	32 Kwords	3C0000h–3C7FFFh
	SA89	32 Kwords	2C8000h–2CFFFFh	SA121	32 Kwords	3C8000h–3CFFFFh
	SA90	32 Kwords	2D0000h–2D7FFFh	SA122	32 Kwords	3D0000h–3D7FFFh
	SA91	32 Kwords	2D8000h–2DFFFFh	SA123	32 Kwords	3D8000h–3DFFFFh
	SA92	32 Kwords	2E0000h–2E7FFFh	SA124	32 Kwords	3E0000h–3E7FFFh
	SA93	32 Kwords	2E8000h–2EFFFFh	SA125	32 Kwords	3E8000h–3EFFFFh
	SA94	32 Kwords	2F0000h–2F7FFFh	SA126	32 Kwords	3F0000h–3F7FFFh
	SA95	32 Kwords	2F8000h–2FFFFFh	SA127	32 Kwords	3F8000h–3FFFFFh

Table 8.5 Sector Address Table, S29NS128J (Sheet 3 of 4)

	Sector	Sector Size	Address Range	Sector	Sector Size	Address Range
Bank B	SA128	32 Kwords	400000h–407FFFh	SA160	32 Kwords	500000h–507FFFh
	SA129	32 Kwords	408000h–40FFFFh	SA161	32 Kwords	508000h–50FFFFh
	SA130	32 Kwords	410000h–417FFFh	SA162	32 Kwords	510000h–517FFFh
	SA131	32 Kwords	418000h–41FFFFh	SA163	32 Kwords	518000h–51FFFFh
	SA132	32 Kwords	420000h–427FFFh	SA164	32 Kwords	520000h–527FFFh
	SA133	32 Kwords	428000h–42FFFFh	SA165	32 Kwords	528000h–52FFFFh
	SA134	32 Kwords	420000h–427FFFh	SA166	32 Kwords	530000h–537FFFh
	SA135	32 Kwords	438000h–43FFFFh	SA167	32 Kwords	538000h–53FFFFh
	SA136	32 Kwords	430000h–437FFFh	SA168	32 Kwords	540000h–547FFFh
	SA137	32 Kwords	448000h–44FFFFh	SA169	32 Kwords	548000h–54FFFFh
	SA138	32 Kwords	450000h–457FFFh	SA170	32 Kwords	550000h–557FFFh
	SA139	32 Kwords	458000h–45FFFFh	SA171	32 Kwords	558000h–55FFFFh
	SA140	32 Kwords	460000h–467FFFh	SA172	32 Kwords	560000h–567FFFh
	SA141	32 Kwords	468000h–46FFFFh	SA173	32 Kwords	568000h–56FFFFh
	SA142	32 Kwords	470000h–477FFFh	SA174	32 Kwords	570000h–577FFFh
	SA143	32 Kwords	478000h–47FFFFh	SA175	32 Kwords	578000h–57FFFFh
	SA144	32 Kwords	480000h–487FFFh	SA176	32 Kwords	580000h–587FFFh
	SA145	32 Kwords	488000h–48FFFFh	SA177	32 Kwords	588000h–58FFFFh
	SA146	32 Kwords	490000h–497FFFh	SA178	32 Kwords	590000h–597FFFh
	SA147	32 Kwords	498000h–49FFFFh	SA179	32 Kwords	598000h–59FFFFh
	SA148	32 Kwords	4A0000h–4A7FFFh	SA180	32 Kwords	5A0000h–5A7FFFh
	SA149	32 Kwords	4A8000h–4AFFFFh	SA181	32 Kwords	5A8000h–5AFFFFh
	SA150	32 Kwords	4B0000h–4B7FFFh	SA182	32 Kwords	5B0000h–5B7FFFh
	SA151	32 Kwords	4B8000h–4BFFFFh	SA183	32 Kwords	5B8000h–5BFFFFh
	SA152	32 Kwords	4C0000h–4C7FFFh	SA184	32 Kwords	5C0000h–5C7FFFh
	SA153	32 Kwords	4C8000h–4CFFFFh	SA185	32 Kwords	5C8000h–5CFFFFh
	SA154	32 Kwords	4D0000h–4D7FFFh	SA186	32 Kwords	5D0000h–5D7FFFh
	SA155	32 Kwords	4D8000h–4DFFFFh	SA187	32 Kwords	5D8000h–5DFFFFh
	SA156	32 Kwords	4E0000h–4E7FFFh	SA188	32 Kwords	5E0000h–5E7FFFh
	SA157	32 Kwords	4E8000h–4EFFFFh	SA189	32 Kwords	5E8000h–5EFFFFh
	SA158	32 Kwords	4F0000h–4F7FFFh	SA190	32 Kwords	5F0000h–5F7FFFh
	SA159	32 Kwords	4F8000h–4FFFFFh	SA191	32 Kwords	5F8000h–5FFFFFh

Table 8.5 Sector Address Table, S29NS128J (Sheet 4 of 4)

	Sector	Sector Size	Address Range
Bank A	SA192	32 Kwords	600000h–607FFFh
	SA193	32 Kwords	608000h–60FFFFh
	SA194	32 Kwords	610000h–617FFFh
	SA195	32 Kwords	618000h–61FFFFh
	SA196	32 Kwords	620000h–627FFFh
	SA197	32 Kwords	628000h–62FFFFh
	SA198	32 Kwords	630000h–637FFFh
	SA199	32 Kwords	638000h–63FFFFh
	SA200	32 Kwords	640000h–647FFFh
	SA201	32 Kwords	648000h–64FFFFh
	SA202	32 Kwords	650000h–657FFFh
	SA203	32 Kwords	658000h–65FFFFh
	SA204	32 Kwords	660000h–667FFFh
	SA205	32 Kwords	668000h–66FFFFh
	SA206	32 Kwords	670000h–677FFFh
	SA207	32 Kwords	678000h–67FFFFh
	SA208	32 Kwords	680000h–687FFFh
	SA209	32 Kwords	688000h–68FFFFh
	SA210	32 Kwords	690000h–697FFFh
	SA211	32 Kwords	698000h–69FFFFh
	SA212	32 Kwords	6A0000h–6A7FFFh
	SA213	32 Kwords	6A8000h–6AFFFFh
	SA214	32 Kwords	6B0000h–6B7FFFh
	SA215	32 Kwords	6B8000h–6BFFFFh
	SA216	32 Kwords	6C0000h–6C7FFFh
	SA217	32 Kwords	6C8000h–6CFFFFh
	SA218	32 Kwords	6D0000h–6D7FFFh
	SA219	32 Kwords	6D8000h–6DFFFFh
	SA220	32 Kwords	6E0000h–6E7FFFh
	SA221	32 Kwords	6E8000h–6EFFFFh
	SA222	32 Kwords	6F0000h–6F7FFFh
	SA223	32 Kwords	6F8000h–6FFFFFh

Sector	Sector Size	Address Range
SA224	32 Kwords	700000h–707FFFh
SA225	32 Kwords	708000h–70FFFFh
SA226	32 Kwords	710000h–717FFFh
SA227	32 Kwords	718000h–71FFFFh
SA228	32 Kwords	720000h–727FFFh
SA229	32 Kwords	728000h–72FFFFh
SA230	32 Kwords	730000h–737FFFh
SA231	32 Kwords	738000h–73FFFFh
SA232	32 Kwords	740000h–747FFFh
SA233	32 Kwords	748000h–74FFFFh
SA234	32 Kwords	750000h–757FFFh
SA235	32 Kwords	758000h–75FFFFh
SA236	32 Kwords	760000h–767FFFh
SA237	32 Kwords	768000h–76FFFFh
SA238	32 Kwords	770000h–777FFFh
SA239	32 Kwords	778000h–77FFFFh
SA240	32 Kwords	780000h–787FFFh
SA241	32 Kwords	788000h–78FFFFh
SA242	32 Kwords	790000h–797FFFh
SA243	32 Kwords	798000h–79FFFFh
SA244	32 Kwords	7A0000h–7A7FFFh
SA245	32 Kwords	7A8000h–7AFFFFh
SA246	32 Kwords	7B0000h–7B7FFFh
SA247	32 Kwords	7B8000h–7BFFFFh
SA248	32 Kwords	7C0000h–7C7FFFh
SA249	32 Kwords	7C8000h–7CFFFFh
SA250	32 Kwords	7D0000h–7D7FFFh
SA251	32 Kwords	7D8000h–7DFFFFh
SA252	32 Kwords	7E0000h–7E7FFFh
SA253	32 Kwords	7E8000h–7EFFFFh
SA254	32 Kwords	7F0000h–7F7FFFh
SA255	8 Kwords	7F8000h–7F9FFFh
SA256	8 Kwords	7FA000h–7FBFFFh
SA257	8 Kwords	7FC000h–7FDFFFh
SA258	8 Kwords	7FE000h–7FFFFFh

Table 8.6 Sector Address Table, S29NS064J (Sheet 1 of 4)

	Sector	Sector Size	Address Range
Bank D	SA0	32 Kwords	000000h–007FFFh
	SA1	32 Kwords	008000h–00FFFFh
	SA2	32 Kwords	010000h–017FFFh
	SA3	32 Kwords	018000h–01FFFFh
	SA4	32 Kwords	020000h–027FFFh
	SA5	32 Kwords	028000h–02FFFFh
	SA6	32 Kwords	030000h–037FFFh
	SA7	32 Kwords	038000h–03FFFFh
	SA8	32 Kwords	040000h–047FFFh
	SA9	32 Kwords	048000h–04FFFFh
	SA10	32 Kwords	050000h–057FFFh
	SA11	32 Kwords	058000h–05FFFFh
	SA12	32 Kwords	060000h–067FFFh
	SA13	32 Kwords	068000h–06FFFFh
	SA14	32 Kwords	070000h–077FFFh
	SA15	32 Kwords	078000h–07FFFFh
	SA16	32 Kwords	080000h–087FFFh
	SA17	32 Kwords	088000h–08FFFFh
	SA18	32 Kwords	090000h–097FFFh
	SA19	32 Kwords	098000h–09FFFFh
	SA20	32 Kwords	0A0000h–0A7FFFh
	SA21	32 Kwords	0A8000h–0AFFFFh
	SA22	32 Kwords	0B0000h–0B7FFFh
	SA23	32 Kwords	0B8000h–0BFFFFh
	SA24	32 Kwords	0C0000h–0C7FFFh
	SA25	32 Kwords	0C8000h–0CFFFFh
	SA26	32 Kwords	0D0000h–0D7FFFh
	SA27	32 Kwords	0D8000h–0DFFFFh
	SA28	32 Kwords	0E0000h–0E7FFFh
	SA29	32 Kwords	0E8000h–0EFFFFh
	SA30	32 Kwords	0F0000h–0F7FFFh
	SA31	32 Kwords	0F8000h–0FFFFFh

Table 8.6 Sector Address Table, S29NS064J (Sheet 2 of 4)

	Sector	Sector Size	Address Range
Bank C	SA32	32 Kwords	100000h–107FFFh
	SA33	32 Kwords	108000h–10FFFFh
	SA34	32 Kwords	110000h–117FFFh
	SA35	32 Kwords	118000h–11FFFFh
	SA36	32 Kwords	120000h–127FFFh
	SA37	32 Kwords	128000h–12FFFFh
	SA38	32 Kwords	130000h–137FFFh
	SA39	32 Kwords	138000h–13FFFFh
	SA40	32 Kwords	140000h–147FFFh
	SA41	32 Kwords	148000h–14FFFFh
	SA42	32 Kwords	150000h–157FFFh
	SA43	32 Kwords	158000h–15FFFFh
	SA44	32 Kwords	160000h–167FFFh
	SA45	32 Kwords	168000h–16FFFFh
	SA46	32 Kwords	170000h–177FFFh
	SA47	32 Kwords	178000h–17FFFFh
	SA48	32 Kwords	180000h–187FFFh
	SA49	32 Kwords	188000h–18FFFFh
	SA50	32 Kwords	190000h–197FFFh
	SA51	32 Kwords	198000h–19FFFFh
	SA52	32 Kwords	1A0000h–1A7FFFh
	SA53	32 Kwords	1A8000h–1AFFFFh
	SA54	32 Kwords	1B0000h–1B7FFFh
	SA55	32 Kwords	1B8000h–1BFFFFh
	SA56	32 Kwords	1C0000h–1C7FFFh
	SA57	32 Kwords	1C8000h–1CFFFFh
	SA58	32 Kwords	1D0000h–1D7FFFh
	SA59	32 Kwords	1D8000h–1DFFFFh
	SA60	32 Kwords	1E0000h–1E7FFFh
	SA61	32 Kwords	1E8000h–1EFFFFh
	SA62	32 Kwords	1F0000h–1F7FFFh
	SA63	32 Kwords	1F8000h–1FFFFFh

Table 8.6 Sector Address Table, S29NS064J (Sheet 3 of 4)

	Sector	Sector Size	Address Range
Bank B	SA64	32 Kwords	200000h–207FFFh
	SA65	32 Kwords	208000h–20FFFFh
	SA66	32 Kwords	210000h–217FFFh
	SA67	32 Kwords	218000h–21FFFFh
	SA68	32 Kwords	220000h–227FFFh
	SA69	32 Kwords	228000h–22FFFFh
	SA70	32 Kwords	230000h–237FFFh
	SA71	32 Kwords	238000h–23FFFFh
	SA72	32 Kwords	240000h–247FFFh
	SA73	32 Kwords	248000h–24FFFFh
	SA74	32 Kwords	250000h–257FFFh
	SA75	32 Kwords	258000h–25FFFFh
	SA76	32 Kwords	260000h–267FFFh
	SA77	32 Kwords	268000h–26FFFFh
	SA78	32 Kwords	270000h–277FFFh
	SA79	32 Kwords	278000h–27FFFFh
	SA80	32 Kwords	280000h–287FFFh
	SA81	32 Kwords	288000h–28FFFFh
	SA82	32 Kwords	290000h–297FFFh
	SA83	32 Kwords	298000h–29FFFFh
	SA84	32 Kwords	2A0000h–2A7FFFh
	SA85	32 Kwords	2A8000h–2AFFFFh
	SA86	32 Kwords	2B0000h–2B7FFFh
	SA87	32 Kwords	2B8000h–2BFFFFh
	SA88	32 Kwords	2C0000h–2C7FFFh
	SA89	32 Kwords	2C8000h–2CFFFFh
	SA90	32 Kwords	2D0000h–2D7FFFh
	SA91	32 Kwords	2D8000h–2DFFFFh
	SA92	32 Kwords	2E0000h–2E7FFFh
	SA93	32 Kwords	2E8000h–2EFFFFh
	SA94	32 Kwords	2F0000h–2F7FFFh
	SA95	32 Kwords	2F8000h–2FFFFFh

Table 8.6 Sector Address Table, S29NS064J (Sheet 4 of 4)

	Sector	Sector Size	Address Range
Bank A	SA96	32 Kwords	300000h–307FFFh
	SA97	32 Kwords	308000h–30FFFFh
	SA98	32 Kwords	310000h–317FFFh
	SA99	32 Kwords	318000h–31FFFFh
	SA100	32 Kwords	320000h–327FFFh
	SA101	32 Kwords	328000h–32FFFFh
	SA102	32 Kwords	330000h–337FFFh
	SA103	32 Kwords	338000h–33FFFFh
	SA104	32 Kwords	340000h–347FFFh
	SA105	32 Kwords	348000h–34FFFFh
	SA106	32 Kwords	350000h–357FFFh
	SA107	32 Kwords	358000h–35FFFFh
	SA108	32 Kwords	360000h–367FFFh
	SA109	32 Kwords	368000h–36FFFFh
	SA110	32 Kwords	370000h–377FFFh
	SA111	32 Kwords	378000h–37FFFFh
	SA112	32 Kwords	380000h–387FFFh
	SA113	32 Kwords	388000h–38FFFFh
	SA114	32 Kwords	390000h–397FFFh
	SA115	32 Kwords	398000h–39FFFFh
	SA116	32 Kwords	3A0000h–3A7FFFh
	SA117	32 Kwords	3A8000h–3AFFFFh
	SA118	32 Kwords	3B0000h–3B7FFFh
	SA119	32 Kwords	3B8000h–3BFFFFh
	SA120	32 Kwords	3C0000h–3C7FFFh
	SA121	32 Kwords	3C8000h–3CFFFFh
	SA122	32 Kwords	3D0000h–3D7FFFh
	SA123	32 Kwords	3D8000h–3DFFFFh
	SA124	32 Kwords	3E0000h–3E7FFFh
	SA125	32 Kwords	3E8000h–3EFFFFh
	SA126	32 Kwords	3F0000h–3F7FFFh
	SA127	8 Kwords	3F8000h–3F9FFFh
	SA128	8 Kwords	3FA000h–3FBFFFh
	SA129	8 Kwords	3FC000h–3FDFFFh
	SA130	8 Kwords	3FE000h–3FFFFFh

Table 8.7 Sector Address Table, S29NS032J (Sheet 1 of 2)

	Sector	Sector Size	Address Range
Bank D	SA0	32 Kwords	000000h–007FFFh
	SA1	32 Kwords	008000h–00FFFFh
	SA2	32 Kwords	010000h–017FFFh
	SA3	32 Kwords	018000h–01FFFFh
	SA4	32 Kwords	020000h–027FFFh
	SA5	32 Kwords	028000h–02FFFFh
	SA6	32 Kwords	030000h–037FFFh
	SA7	32 Kwords	038000h–03FFFFh
	SA8	32 Kwords	040000h–047FFFh
	SA9	32 Kwords	048000h–04FFFFh
	SA10	32 Kwords	050000h–057FFFh
	SA11	32 Kwords	058000h–05FFFFh
	SA12	32 Kwords	060000h–067FFFh
	SA13	32 Kwords	068000h–06FFFFh
	SA14	32 Kwords	070000h–077FFFh
	SA15	32 Kwords	078000h–07FFFFh
Bank C	SA16	32 Kwords	080000h–087FFFh
	SA17	32 Kwords	088000h–08FFFFh
	SA18	32 Kwords	090000h–097FFFh
	SA19	32 Kwords	098000h–09FFFFh
	SA20	32 Kwords	0A0000h–0A7FFFh
	SA21	32 Kwords	0A8000h–0AFFFFh
	SA22	32 Kwords	0B0000h–0B7FFFh
	SA23	32 Kwords	0B8000h–0BFFFFh
	SA24	32 Kwords	0C0000h–0C7FFFh
	SA25	32 Kwords	0C8000h–0CFFFFh
	SA26	32 Kwords	0D0000h–0D7FFFh
	SA27	32 Kwords	0D8000h–0DFFFFh
	SA28	32 Kwords	0E0000h–0E7FFFh
	SA29	32 Kwords	0E8000h–0EFFFFh
	SA30	32 Kwords	0F0000h–0F7FFFh
	SA31	32 Kwords	0F8000h–0FFFFFh
Bank B	SA32	32 Kwords	100000h–107FFFh
	SA33	32 Kwords	108000h–10FFFFh
	SA34	32 Kwords	110000h–117FFFh
	SA35	32 Kwords	118000h–11FFFFh
	SA36	32 Kwords	120000h–127FFFh
	SA37	32 Kwords	128000h–12FFFFh
	SA38	32 Kwords	130000h–137FFFh
	SA39	32 Kwords	138000h–13FFFFh
	SA40	32 Kwords	140000h–147FFFh
	SA41	32 Kwords	148000h–14FFFFh
	SA42	32 Kwords	150000h–157FFFh
	SA43	32 Kwords	158000h–15FFFFh
	SA44	32 Kwords	160000h–167FFFh
	SA45	32 Kwords	168000h–16FFFFh
	SA46	32 Kwords	170000h–177FFFh
	SA47	32 Kwords	178000h–17FFFFh

Table 8.7 Sector Address Table, S29NS032J (Sheet 2 of 2)

	Sector	Sector Size	Address Range
Bank A	SA48	32 Kwords	180000h–187FFFh
	SA49	32 Kwords	188000h–18FFFFh
	SA50	32 Kwords	190000h–197FFFh
	SA51	32 Kwords	198000h–19FFFFh
	SA52	32 Kwords	1A0000h–1A7FFFh
	SA53	32 Kwords	1A8000h–1AFFFFh
	SA54	32 Kwords	1B0000h–1B7FFFh
	SA55	32 Kwords	1B8000h–1BFFFFh
	SA56	32 Kwords	1C0000h–1C7FFFh
	SA57	32 Kwords	1C8000h–1CFFFFh
	SA58	32 Kwords	1D0000h–1D7FFFh
	SA59	32 Kwords	1D8000h–1DFFFFh
	SA60	32 Kwords	1E0000h–1E7FFFh
	SA61	32 Kwords	1E8000h–1EFFFFh
	SA62	32 Kwords	1F0000h–1F7FFFh
	SA63	8 Kwords	1F8000h–1F9FFFh
	SA64	8 Kwords	1FA000h–1FBFFFh
	SA65	8 Kwords	1FC000h–1FDFFFh
	SA66	8 Kwords	1FE000h–1FFFFFh

Table 8.8 Sector Address Table, S29NS016J (Sheet 1 of 2)

	Sector	Sector Size	Address Range
Bank D	SA0	32 Kwords	000000h–007FFFh
	SA1	32 Kwords	008000h–00FFFFh
	SA2	32 Kwords	010000h–017FFFh
	SA3	32 Kwords	018000h–01FFFFh
	SA4	32 Kwords	020000h–027FFFh
	SA5	32 Kwords	028000h–02FFFFh
	SA6	32 Kwords	030000h–037FFFh
	SA7	32 Kwords	038000h–03FFFFh
Bank C	SA8	32 Kwords	040000h–047FFFh
	SA9	32 Kwords	048000h–04FFFFh
	SA10	32 Kwords	050000h–057FFFh
	SA11	32 Kwords	058000h–05FFFFh
	SA12	32 Kwords	060000h–067FFFh
	SA13	32 Kwords	068000h–06FFFFh
	SA14	32 Kwords	070000h–077FFFh
	SA15	32 Kwords	078000h–07FFFFh
Bank B	SA16	32 Kwords	080000h–087FFFh
	SA17	32 Kwords	088000h–08FFFFh
	SA18	32 Kwords	090000h–097FFFh
	SA19	32 Kwords	098000h–09FFFFh
	SA20	32 Kwords	0A0000h–0A7FFFh
	SA21	32 Kwords	0A8000h–0AFFFFh
	SA22	32 Kwords	0B0000h–0B7FFFh
	SA23	32 Kwords	0B8000h–0BFFFFh

Table 8.8 Sector Address Table, S29NS016J (Sheet 2 of 2)

	Sector	Sector Size	Address Range
Bank A	SA24	32 Kwords	0C0000h–0C7FFFh
	SA25	32 Kwords	0C8000h–0CFFFFh
	SA26	32 Kwords	0D0000h–0D7FFFh
	SA27	32 Kwords	0D8000h–0DFFFFh
	SA28	32 Kwords	0E0000h–0E7FFFh
	SA29	32 Kwords	0E8000h–0EFFFFh
	SA30	32 Kwords	0F0000h–0F7FFFh
	SA31	8 Kwords	0F8000h–0F9FFFh
	SA32	8 Kwords	0FA000h–0FBFFFh
	SA33	8 Kwords	0FC000h–0FDFFFh
	SA34	8 Kwords	0FE000h–0FFFFFh

8.1 Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table 8.16 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the rising edge of AVD#. All data is latched on the rising edge of WE#. Refer to the *AC Characteristics* section for timing diagrams.

8.2 Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data in asynchronous mode. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the *Erase Suspend/Erase Resume Commands* section for more information.

The system *must* issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See the next section, *Reset Command*, for more information.

See also *Requirements for Asynchronous Read Operation (Non-Burst)* and *Requirements for Synchronous (Burst) Read Operation* in the *Device Bus Operations* section for more information. The *Asynchronous Read* and *Synchronous/Burst Read* tables provide the read parameters, and Figures 14.3 and 14.5 show the timings.

8.3 Set Configuration Register Command Sequence

The configuration register command sequence instructs the device to set a particular number of clock cycles for the initial access in burst mode. The number of wait states that should be programmed into the device is directly related to the clock frequency. The first two cycles of the command sequence are for unlock purposes. On the third cycle, the system should write C0h to the address associated with the intended wait state setting (see Table 8.9). Address bits A17–A12 determine the setting. Note that addresses A_{max}–A18 are shown as “0” but are actually don’t care.

Table 8.9 Burst Modes (Sheet 1 of 2)

Burst Mode	Third Cycle Addresses for Wait States						
	Wait States	0	1	2	3	4	5
	Clock Cycles	2	3	4	5	6	7
Continuous		00555h	01555h	02555h	03555h	04555h	05555h
8-word Linear (wrap around)		08555h	09555h	0A555h	0B555h	0C555h	0D555h

Table 8.9 Burst Modes (Sheet 2 of 2)

Burst Mode	Third Cycle Addresses for Wait States						
	Wait States	**0**	**1**	**2**	**3**	**4**	**5**
	Clock Cycles	**2**	**3**	**4**	**5**	**6**	**7**
16-word Linear (wrap around)		10555h	11555h	12555h	13555h	14555h	15555h
32-word Linear (wrap around)		18555h	19555h	1A555h	1B555h	1C555h	1D555h
8-word Linear (no wrap around)		28555h	29555h	2A555h	2B555h	2C555h	2D555h
16-word Linear (no wrap around)		30555h	31555h	32555h	33555h	34555h	35555h
32-word Linear (no wrap around)		38555h	39555h	3A555h	3B555h	3C555h	3D555h

Note:

1. The burst mode is set in the third cycle of the Set Wait State command sequence.

Upon power up, the device defaults to the maximum seven cycle wait state setting. It is recommended that the wait state command sequence be written, even if the default wait state value is desired, to ensure the device is set as expected. A hardware reset will set the wait state to the default setting.

8.3.1 Handshaking Feature

The host system should set address bits A17–A12 to “000011” for a clock frequency of 54 MHz, assuming continuous burst is desired in both cases, for optimal burst operation.

Table 8.10 describes the typical number of clock cycles (wait states) for various conditions.

Table 8.10 Wait States for Handshaking

Conditions at Address	Typical No. of Clock Cycles after AVD# Low	
	40 MHz	**54 MHz**
Initial address is even	4	5
Initial address is odd	5	6
Initial address is even, and is at boundary crossing (1)	6	7
Initial address is odd, and is at boundary crossing*	7	8

Note:

1. In the 8-, 16- and 32-word burst read modes, the address pointer does not cross 64-word boundaries when wrap around is enabled (at address 3Fh, and at addresses offset from 3Fh by multiples of 64).

The autoselect function allows the host system to determine whether the flash device is enabled for handshaking. See the *Autoselect Command Sequence* section for more information.

8.4 Sector Lock/Unlock Command Sequence

The sector lock/unlock command sequence allows the system to determine which sectors are protected from accidental writes. When the device is first powered up, all sectors are locked. To unlock a sector, the system must write the sector lock/unlock command sequence. Two cycles are first written: addresses are don’t care and data is 60h. During the third cycle, the sector address (SLA) and unlock command (60h) is written, while specifying with address A6 whether that sector should be locked (A6 = V_{IL}) or unlocked (A6 = V_{IH}). After the third cycle, the system can continue to lock or unlock additional cycles, or exit the sequence by writing F0h (reset command).

Note that the last two outermost boot sectors can be locked by taking the WP# signal to V_{IL}. Also, if A_{cc} is at V_{IL} all sectors are locked; if the A_{cc} input is at V_{ID}, all sectors are unlocked.

8.5 Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don’t cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend).

8.6 Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Table 8.16 shows the address and data requirements. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. The system may read at any address within the same bank any number of times without initiating another autoselect command sequence. The following table describes the address requirements for the various autoselect functions, and the resulting data. BA represents the bank address, and SA represent the sector address. The device ID is read in three cycles.

Table 8.11 Autoselect Device ID

Description	Address	Read Data			
		S29NS128J	S29NS064J	S29NS032J	S29NS016J
Manufacturer ID	(BA) + 00h	0001h			
Device ID, Word 1	(BA) + 01h	007Eh	277Eh	2A7Eh	297Eh
Device ID, Word 2	(BA) + 0Eh	0016h	2702h	2A24h	2915h
Device ID, Word 3	(BA) + 0Fh	0000h	2700h	2A00h	2900h
Sector Block Lock/Unlock	(SA) + 02h	0001h (locked), 0000h (unlocked)			
Revision ID	(BA) + 03h	TBD, Based on Nokia spec			

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

8.7 Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 8.16 shows the address and data requirements for the program command sequence.

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by monitoring DQ7. Refer to the *Write Operation Status* section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so may cause that bank to set DQ5 = 1, or cause the DQ7 status bit to

indicate the operation was successful. However, a succeeding read will show that the data is still “0.” Only erase operations can convert a “0” to a “1.”

Note: By default, upon every power up, the sectors will automatically be locked.

Therefore, everytime after power-up, users need to write unlock command to unlock the sectors before giving program/erase command.

8.7.1 Unlock Bypass Command Sequence

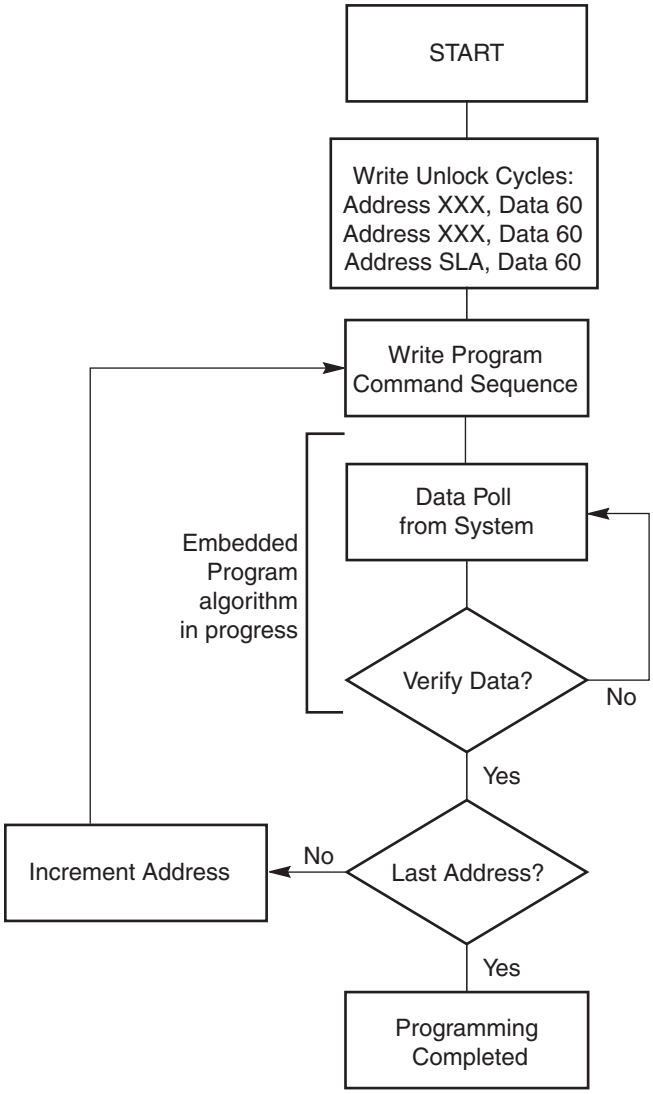
The unlock bypass feature allows the system to program to a bank faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. That bank then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 8.16 shows the requirements for the unlock bypass command sequences.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the bank address and the data 90h. The second cycle need only contain the data 00h. The bank then returns to the read mode.

The device offers accelerated program operations through the A_{cc} input. When the system asserts A_{cc} on this input, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the A_{cc} input to accelerate the operation.

Figure 8.1 illustrates the algorithm for the program operation. Refer to the *Erase/Program Operations* table in the AC Characteristics section for parameters, and Figure 14.7 for timing diagrams.

Figure 8.1 Program Operation



Note

1. See Table 8.16 for program command sequence.

8.8 Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 8.16 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7. Refer to the *Write Operation Status* section for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 8.2 illustrates the algorithm for the erase operation. Refer to the *Erase/Program Operations* table in the AC Characteristics section for parameters, and Figure 14.8 section for timing diagrams.

8.9 Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 8.16 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of no less than t_{SEA} (sector erase accept) occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than t_{SEA}, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets that bank to the read mode.** The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing bank. The system can determine the status of the erase operation by reading DQ7in the erasing bank. Refer to the *Write Operation Status* section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 8.2 illustrates the algorithm for the erase operation. Refer to the *Erase/Program Operations* table in the AC Characteristics section for parameters, and Figure 14.8 section for timing diagrams.

8.9.1 Accelerated Sector Group Erase

Under certain conditions, the device can erase sectors in parallel. This method of erasing sectors is faster than the standard sector erase command sequence. Table 8.12 lists the sector erase groups.

The accelerated sector group erase function must not be used more than 100 times per sector. In addition, accelerated sector group erase should be performed at room temperature (30 +/- 10°C).

Table 8.12 Accelerated Sector Erase Groups, S29NS128J

SA0–SA7	SA128–SA135
SA8–SA15	SA136–SA143
SA16–SA23	SA144–SA151
SA24–SA31	SA152–SA159
SA32–SA39	SA160–SA167
SA40–SA47	SA168–SA175
SA48–SA55	SA176–SA183
SA56–SA63	SA184–SA191
SA64–SA71	SA192–SA199
SA72–SA79	SA200–SA207
SA80–SA87	SA208–SA215
SA88–SA95	SA216–SA223
SA96–SA103	SA224–SA231
SA104–SA111	SA232–SA239
SA112–SA119	SA240–SA247
SA120–SA127	SA248–SA254

Table 8.13 Accelerated Sector Erase Groups, S29NS064J

SA0–SA7
SA8–SA15
SA16–SA23
SA24–SA31
SA32–SA39
SA40–SA47
SA48–SA55
SA56–SA63
SA64–SA71
SA72–SA79
SA80–SA87
SA88–SA95
SA96–SA103
SA104–SA111
SA112–SA119
SA120–SA126

Table 8.14 Accelerated Sector Erase Groups, S29NS032J

SA0–SA3	SA16-SA19	SA32-SA35	SA48-SA51
SA4–SA7	SA20-SA23	SA36-SA39	SA52-SA55
SA8–SA11	SA24-SA27	SA40-SA43	SA56–SA59
SA12-SA15	SA28-SA31	SA44-SA47	SA60–SA62

Table 8.15 Accelerated Sector Erase Groups, S29NS016J

SA0–SA1	SA8-SA9	SA16-SA17	SA24-SA25
SA2–SA3	SA10-SA11	SA18-SA19	SA26-SA27
SA4–SA5	SA12-SA13	SA20-SA21	SA28-SA29
SA6–SA7	SA14-SA15	SA24-SA25	SA30

Use the following procedure to perform accelerated sector group erase:

1. Unlock all sectors in a sector group to be erased using the sector lock/unlock command sequence. All sectors that remain locked will not be erased.
2. Apply 12 V to the A_{cc} input. This voltage must be applied at least 1 µs before executing Step 3.
3. Write 80h to any address within a sector group to be erased.
4. Write 10h to any address within a sector group to be erased.
5. Monitor status bits DQ2/DQ6 or DQ7 to determine when erasure is complete, just as in the standard erase operation. See *Write Operation Status* for further details.
6. Lower A_{cc} from 12 V to V_{CC}.
7. Relock sectors as required.

8.10 Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, program data to, any sector not selected for erasure. The system may also lock or unlock any sector while the erase operation is suspended. **The system must not write the sector lock/unlock command to sectors selected for erasure.** The bank address is required when writing this command. This command is valid only during the sector erase operation, including the minimum t_{SEA} time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires t_{ESL} (erase suspend latency) to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

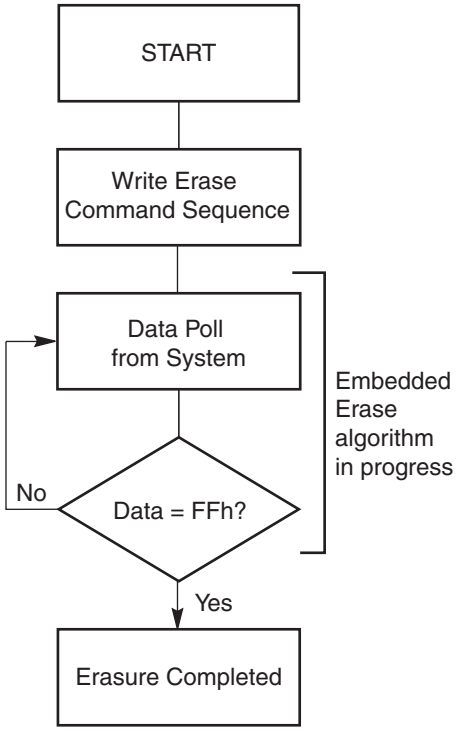
After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) The system may also lock or unlock any sector while in the erase-suspend-read mode. Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7 to determine if a sector is actively erasing or is erase-suspended. Refer to the *Write Operation Status* section for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using DQ7 , just as in the standard program operation. Refer to the *Write Operation Status* section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the *Autoselect Functions* and *Autoselect Command Sequence* sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Figure 8.2 Erase Operation



Notes

1. *See Table 8.16 for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Table 8.16 Command Definitions

Command Sequence (Notes)	Cycles	Bus Cycles (Notes 1–6)											
		First		Second		Third		Fourth		Fifth		Sixth	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Asynchronous Read (7)	1	RA	RD										
Reset (8)	1	XXX	F0										

Table 8.16 Command Definitions

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 1–6)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Autoselect (9)	Manufacturer ID	4	555	AA	2AA	55	(BA)555	90	(BA)X00	0001				
	Device ID	6	555	AA	2AA	55	(BA)555	90	(BA)X01	(10)	(BA)X0E	(11)	(BA) X0F	(12)
	Sector Lock Verify (13)	4	555	AA	2AA	55	(SA)555	90	(SA)X02	(13)				
	Revision ID (14)	4	555	AA	2AA	55	(BA)555	90	(BA)X03	(14)				
Unlock Bypass	Mode Entry	3	555	AA	2AA	55	555	20						
	Program (15)	2	XXX	A0	PA	PD								
	Reset (16)	2	BA	90	XXX	00								
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend (17)		1	BA	B0										
Erase Resume (18)		1	BA	30										
Sector Lock/Unlock		3	XXX	60	XXX	60	SLA	60						
Set Config. Register (19)		3	555	AA	2AA	55	(CR)555	C0						
CFI Query (20)		1	55	98										

Legend
X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A_{max}–A13 uniquely select any sector.

BA = Address of the bank (A22–A21 for S29NS128J, A21–A20 for S29NS064J, A20–A19 for S29NS032J, A19–A18 for S29NS016J) that is being switched to autoselect mode, is in bypass mode, or is being erased.

SLA = Address of the sector to be locked. Set sector address (SA) and either A6 = 1 for unlocked or A6 = 0 for locked.

CR = Configuration Register set by address bits A17–A12.

Notes
1. *See Table 7.1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15–DQ8 are don't care in command sequences, except for RD and PD.*
5. *Unless otherwise noted, address bits A_{max}–A12 are don't cares.*
6. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.*
7. *No unlock or command cycles required when bank is reading array data.*
8. *The Reset command is required to return to reading array data (or to the erase-suspend-read mode if previously in Erase Suspend) when a bank i in the autoselect mode, or if DQ5 goes high (while the bank is providing status information).*
9. *The fourth cycle of the autoselect command sequence is a read cycle. Th system must read device IDs across the 4th, 5th, and 6th cycles, The system must provide the bank address. See the Autoselect Command Sequence section for more information.*
10. *For S29NS128J, the data is 007Eh. For S29NS064J, the data is 277Eh. Fo S29NS032J, the data is 2A7Eh. For S29NS016J, the data is 297Eh.*
11. *For S29NS128J, the data is 0016h. For S29NS064J, the data is 2702h, fo S29NS032J, the data is 2A24h, for S29NS016J, the data is 2915h.*
12. *For S29NS128J, the data is 0000h, for S29NS064J, the data is 2700h, fo S29NS032J, the data is 2A00h for S29NS016J, the data is 2900h.*
13. *The data is 0000h for an unlocked sector and 0001h for a locked sector.*
14. *The data is TBD, based on Nokia spec.*
15. *The Unlock Bypass command sequence is required prior to this comman sequence.*
16. *The Unlock Bypass Reset command is required to return to reading array data when the bank is in the unlock bypass mode.*
17. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation, and requires the bank address.*
18. *The Erase Resume command is valid only during the Erase Suspend mode, and requires the bank address.*
19. *The addresses in the third cycle must contain, on A17–A12, the additiona wait counts to be set. See Set Configuration Register Command Sequenc*
20. *Command is valid when device is ready to read array data or when device in autoselect mode.*

9. Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5 and DQ7. Table 9.2 and the following subsections describe the function of these bits. DQ7 a method for determining whether a program or erase operation is complete or in progress.

9.1 DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately t_{PSP}, then that bank returns to the read mode.

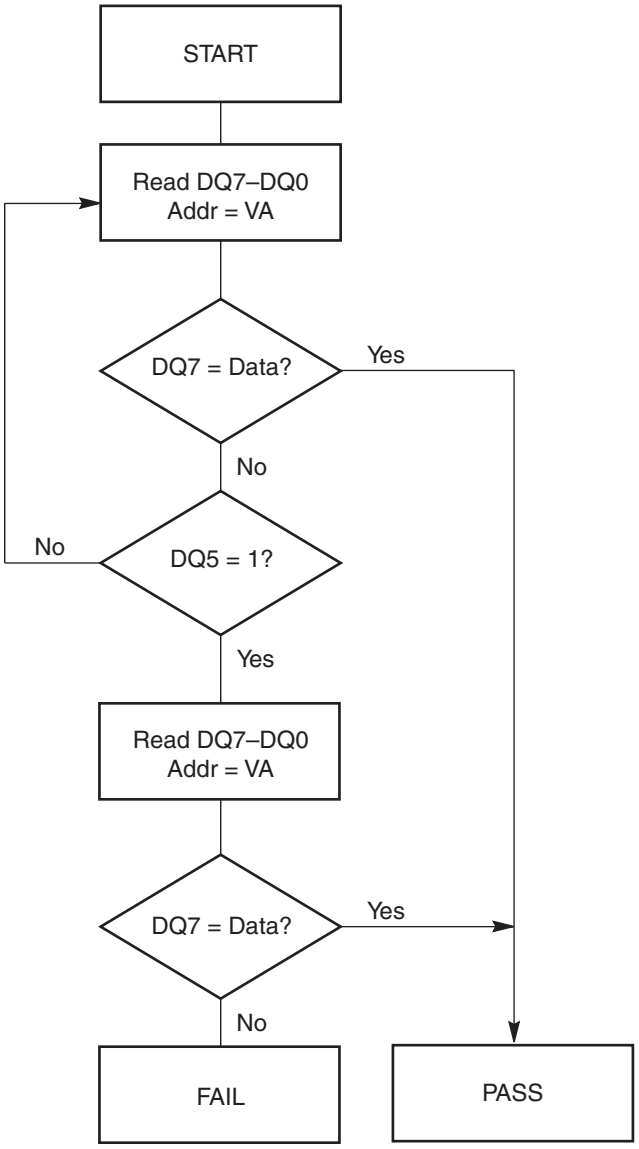
During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately t_{ASP} (all sectors protected toggle time), then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ6–DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ6–DQ0 may be still invalid. Valid data on DQ7–DQ0 will appear on successive read cycles.

Table 9.2 shows the outputs for Data# Polling on DQ7. Figure 9.1 shows the Data# Polling algorithm. Figure 14.10 in the *AC Characteristics* section shows the Data# Polling timing diagram.

Figure 9.1 Data# Polling Algorithm



Notes

1. *VA = Valid Address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

9.2 RDY: Ready

The RDY pin is a dedicated status output that indicates valid output data on A/DQ15–A/DQ0 during burst (synchronous) reads. When RDY is asserted (RDY = V_{OH}), the output data is valid and can be read. When RDY is de-asserted (RDY = V_{OL}), the system should wait until RDY is re-asserted before expecting the next word of data.

In synchronous (burst) mode with CE# = OE# = V_{IL}, RDY is de-asserted under the following conditions: during the initial access; after crossing the internal boundary between addresses 3Eh and 3Fh (and addresses offset from these by a multiple of 64); and when the clock frequency is less than 6 MHz (in which case RDY is de-asserted every third clock cycle). The RDY pin will also switch during status reads when a clock signal drives the CLK input. In addition, RDY = V_{OH} when CE# = V_{IL} and OE# = V_{IH}, and RDY is Hi-Z when CE# = V_{IH}.

In asynchronous (non-burst) mode, the RDY pin does not indicate valid or invalid output data. Instead, RDY = V_{OH} when CE# = V_{IL}, and RDY is Hi-Z when CE# = V_{IH}.

9.3 DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address in the same bank, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. Note that OE# must be low during toggle bit status reads. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately t_{ASP}, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

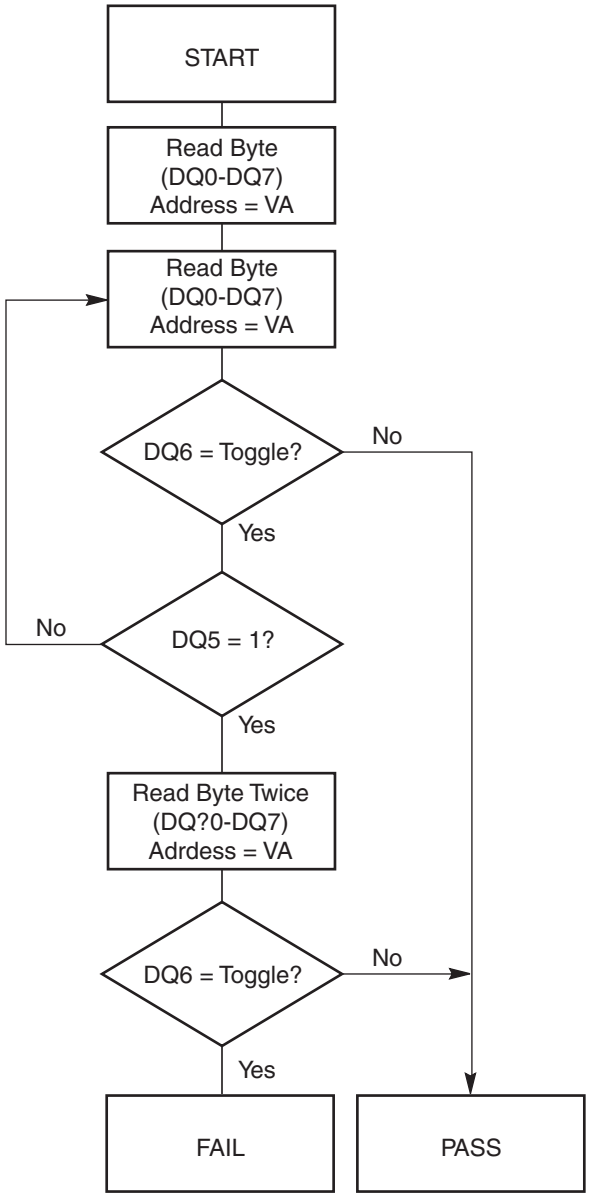
The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on *DQ7: Data# Polling*).

If a program address falls within a protected sector, DQ6 toggles for approximately after t_{PSP} the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

See the following for additional information: (toggle bit flowchart), *DQ6: Toggle Bit I* (description), Figure 14.11 (toggle bit timing diagram), and Table 9.1 (compares DQ2 and DQ6).

Figure 9.2 Toggle Bit Algorithm



Note

1. *The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See the subsections on DQ6 and DQ2 for more information.*

9.4 DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. Note that OE# must be low during toggle bit status reads. But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 9.2 to compare outputs for DQ2 and DQ6.

See the following for additional information: (toggle bit flowchart), *DQ6: Toggle Bit I* (description), Figure 14.11 (toggle bit timing diagram), and Table 9.1 (compares DQ2 and DQ6).

Table 9.1 DQ6 and DQ2 Indications

If device is	and the system reads	then DQ6	and DQ2
programming,	at any address,	toggles,	does not toggle.
actively erasing,	at an address within a sector selected for erasure,	toggles,	also toggles.
	at an address within sectors *not* selected for erasure,	toggles,	does not toggle.
erase suspended,	at an address within a sector selected for erasure,	does not toggle,	toggles.
	at an address within sectors *not* selected for erasure,	returns array data,	returns array data. The system can read from any sector not selected for erasure.
programming in erase suspend	at any address,	toggles,	is not applicable.

9.5 Reading Toggle Bits DQ6/DQ2

Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

9.6 DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1,” indicating that the program or erase cycle was not successfully completed.

The device may output a “1” on DQ5 if the system tries to program a “1” to a location that was previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a “1.”

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

9.7 DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a “0” to a “1.” If the time between additional sector erase commands from the system can be assumed to be less than t_{SEA}, the system need not monitor DQ3. See also the *Sector Erase Command Sequence* section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is “1,” the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0,” the device will accept additional sector erase commands.

To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 9.2 shows the status of DQ3 relative to the other status bits.

Table 9.2 Write Operation Status

Status			DQ7 (2)	DQ6	DQ5 (1)	DQ3	DQ2 (2)
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle
Erase Suspend Mode	Erase Suspend Read (4)	Erase Suspended Sector	1	No toggle	0	N/A	Toggle
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data
	Erase Suspend Program		DQ7#	Toggle	0	N/A	N/A

Notes

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.*
4. *The system may read either asynchronously or synchronously (burst) while in erase suspend. RDY will function exactly as in non-erase-suspended mode.*

10. Absolute Maximum Ratings

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–65°C to +125°C
Voltage with Respect to Ground, All Inputs and I/Os except A_{cc} (Note 1)	–0.5 V to V_{CC} + 0.5 V
V_{CC} (1)	–0.5 V to +2.5 V
A_{cc} (2)	–0.5 V to +12.5 V
Output Short Circuit Current (3)	100 mA

Notes

1. *Minimum DC voltage on input or I/Os is –0.5 V. During voltage transitions, input at I/Os may undershoot V_{SS} to –2.0 V for periods of up to 20 ns during voltage transitions inputs might overshooot to V_{CC} +0.5 V for periods up to 20 ns. See Figure 10.1. Maximum DC voltage on output and I/Os is V_{CC} + 0.5 V. During voltage transitions outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 10.2.*
2. *Minimum DC input voltage on A_{cc} is –0.5 V. During voltage transitions, A_{cc} may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 10.1. Maximum DC input voltage on A_{cc} is +12.5 V which may overshoot to +13.5 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

Figure 10.1 Maximum Negative Overshoot Waveform

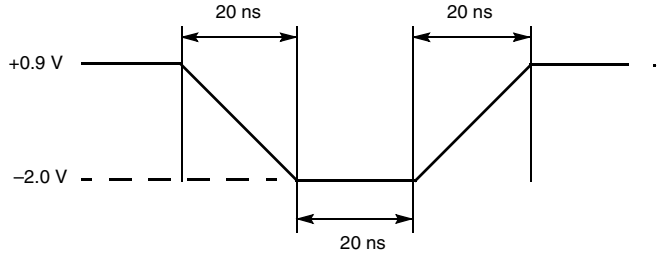
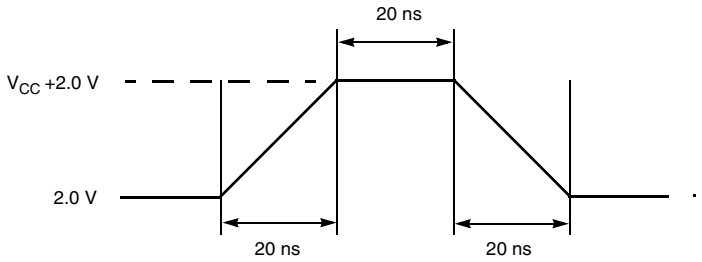


Figure 10.2 Maximum Positive Overshoot Waveform



10.1 Operating Ranges

Ambient Temperature (T_A)	–25°C to +85°C
V_{CC} Supply Voltages	
V_{CC} min	+1.7 V
V_{CC} max	+1.95 V

Note

1. *Operating ranges define those limits between which the functionality of the device is guaranteed.*

11. DC Characteristics

11.1 CMOS Compatible

Parameter	Description	Test Conditions (1)		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1	µA
I_{CCB}	V_{CC} Active Burst Read Current (5)	CE# = V_{IL}, OE# = V_{IL}			25	30	mA
I_{CC1}	V_{CC} Active Asynchronous Read Current (2)	CE# = V_{IL}, OE# = V_{IH}	5 MHz		12	16	mA
			1 MHz		3.5	5	mA
I_{CC2}	V_{CC} Active Write Current (3)	CE# = V_{IL}, OE# = V_{IH}, $A_{cc} = V_{IH}$			15	40	mA
I_{CC3}	V_{CC} Standby Current (4)	CE# = V_{IH}, RESET# = V_{IH}			9	40	µA
I_{CC4}	V_{CC} Reset Current	RESET# = V_{IL}, CLK = V_{IL}			9	40	µA
I_{CC5}	V_{CC} Active Current (Read While Write)	CE# = V_{IL}, OE# = V_{IL}			40	60	mA
I_{PPW}	Accelerated Program Current (6)	A_{cc} = 12 V			7	15	mA
I_{CCW}					5	10	
I_{PPE}	Accelerated Erase Current (6)	A_{cc} = 12 V			7	15	mA
I_{CCE}					5	10	
V_{IL}	Input Low Voltage			–0.5		0.4	V
V_{IH}	Input High Voltage			V_{CC} – 0.4		V_{CC} + 0.2	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA, $V_{CC} = V_{CC\ min}$				0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{CC} – 0.1			V
V_{ID}	Voltage for Accelerated Program			11.5		12.5	V
V_{LKO}	Low V_{CC} Lock-out Voltage			1.0		1.4	V

Notes

1. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
2. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Device enters automatic sleep mode when addresses are stable for t_{ACC} + 60 ns. Typical sleep mode current is equal to I_{CC3}.*
5. *Specifications assume 8 I/Os switching and continuous burst length.*
6. *Not 100% tested. A_{cc} is not a power supply pin.*

12. Test Conditions

Figure 12.1 Test Setup

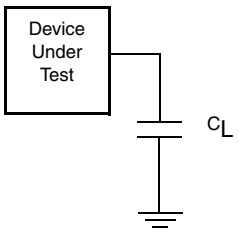
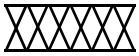
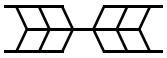


Table 12.1 Test Specifications

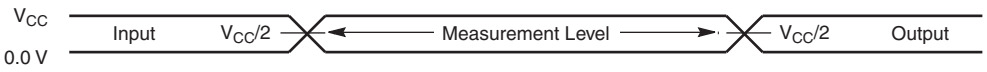
Test Condition	All Speeds	Unit
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0–V_{CC}	V
Input timing measurement reference levels	$V_{CC}/2$	V
Output timing measurement reference levels	$V_{CC}/2$	V

13. Key to Switching Waveforms

Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

13.1 Switching Waveforms

Figure 13.1 Input Waveforms and Measurement Levels

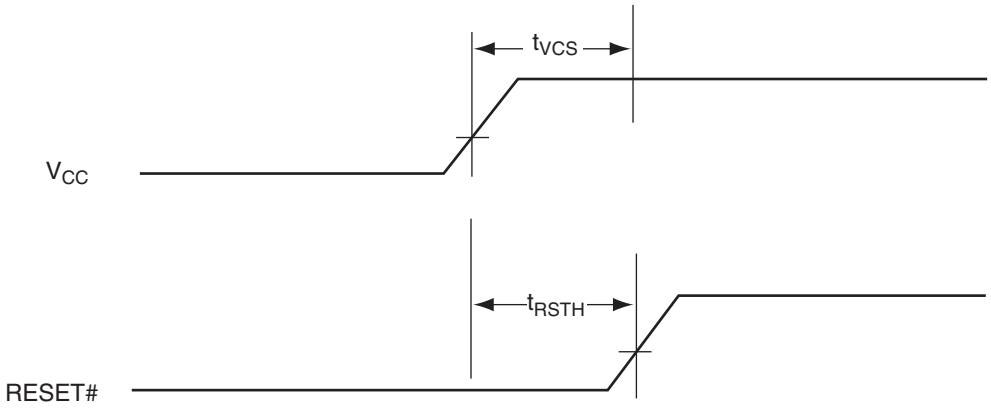


14. AC Characteristics

14.1 V_{CC} Power-up

Parameter	Description	Test Setup	Speed	Unit
t_{VCS}	V_{CC} Setup Time	Min	50	µs
t_{RSTH}	RESET# Low Hold Time	Min	50	µs

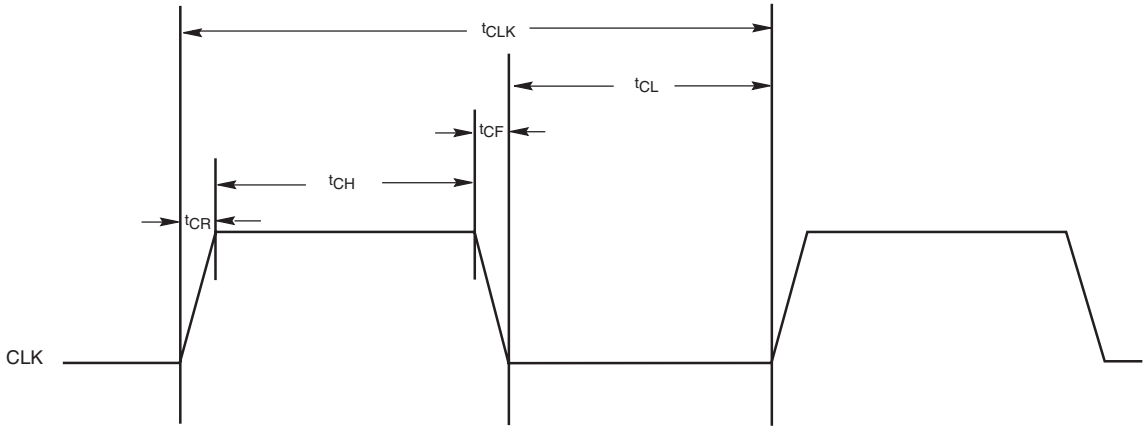
Figure 14.1 V_{CC} Power-up Diagram



14.2 CLK Characterization

Parameter	Description		0L (54 MHz)	Unit
f_{CLK}	CLK Frequency	Max	54	MHz
t_{CLK}	CLK Period	Min	18.5	ns
t_{CH}	CLK High Time	Min	4.5	ns
t_{CL}	CLK Low Time			
t_{CR}	CLK Rise Time	Max	3	ns
t_{CF}	CLK Fall Time			

Figure 14.2 CLK Characterization



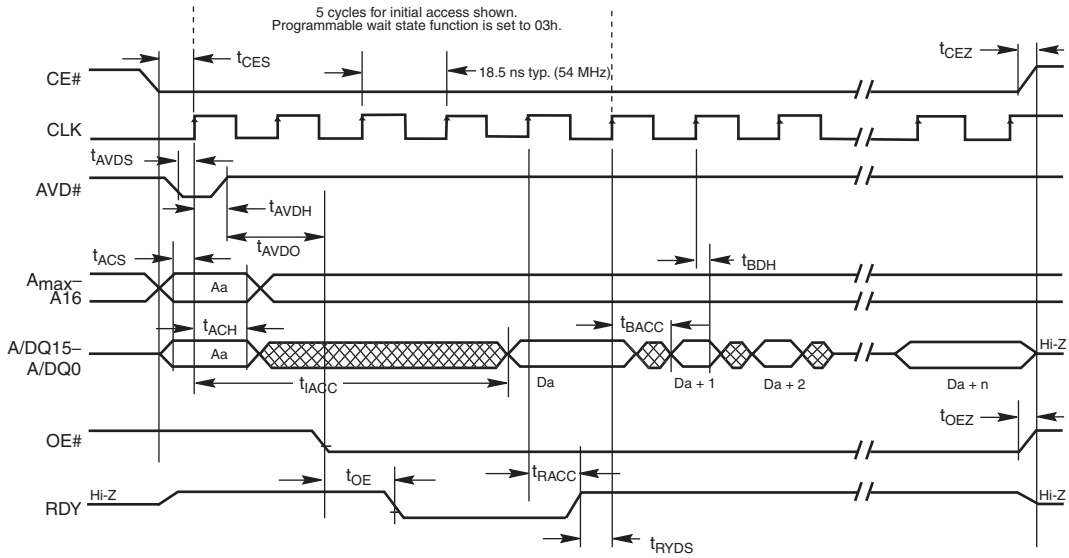
14.3 Synchronous/Burst Read

Parameter		Description		0L (54 MHz)	Unit
JEDEC	Standard				
	t_{IACC}	Initial Access Time	Max	87.5	ns
	t_{BACC}	Burst Access Time Valid Clock to Output Delay	Max	13.5	ns
	t_{AVDS}	AVD# Setup Time to CLK	Min	5	ns
	t_{AVDH}	AVD# Hold Time from CLK	Min	7	ns
	t_{AVDO}	AVD# High to OE# Low	Min	0	ns
	t_{ACS}	Address Setup Time to CLK	Min	5	ns
	t_{ACH}	Address Hold Time from CLK	Min	7	ns
	t_{BDH}	Data Hold Time from Next Clock Cycle (1))	Min	3	ns
	t_{OE}	Output Enable to Data, PS, or RDY Valid	Max	13.5	ns
	t_{CEZ}	Chip Enable to High Z	Max	10	ns
	t_{OEZ}	Output Enable to High Z	Max	10	ns
	t_{CES}	CE# Setup Time to CLK	Min	5	ns
	t_{RDYS}	RDY Setup Time to CLK	Min	5	ns
	t_{RACC}	Ready access time from CLK	Max	13.5	ns

Note:

1. Not 100% tested

Figure 14.3 Burst Mode Read (54 MHz)

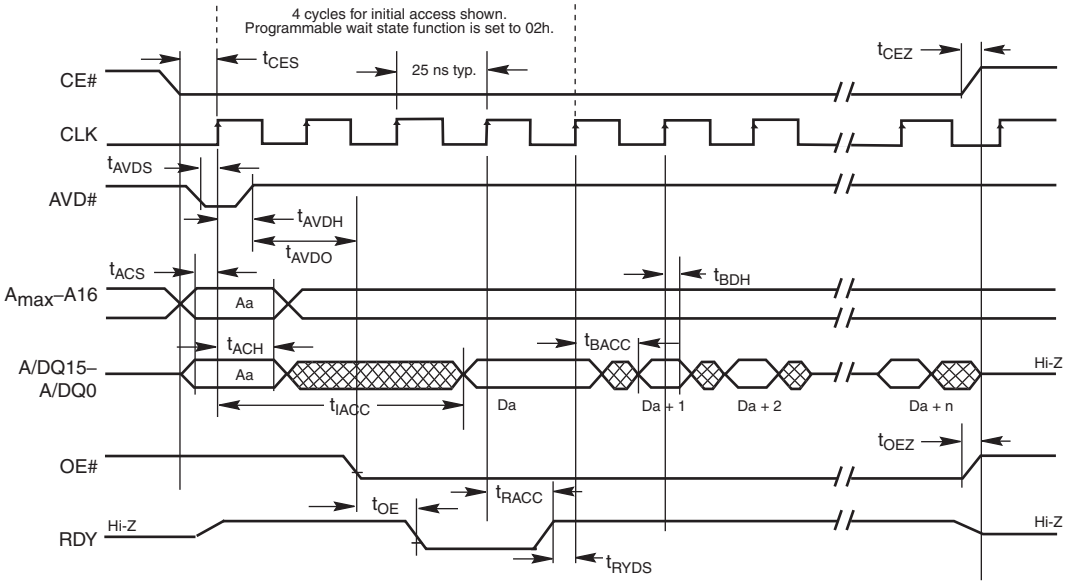


Notes:

1. Figure shows total number of clock set to five.

2. If any burst address occurs at a 64-word boundary, two additional clock cycles are inserted and are indicated by RDY.

Figure 14.4 Burst Mode Read (40 MHz)



Notes

1. *Figure shows total number of clock cycles set to four.*
2. *If any burst address occurs at a 64-word boundary, two additional clock cycle are inserted, and are indicated by RDY.*

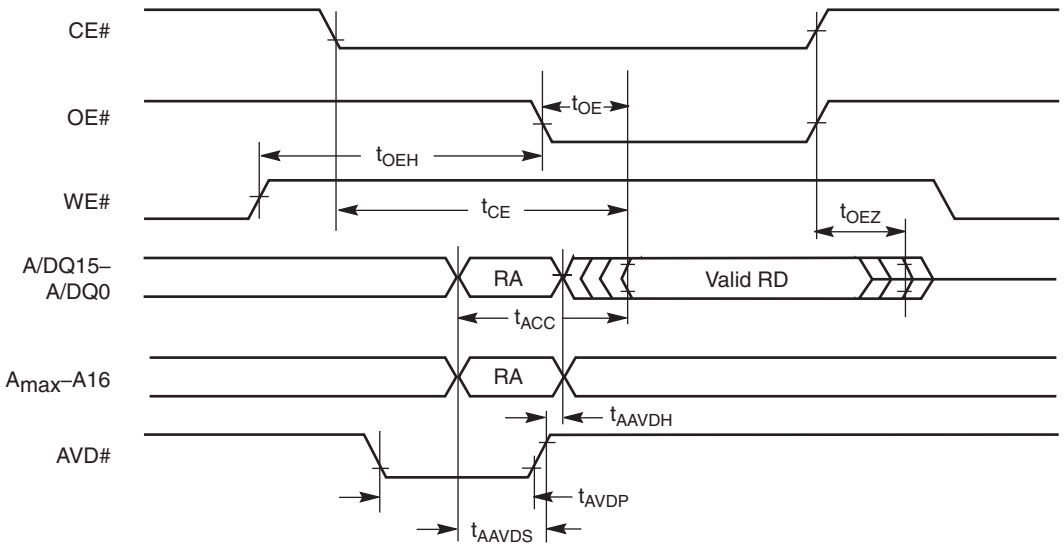
14.4 Asynchronous Read

Parameter		Description			0L (54 MHz)	Unit
JEDEC	Standard					
	t_{CE}	Access Time from CE# Low		Max	70	ns
	t_{ACC}	Asynchronous Access Time		Max	70	ns
	t_{AVDP}	AVD# Low Time		Min	12	ns
	t_{AAVDS}	Address Setup Time to Rising Edge of AVD		Min	5	ns
	t_{AAVDH}	Address Hold Time from Rising Edge of AVD		Min	3.7	ns
	t_{OE}	Output Enable to Output Valid		Max	13.5	ns
	t_{OEH}	Output Enable Hold Time	Read	Min	0	ns
			Data# Polling	Min	10	ns
	t_{OEZ}	Output Enable to High Z (1)		Max	10	ns

Note

1. *Not 100% tested.*

Figure 14.5 Asynchronous Mode Read



Note

1. RA = Read Address, RD = Read Data.

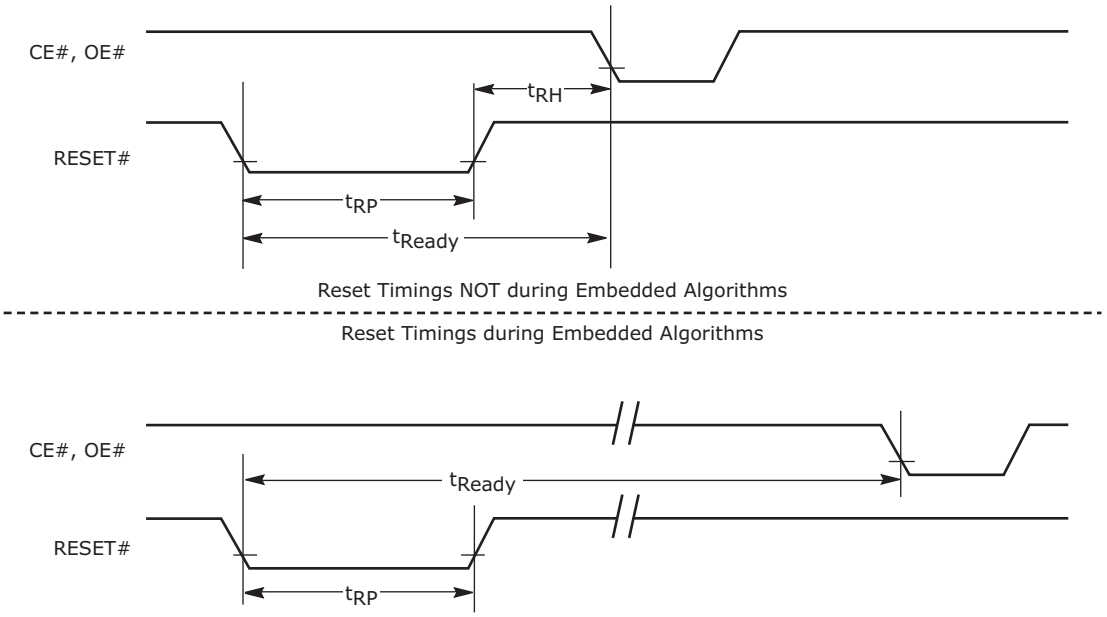
14.5 Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{Readyw}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (1)	Max	35	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (1)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (1)	Min	200	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs

Note

1. Not 100% tested.

Figure 14.6 Reset Timings



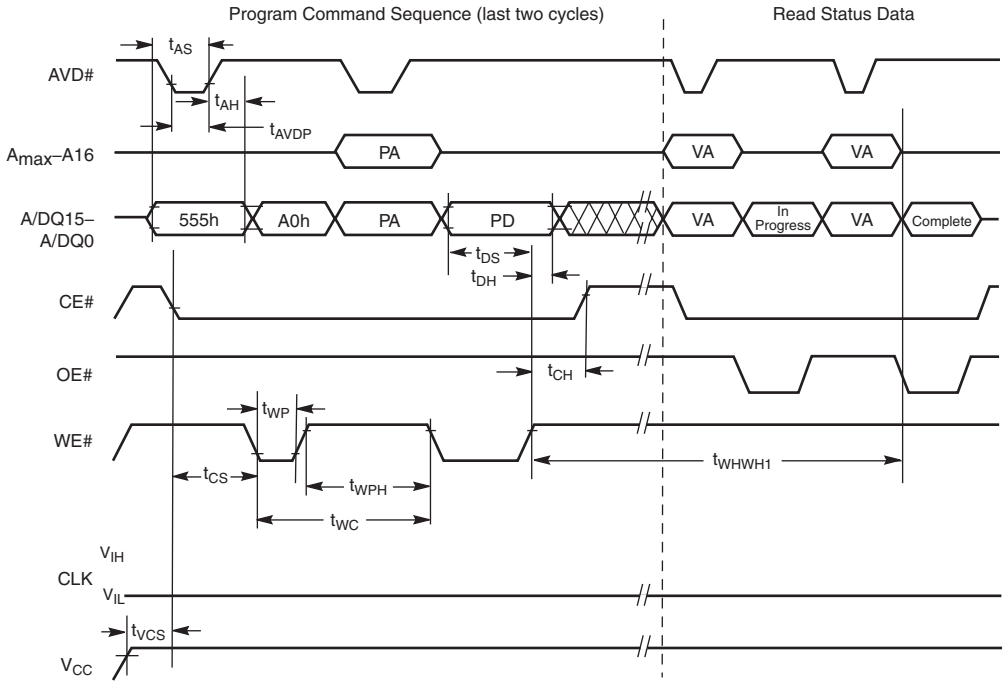
14.6 Erase/Program Operations

Parameter		Description		0L (54 MHz)	Unit
JEDEC	Standard				
t_{AVAV}	t_{WC}	Write Cycle Time (1)	Min	80	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	5	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	7	ns
	t_{AVDP}	AVD# Low Time	Min	12	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	45	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write	Typ	0	ns
t_{ELWL}	t_{CS}	CE# Setup Time	Typ	0	ns
t_{WHEH}	t_{CH}	CE# Hold Time	Typ	0	ns
t_{WLWH}	t_{WP}/t_{WRL}	Write Pulse Width	Typ	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Typ	30	ns
	$t_{SR/W}$	Latency Between Read and Write Operations	Min	0	ns
	t_{Acc}	A_{cc} Rise and Fall Time	Min	500	ns
	t_{VPS}	A_{cc} Setup Time (During Accelerated Programming)	Min	1	µs
	t_{VCS}	V_{CC} Setup Time	Min	50	µs
	t_{SEA}	Sector Erase Accept Time-out	Max	50	µs
	t_{ESL}	Erase Suspend Latency	Max	35	µs
	t_{ASP}	Toggle Time During Sector Protection	Typ	100	µs
	t_{PSP}	Toggle Time During Programming Within a Prot	Typ	1	µs

Notes

1. *Not 100% tested.*
2. *See the Erase and Programming Performance section for more information.*
3. *Does not include the preprogramming time.*

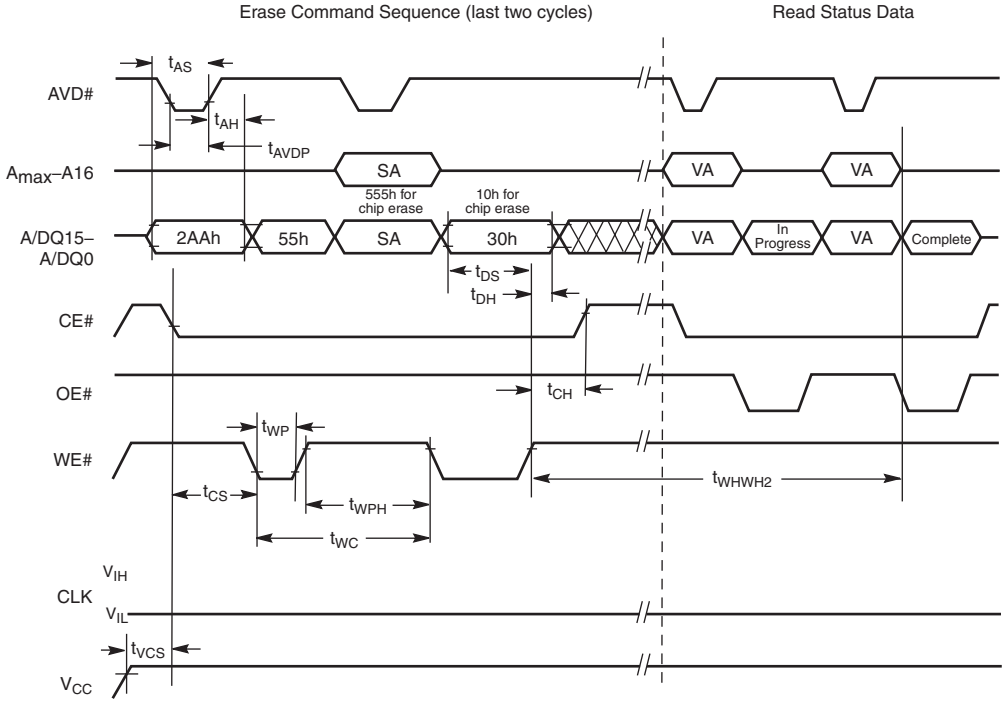
Figure 14.7 Program Operation Timings



Notes

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A_{max}–A16 are don't care during command sequence unlock cycles.*

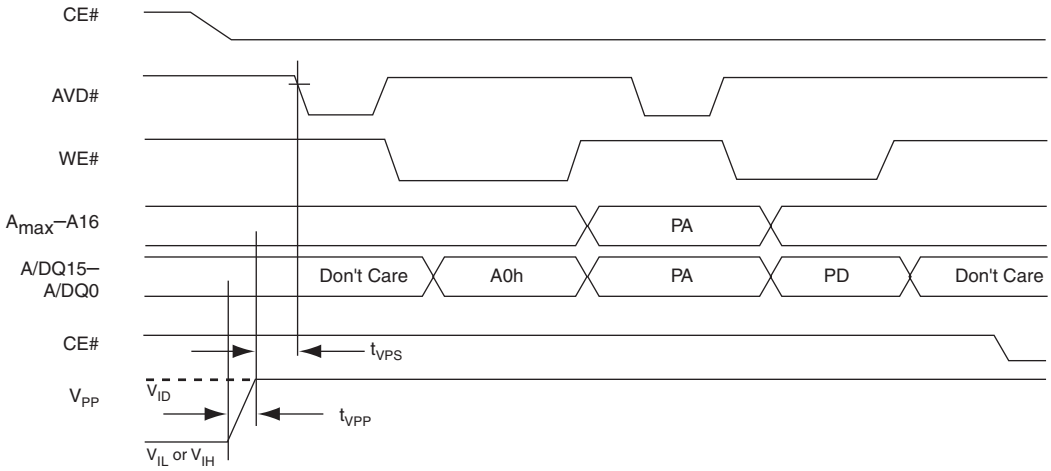
Figure 14.8 Chip/Sector Erase Operations



Notes

1. *SA is the sector address for Sector Erase.*
2. *Address bits A_{max}–A16 are don't cares during unlock cycles in the command sequence.*

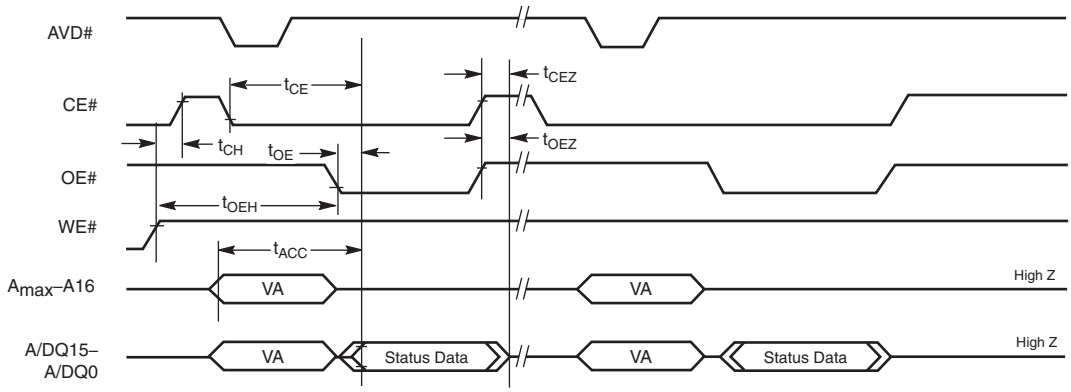
Figure 14.9 Accelerated Unlock Bypass Programming Timing



Notes

1. *A_{cc} can be left high for subsequent programming pulses.*
2. *Use setup and hold times from conventional program operation.*

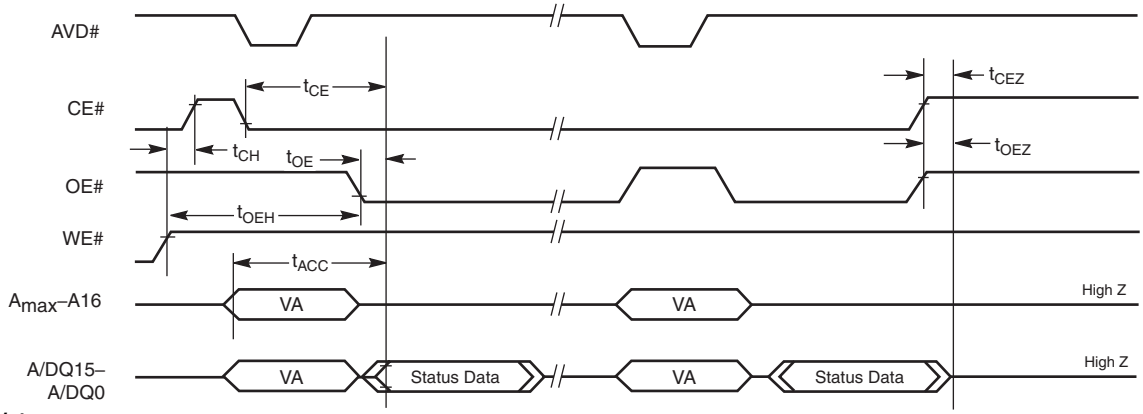
Figure 14.10 Data# Polling Timings (During Embedded Algorithm)



Notes

1. *All status reads are asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is completeData# Polling will output true data.*

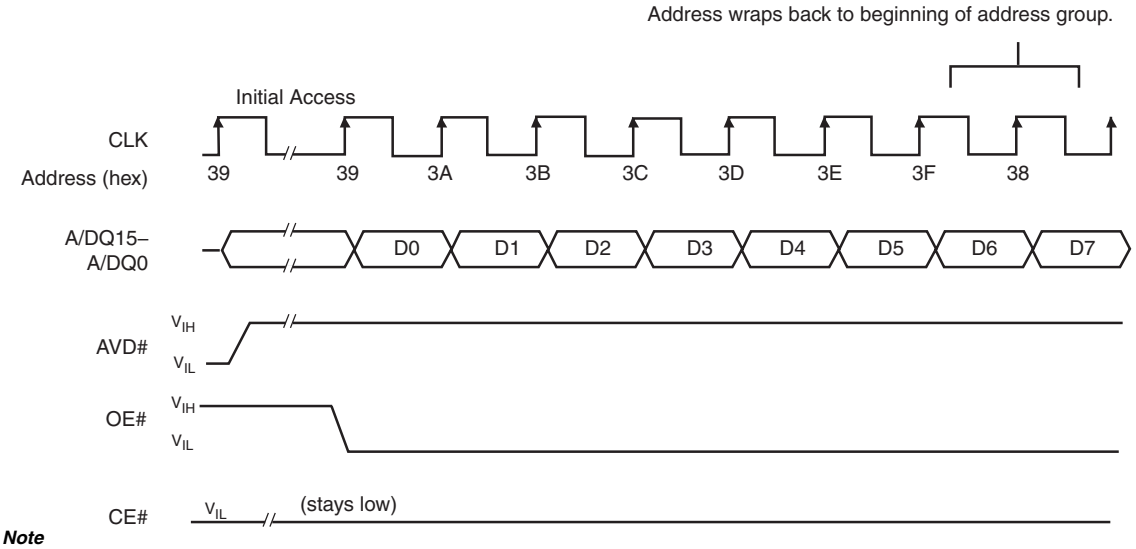
Figure 14.11 Toggle Bit Timings (During Embedded Algorithm)



Notes

1. *All status reads are asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, .*

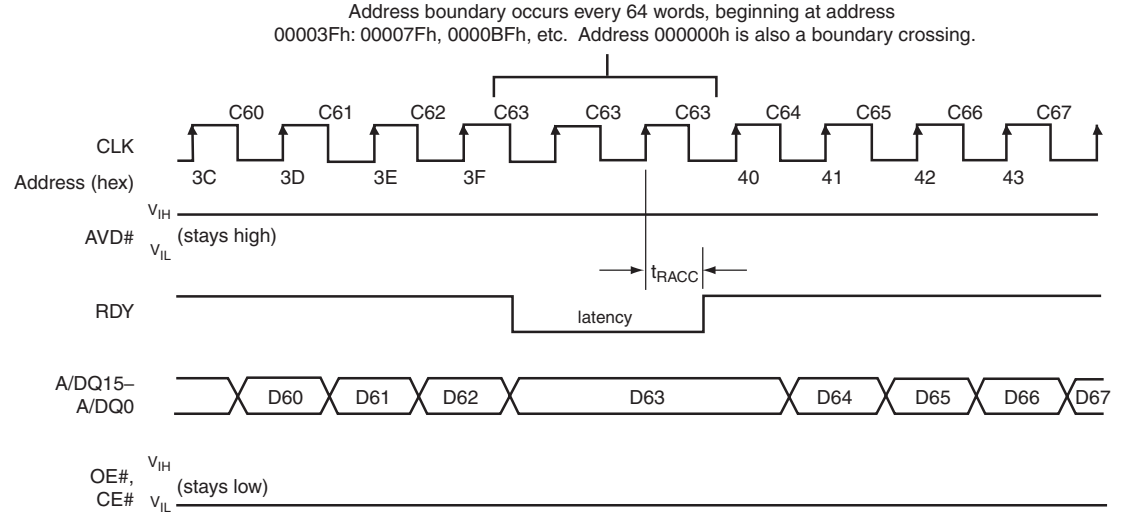
Figure 14.12 8-, 16-, and 32-Word Linear Burst Address Wrap Around



Note

1. *8-word linear burst mode shown. 16- and 32-word linear burst read modes behave similarly. D0 represents the first word of the linear burst.*

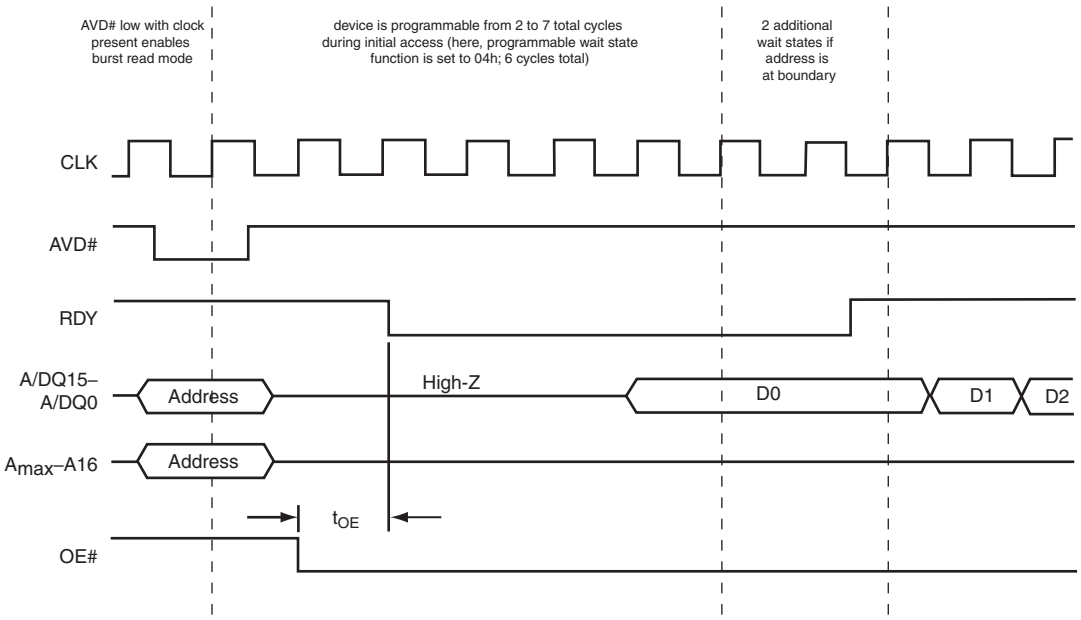
Figure 14.13 Latency with Boundary Crossing



Note

1. *Cxx indicates the clock that triggers data Dxx on the outputs; for example, C60 triggers D60.*

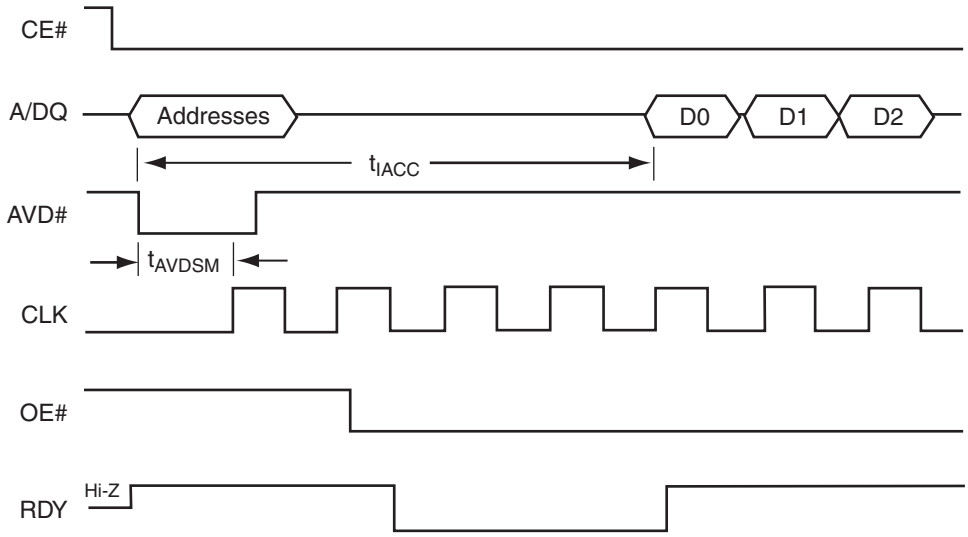
Figure 14.14 Initial Access at 3Eh with Address Boundary Latency



Note

1. *Devices should be programmed with wait states as discussed in Programmable Wait State on page 21.*

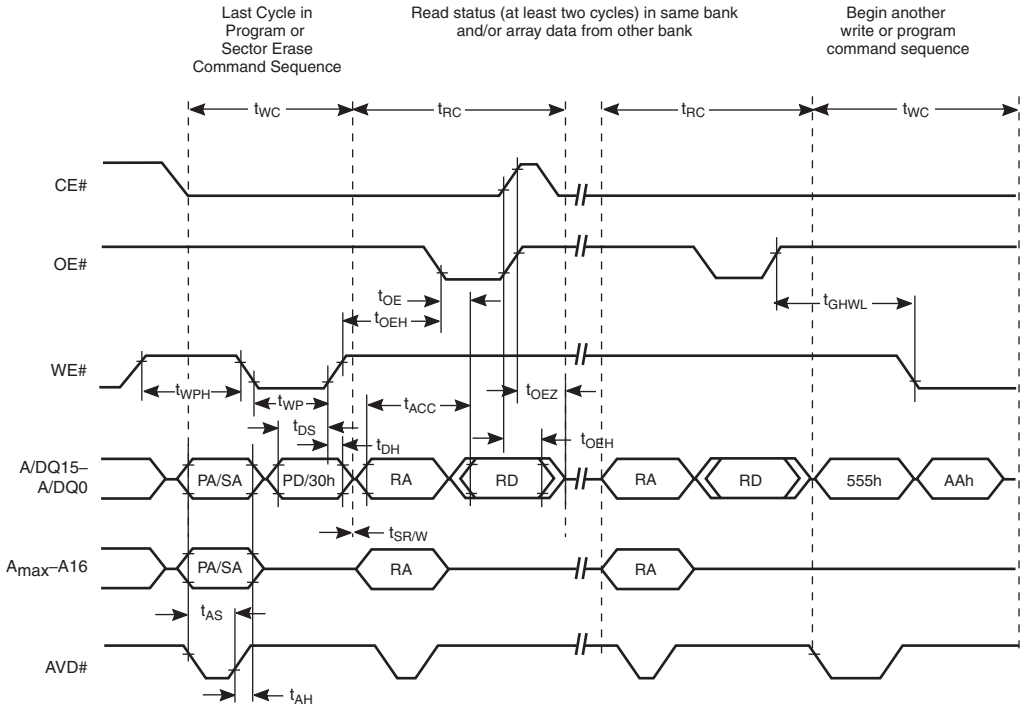
Figure 14.15 Example of Extended Valid Address Reducing Wait State Usage



Note

1. *If t_{AVDSM} > 1 CLK cycle, wait state usage is reduced. Figure shows 40 MHz clock, handshaking enabled. Wait state usage is 4 clock cycles instead of 5. Note that t_{AVDSM} must be less than 76 µs for burst operation to begin.*

Figure 14.16 Back-to-Back Read/Write Cycle Timings



Note

1. *Breakpoints in waveforms indicate that system may alternately read array data from the "non-busy bank" while checking the status of the program or erase operation in the "busy" bank. The system should read status twice to ensure valid information.*

15. Erase and Programming Performance

Parameter			Typ (1)	Max (2)	Unit	Comments
Sector Erase Time	32 Kword		0.4	5	s	
	8 Kword		0.2	5		
Chip Erase Time		128 Mb	108		s	Excludes 00h programming prior to erasure (4)
		64 Mb	54			
		32 Mb	27			
		16 Mb	13.5			
Word Programming Time			9	210	µs	Excludes system level overhead (5)
Accelerated Word Programming Time			4	120	µs	
Chip Programming Time (3)		128 Mb	96	288	s	
		64 Mb	48	144		
		32 Mb	24	72		
		16 Mb	12	36		
Accelerated Chip Programming Time		128 Mb	32	96	s	
		64 Mb	16	48		
		32 Mb	8	24		
		16 Mb	4	12		
Accelerated Chip Erase Time		128 Mb	50		s	
		64 Mb	25			
		32 Mb	12.5			
		16 Mb	6.25			

Notes

1. *Typical program and erase times assume the following conditions: 25°C, 1.8 V V_{CC}, 100,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 1.7 V, 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all words are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 8.16 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 100,000 cycles.*

16. BGA Ball Capacitance

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	4.2	5.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	5.4	6.5	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	3.9	4.7	pF

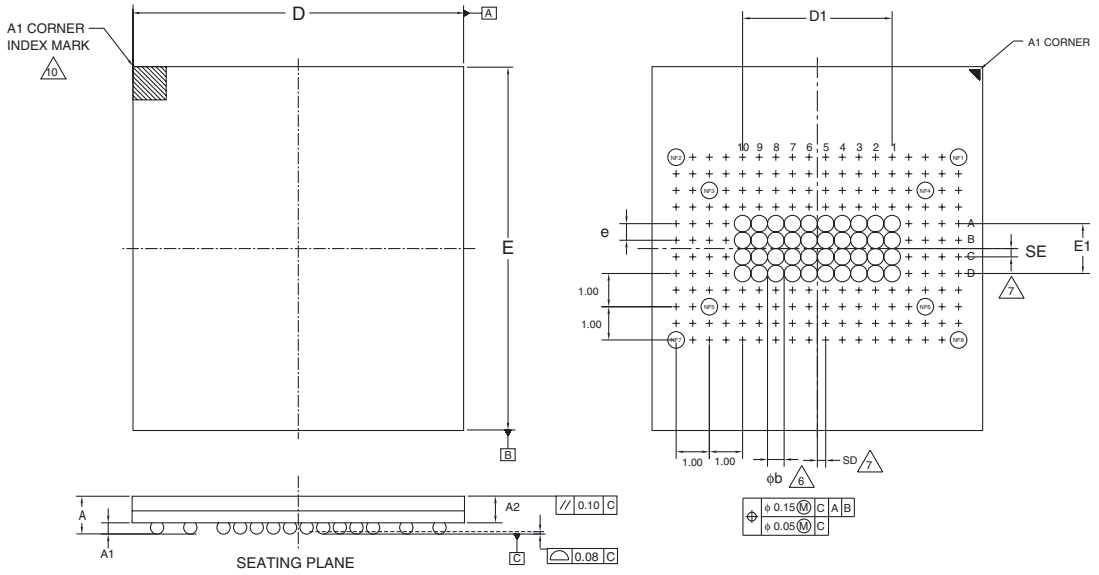
Notes

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

17. Physical Dimensions

17.1 S29NS128J

VDC048—48-Ball Very Thin Fine-Pitch Ball Grid Array (FBGA) 10 x 11 mm Package



PACKAGE	VDC 048			
JEDEC	N/A			
	9.95 mm x 10.95 mm NOM PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	0.86	---	1.00	OVERALL THICKNESS
A1	0.20	---	---	BALL HEIGHT
A2	0.66	0.71	0.76	BODY THICKNESS
D	9.85	9.95	10.05	BODY SIZE
E	10.85	10.95	11.05	BODY SIZE
D1	4.50			BALL FOOTPRINT
E1	1.50			BALL FOOTPRINT
MD	10			ROW MATRIX SIZE D DIRECTION
ME	4			ROW MATRIX SIZE E DIRECTION
N	48			TOTAL BALL COUNT
φb	0.25	0.30	0.35	BALL DIAMETER
e	0.50			BALL PITCH
SD / SE	0.25			SOLDER BALL PLACEMENT

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.

   N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. NOT USED.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

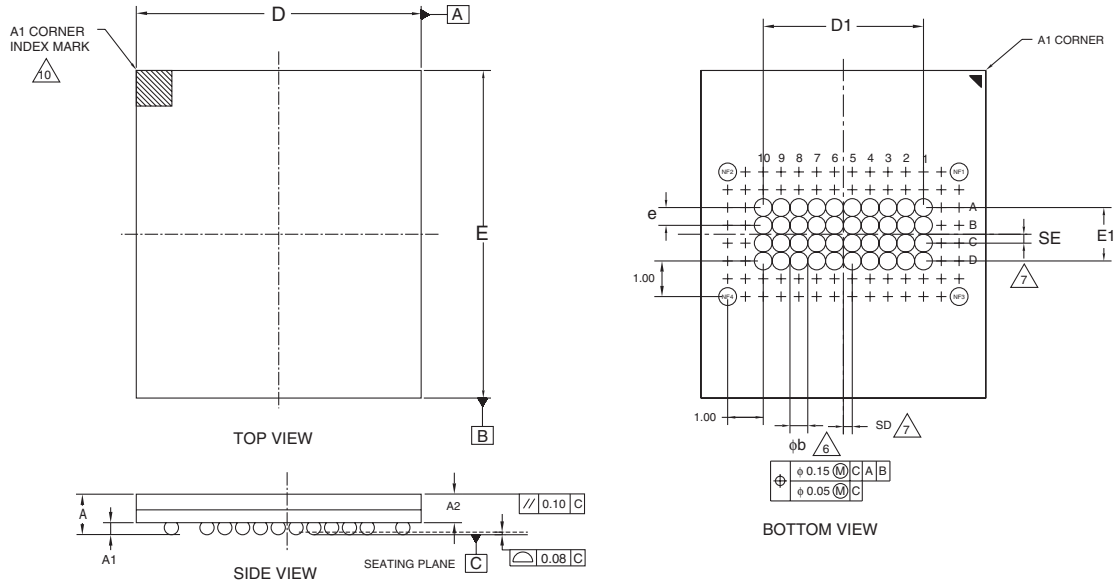
3241 \ 16-038.9h.aa01

Note

1. For reference only. BSC is an ANSI standard for Basic Space Centering.

17.2 S29NS064J

VDD044—44-Ball Very Thin Fine-Pitch Ball Grid Array (FBGA) 9.2 x 8 mm Package



PACKAGE	VDD 044			
JEDEC	N/A			
	8.00 mm x 9.20 mm NOM PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	0.86	---	1.00	OVERALL THICKNESS
A1	0.20	---	---	BALL HEIGHT
A2	0.66	0.71	0.76	BODY THICKNESS
D	7.90	8.00	8.10	BODY SIZE
E	9.10	9.20	9.30	BODY SIZE
D1		4.50		BALL FOOTPRINT
E1		1.50		BALL FOOTPRINT
MD		10		ROW MATRIX SIZE D DIRECTION
ME		4		ROW MATRIX SIZE E DIRECTION
N		44		TOTAL BALL COUNT
ϕb	0.25	0.30	0.35	BALL DIAMETER
e		0.50		BALL PITCH
SD / SE		0.25		SOLDER BALL PLACEMENT

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.

   N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]
8. NOT USED.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

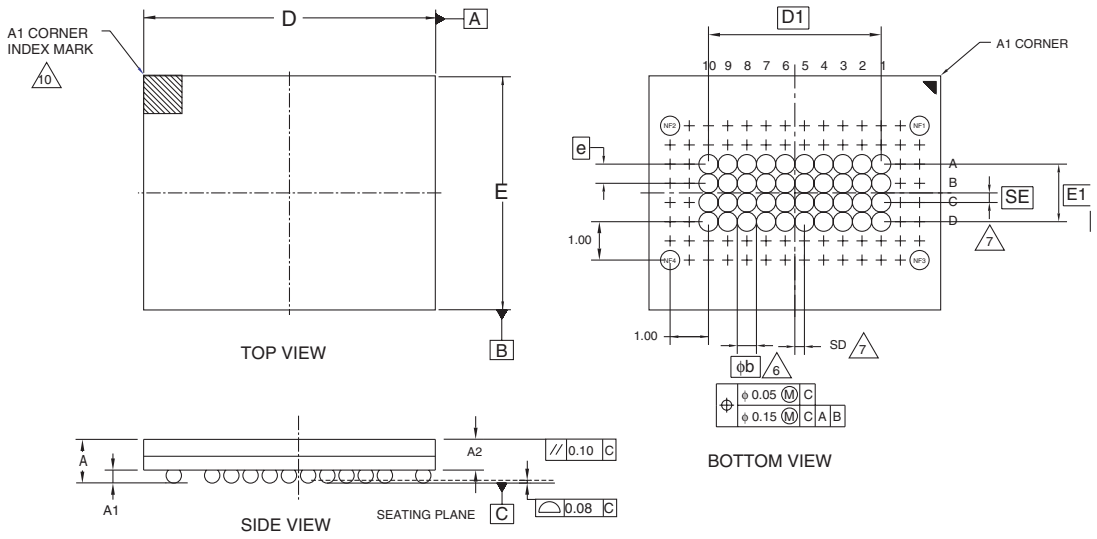
3239 \ 16-038.9h.aa01

Note

1. For reference only. BSC is an ANSI standard for Basic Space Centering.

17.3 S29NS032J and S29NS016J

VDE044—44-Ball Very Thin Fine-Pitch Ball Grid Array (FBGA) 7.7 x 6.2 mm Package



PACKAGE	VDE 044			
JEDEC	N/A			
	7.70 mm x 6.20 mm NOM PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	0.86	---	1.00	OVERALL THICKNESS
A1	0.20	---	---	BALL HEIGHT
A2	0.66	0.71	0.76	BODY THICKNESS
D	7.65	7.7	7.75	BODY SIZE
E	6.15	6.2	6.25	BODY SIZE
D1	4.50			BALL FOOTPRINT
E1	1.50			BALL FOOTPRINT
MD	10			ROW MATRIX SIZE D DIRECTION
ME	4			ROW MATRIX SIZE E DIRECTION
N	44			TOTAL BALL COUNT
φb	0.25	0.30	0.35	BALL DIAMETER
e	0.50 BSC.			BALL PITCH
SD / SE	0.25 BSC.			SOLDER BALL PLACEMENT
				DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.

   N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. NOT USED.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3308.1 \ 16-038.9L

Note

1. For reference only. BSC is an ANSI standard for Basic Space Centering.

18. Appendix A: Daisy Chain Information

Table 18.1 Daisy Chain Part for 128Mbit 110 nm Flash Products (VDC048, 10 x 11 mm)

Daisy Chain Part Number	Package Marking	Daisy Chain Connection	Spansion 128Mb Flash Part Number	Flash Description
Lead (Pb) - Free Compliant: AM29N128HVCD21CT	N128HD21C	Die Level	S29NS128J	128Mbit 110nm
Lead (Pb) - Free: Am29N128HVCD21CFT	N128HD21CF			

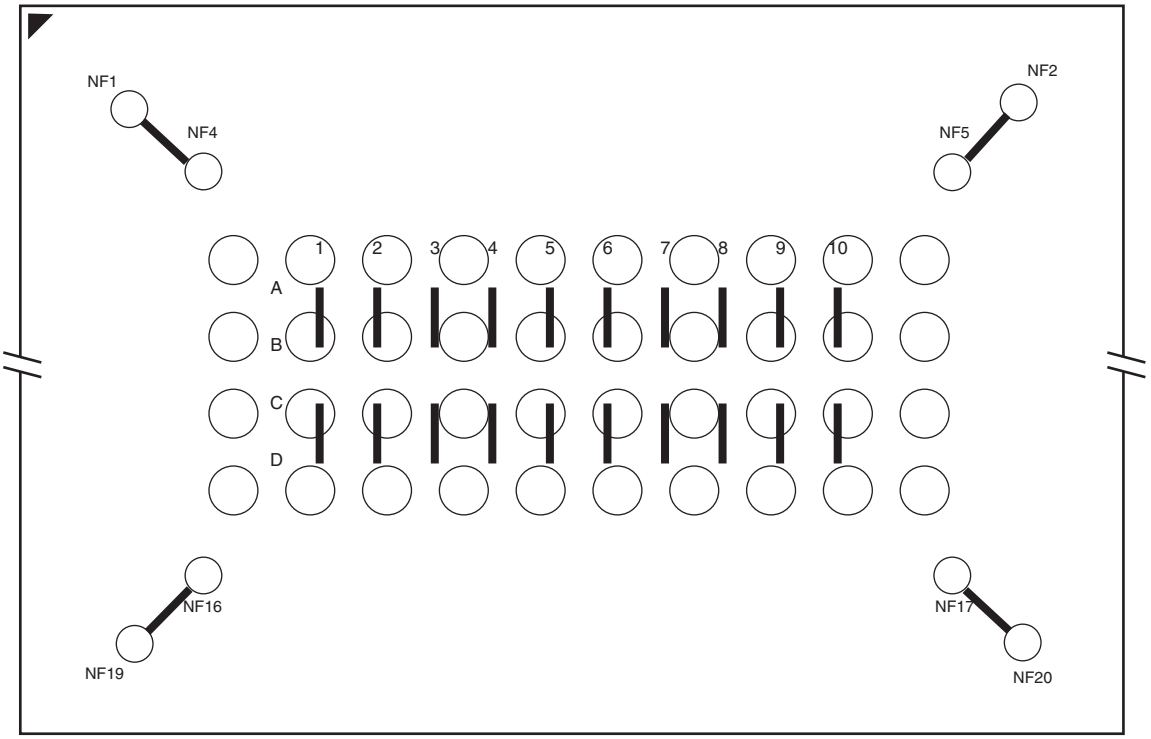
Table 18.2 VDC048 Package Information

Component Type/Name	VDC048
Solder resist opening	0.25 ± 0.05 mm
Daisy Chain Connection Level	On die
Lead-Free Compliant	Yes
Quantity per Reel	550 (300 units per reel by special request to factory)

Table 18.3 VDC048 Connections

C1–D1	C6–D6	A10–B10	A5–B5
C2–D2	C7–D7	A9–B9	A4–B4
C3–D3	C8–D8	A8–B8	A3–B3
C4–D4	C9–D9	A7–B7	A2–B2
C5–D5	C10–D10	A6–B6	A1–B1
On substrate			
NF1–NF4		NF2–NF5	
NF16-NF19		NF17-NF20	

Figure 18.1 VDC048 Daisy Chain Layout (Top View, Balls Facing Down)



19. Appendix B: Daisy Chain Information

Table 19.1 Daisy Chain Part for 64Mbit 110 nm Flash Products (VDD044, 9.2 x 8 mm)

Daisy Chain Part Number	Package Marking	Daisy Chain Connection	Spansion 64Mb Flash Part Number	Description
Lead (Pb) - Free Compliant: AM29N643GVAD21CT	N643GD21C	Die Level	S29NS064J	64Mbit 110nm
Lead (Pb)- Free: AM29N643GVAD21CFT	N643GD21CF			

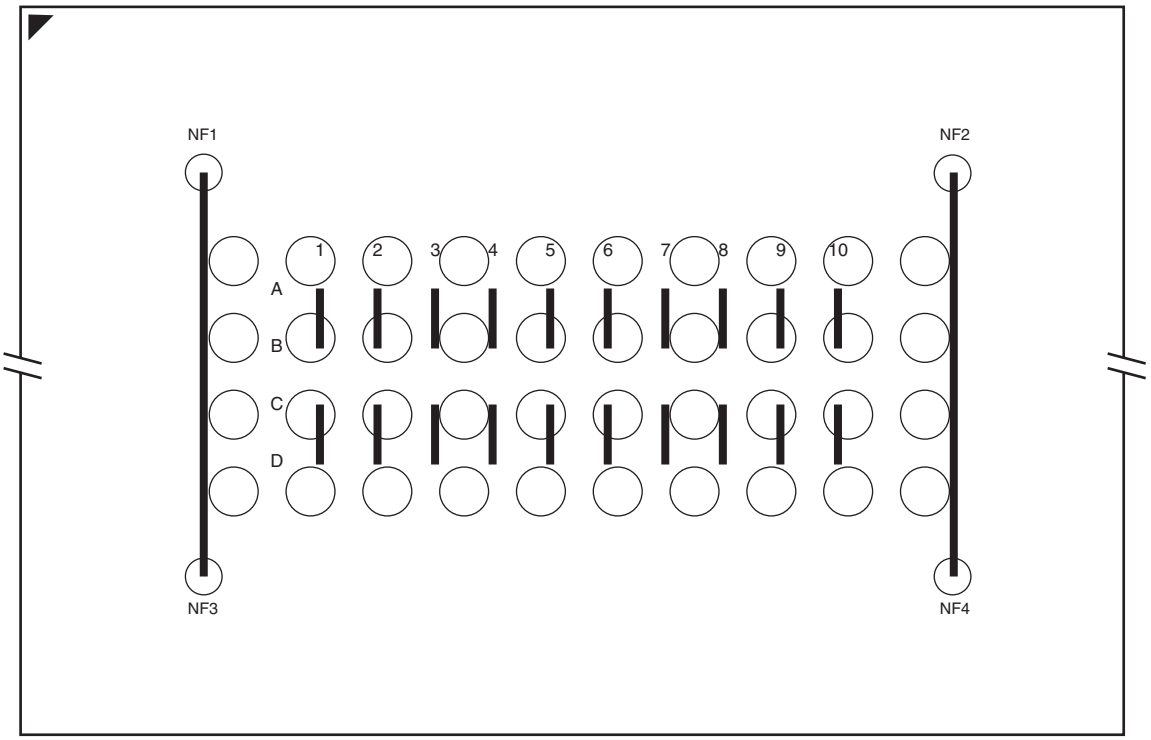
Table 19.2 VDD044 Package Information

Component Type/Name	VDD044
Solder resist opening	0.25 ± 0.05 mm
Daisy Chain Connection Level	On die
Lead-Free Compliant	Yes
Quantity per Reel	600 (300 units per reel by special request to factory)

Table 19.3 VDD044 Connections

C1–D1	C6–D6	A10–B10	A5–B5
C2–D2	C7–D7	A9–B9	A4–B4
C3–D3	C8–D8	A8–B8	A3–B3
C4–D4	C9–D9	A7–B7	A2–B2
C5–D5	C10–D10	A6–B6	A1–B1
On substrate			
NF1–NF3		NF2–NF4	

Figure 19.1 VDD044 Daisy Chain Layout (Top View, Balls Facing Down)



20. Appendix C: Daisy Chain Information

Table 20.1 Daisy Chain Part for 32 and 16 Mbit 110 nm Flash Products (VDE044, 7.7 x 6.2 mm)

Daisy Chain Part Number	Package Marking	Daisy Chain Connection	Spansion 64Mb Flash Part Number	Description
Lead (Pb) - Free Compliant: S99DCVDE044SDA002 Lead (Pb)- Free: S99DCVDE044SDF002	99DCVDE044SDA00 99DCVDE044SDF00	Die Level	S29NS032J S29NS016J	64Mbit 110nm 32Mbit 110nm

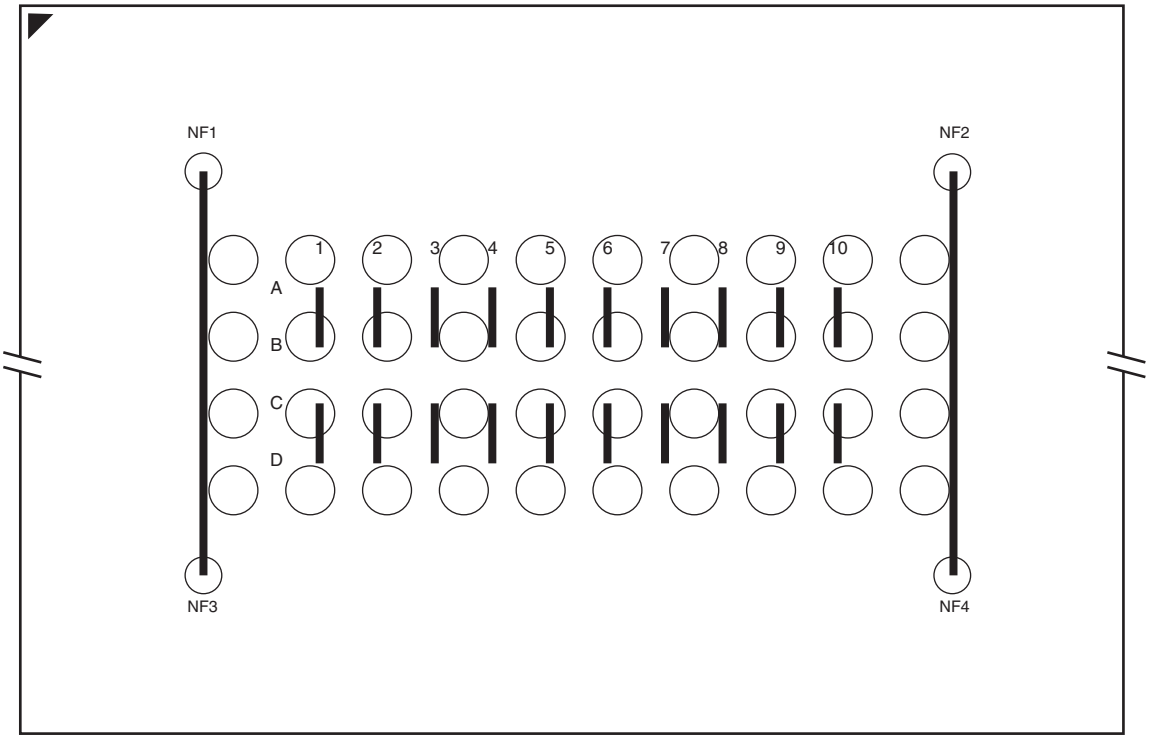
Table 20.2 VDE044 Package Information

Component Type/Name	VDE044
Solder resist opening	0.25 ± 0.05 mm
Daisy Chain Connection Level	On die
Lead-Free Compliant	Yes
Quantity per 7-inch Reel	600 (300 units per reel by special request to factory)

Table 20.3 VDE044 Connections

C1–D1	C6–D6	A10–B10	A5–B5
C2–D2	C7–D7	A9–B9	A4–B4
C3–D3	C8–D8	A8–B8	A3–B3
C4–D4	C9–D9	A7–B7	A2–B2
C5–D5	C10–D10	A6–B6	A1–B1
On substrate			
NF1–NF3		NF2–NF4	

Figure 20.1 VDE044 Daisy Chain Layout(Top View, Balls Facing Down)



21. Revision History

Section	Description
Revision A (May 16, 2003)	
	Initial release
Revision A1 (August 11, 2003)	
Connection Diagram	Modified Connection Diagrams for Am29N129J and S29NS064J.
Input/Output Descriptions	Changed VSS to GND, removed VCCQ and VSSQ.
Requirements for Synchronous (Burst) Read Operation, Continuous Burst	First paragraph, bold text, second sentence: the highest address changed to 000000h.
RESET#: Hardware Reset Input	Fourth paragraph: t_{READY} changed to t_{READYW}
Autoselect Command Sequence	Added Table 11 title, Autoselect Device ID
WP# Boot Sector Protection, Low VCC Write Inhibit, Table immediately preceding Program Command Sequence section	Modified Read Data for Device ID, Word 1, Device ID, Word 2 for S29NS064J only, Device ID, Word 3
Table 14, Command Definitions	Added Notes 10 and 12; changed BA = Address of the bank from A22-A20 to A22-A21 for S29NS128J, A21-A19 to A21-A20 for S29NS064J.
AC Characteristics CMOS Compatible	Added I_{CCW}, Typ and Max values for I_{PPW} and I_{CCW}; added I_{CCE}, Typ and Max values for I_{PPE} and I_{CCE}.
AC Characteristics, Figure 15, 16, 18, and 19	Changed AVD to AVD#
Revision A2 (August 19, 2003)	
Requirements for Synchronous (Burst) Read Operation	Modified bold text to indicate “highest address to 00000h”
Revision A3 (September 10, 2003)	
DC Characteristics, CMOS Compatible	Changed ICC3 and ICC4 Max values
Revision A4 (November 13, 2003)	
Global	Converted to Spansion format
Revision A5 (February 5, 2004)	
Ordering Information	Added 0L Clock rate/asynchronous speed. Updated Valid combinations to reflect addition
Appendix C and D	Added these sections
Revision A6 (April 7, 2004)	
Ordering Information	Removed Pb-Free Compliant options from 32 Megabit and 16 Megabit combinations for both 66 MHz and 54 MHz
Global	Corrected figure references
AC Characteristics	Modified the t_{READY} timing in Figure 14 in Hardware Reset (RESET#)
Erase and Programming Performance	Added density and typical values to Accelerated Chip Erase Time parameter.
Data Retention	Removed section
Revision A7 (August 4, 2004)	
Global	Changed all instances of “FASL” to “Spansion”. Added Colophon text.
Sector Erase Command Sequence	Replaced “” with “

Section	Description
Accelerated Sector Erase Groups, S29NS032J	Replaced “SA0–SA7” with “SA0–SA3”. Replaced “SA8–SA15” with “SA4–SA7”. Replaced “SA16–SA23” with “SA8–SA11”. Replaced “SA24–SA31” with “SA56–SA59”. Deleted “SA40–SA47”. Deleted “SA48–SA55”. Deleted “SA48–SA55”. Replaced “SA56–SA62” with “SA60–SA62”.
Accelerated Sector Erase Groups, S29NS016J	Replaced “SA0–SA7” with “SA0–SA1”. Replaced “SA8–SA15” with Replaced “SA16–SA23” with Replaced “SA24–SA30” with Added the following: SA8-SA9; SA10-SA11; SA12-SA13; SA14-SA15; SA16-SA17; SA18-SA19; SA20-SA21; SA22-SA23; SA24-SA25; SA26-SA27; SA28-SA29; SA30
Erase Suspend/Erase Resume Commands	Replaced “ Replaced “
DQ7: Data# Polling	Replaced “ Replaced “
DQ6: Toggle Bit I	Replaced “ Replaced “µ
DQ3: Sector Erase Timer	Replaced “
Erase and Programming Performance	Updated “Accelerated Chip Erase Time” as per the following: **Original** / **Updated** 128Mb: 45 / 50 64Mb: 30 / 25 32Mb: TBD / 12.5 16Mb: TBD / 6.25
Distinctive Characteristics	Deleted the following: “Minimum 100,000 erase cycle guarantee per sector”. “20-year data retention”. “Reliable operation for the life of the system”
Erase and Programming Performance	In Note 2 changed “100,000” to “1,000,000”
8-, 16-, and 32-Word Linear Burst Address Wrap Around	Updated drawing.
Unlock Bypass Command Sequence	Removed “The host system may also initiate the chip erase and sector erase sequences in the unlock bypass mode. The erase command sequences are four cycles in length instead of six cycles.”
Command Definitions	Removed the Unlock Bypass “sector erase” and “chip erase” rows.
Table 18, “Command Definitions”	Removed Unlock Bypass Sector Erase section. Removed Chip Erase section
WP# Boot Sector Protection	Updated 2nd paragraph as follows: “If using the Unlock Bypass feature: on the 2nd program cycle, after the Unlock Bypass command is written, the WP# signal must be asserted on the 2nd cycle.”
Global	Replaced all “AMD” references with “contact your local Spansion sales office”
Chip Erase Command Sequence	Removed “The host system may also initiate the chip erase command sequence while the device is in the unlock bypass mode. The command sequence is two cycles in length instead of six cycles
Sector Erase Command Sequence	Replaced “50 µs” with “Removed the following “The host system may also initiate the sector erase command sequence while the device is in the unlock bypass mode. The command sequence is four cycles in length instead of six cycles.

<table>
<tr><th>Section</th><th>Description</th></tr>
<tr><td>Erase/Program Operations</td><td>Removed the following rows from table:

<table>
<tr><td>t_{WHWH1}</td><td>t_{WHWH1}</td><td>Programming Operation</td><td>Typ</td><td>9</td><td>µs</td></tr>
<tr><td>t_{WHWH1}</td><td>t_{WHWH1}</td><td>Accelerated Programming Operation</td><td>Typ</td><td>4</td><td>µs</td></tr>
<tr><td>t_{WHWH2}</td><td>t_{WHWH2}</td><td>Sector Erase Operation</td><td>Typ</td><td>0.4</td><td>sec</td></tr>
</table>
</td></tr>
<tr><td colspan="2">Revision A8 (September 14, 2004)</td></tr>
<tr><td>Ordering Information</td><td>Added packing types 0 and 2.</td></tr>
<tr><td>Valid Combinations</td><td>Added Packing Type information</td></tr>
<tr><td colspan="2">Revision A9 (November 11, 2005)</td></tr>
<tr><td>Ordering Information</td><td>Added LF35 package ordering option</td></tr>
<tr><td colspan="2">Revision A10 (March 22, 2006)</td></tr>
<tr><td>Global</td><td>Changed V_{PP} to ACC.</td></tr>
<tr><td>AC Characteristics</td><td>Asynchronous Read table: updated the values of t_{AAVDH} for both speed bins.</td></tr>
<tr><td colspan="2">Revision A11 (February 7, 2007)</td></tr>
<tr><td>Global</td><td>Updated document to new template.
Removed 66 MHz option</td></tr>
</table>

Colophon

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