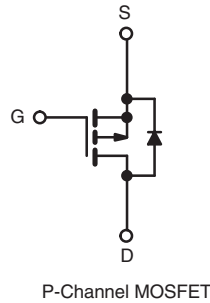
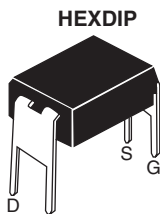


## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	- 100	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = -10$ V	1.2
$Q_g$ (Max.) (nC)	8.7	
$Q_{gs}$ (nC)	2.2	
$Q_{gd}$ (nC)	4.1	
Configuration	Single	



### FEATURES

- Dynamic  $dV/dt$  Rating
- Repetitive Avalanche Rated
- For Automatic Insertion
- End Stackable
- P-Channel
- 175 °C Operating Temperature
- Fast Switching
- Lead (Pb)-free Available



Available  
**RoHS\***  
COMPLIANT

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4 pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.

ORDERING INFORMATION	
Package	HEXDIP
Lead (Pb)-free	IRFD9110PbF
	SiHFD9110-E3
SnPb	IRFD9110
	SiHFD9110



ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	- 100	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current	$V_{GS}$ at - 10 V	$T_C = 25$ °C	- 0.70	A
		$T_C = 100$ °C	- 0.49	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	- 5.6		
Linear Derating Factor		0.0083	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	140	mJ	
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	- 0.7	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	0.13	mJ	
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	1.3	W
Peak Diode Recovery $dV/dt^c$	$dV/dt$	- 5.5	V/ns	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 175	°C	
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>		

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = -25$  V, starting  $T_J = 25$  °C,  $L = 52$  mH,  $R_G = 25$   $\Omega$ ,  $I_{AS} = -2.0$  A (see fig. 12).
- $I_{SD} \leq -4.0$  A,  $dI/dt \leq 75$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 175$  °C.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	120	°C/W

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$		- 100	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = -1\text{ mA}$		-	- 0.091	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$		- 2.0	-	- 4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}$		-	-	- 100	$\mu\text{A}$
		$V_{DS} = -80\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$		-	-	- 500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -0.42\text{ A}^b$	-	-	1.2	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = -50\text{ V}, I_D = -0.42\text{ A}$		0.60	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = -25\text{ V},$ $f = 1.0\text{ MHz}$ , see fig. 5		-	200	-	$\mu\text{F}$
Output Capacitance	$C_{oss}$			-	94	-	
Reverse Transfer Capacitance	$C_{rss}$			-	18	-	
Total Gate Charge	$Q_g$	$V_{GS} = -10\text{ V}$	$I_D = -4.0\text{ A}, V_{DS} = -80\text{ V}$ see fig. 6 and 13 <sup>b</sup>	-	-	8.7	nC
Gate-Source Charge	$Q_{gs}$			-	-	2.2	
Gate-Drain Charge	$Q_{gd}$			-	-	4.1	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -50\text{ V}, I_D = -4.0\text{ A}$ $R_G = 24\text{ }\Omega, R_D = 11\text{ }\Omega,$ see fig. 10 <sup>b</sup>		-	10	-	ns
Rise Time	$t_r$			-	27	-	
Turn-Off Delay Time	$t_{d(off)}$			-	15	-	
Fall Time	$t_f$			-	17	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.0	-	nH
Internal Source Inductance	$L_S$			-	6.0	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	- 0.70	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	- 5.6	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = -0.7\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	- 5.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = -4.0\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	82	160	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.15	0.30	$\mu\text{C}$

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

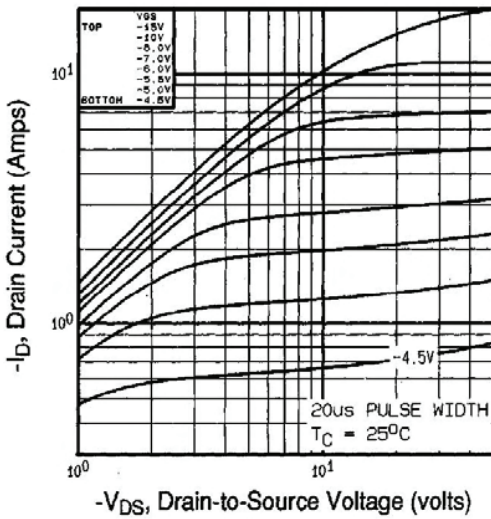


Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ\text{C}$

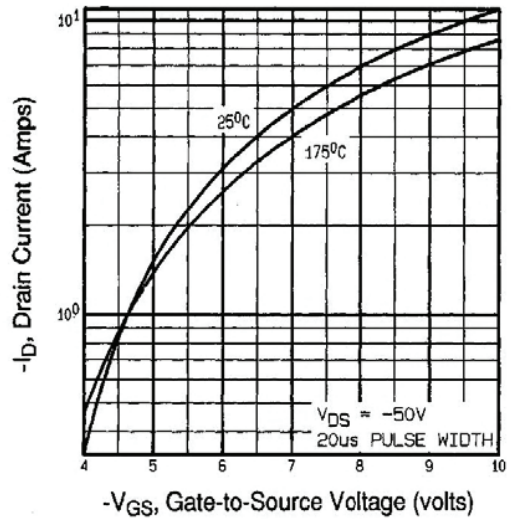


Fig. 3 - Typical Transfer Characteristics

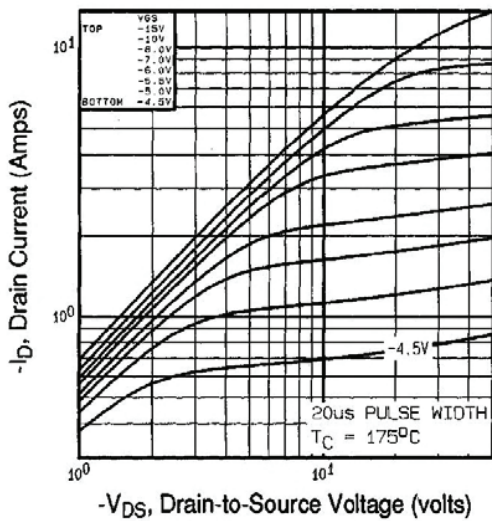


Fig. 2 - Typical Output Characteristics,  $T_C = 175^\circ\text{C}$

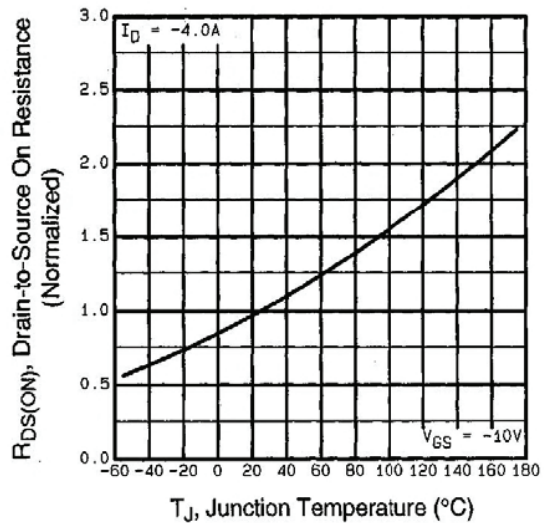


Fig. 4 - Normalized On-Resistance vs. Temperature

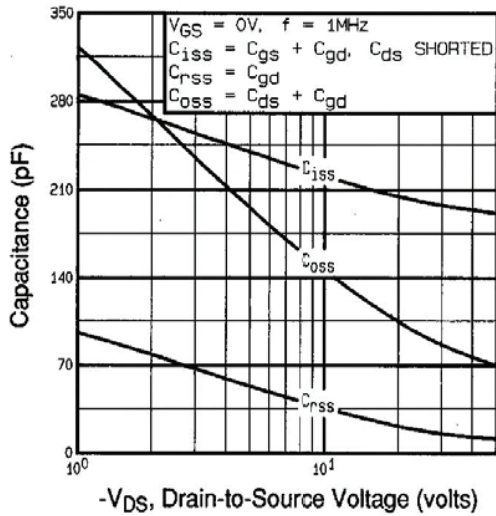


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

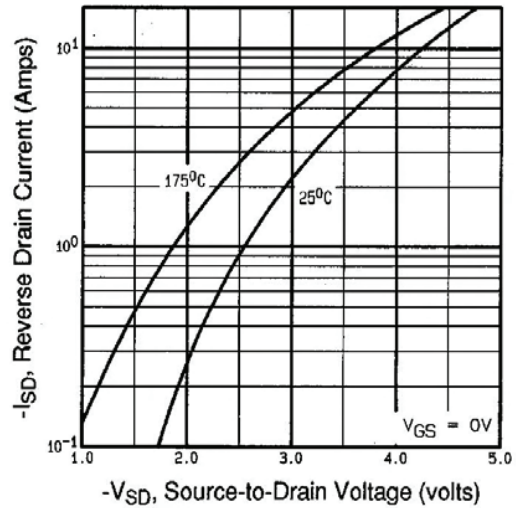


Fig. 7 - Typical Source-Drain Diode Forward Voltage

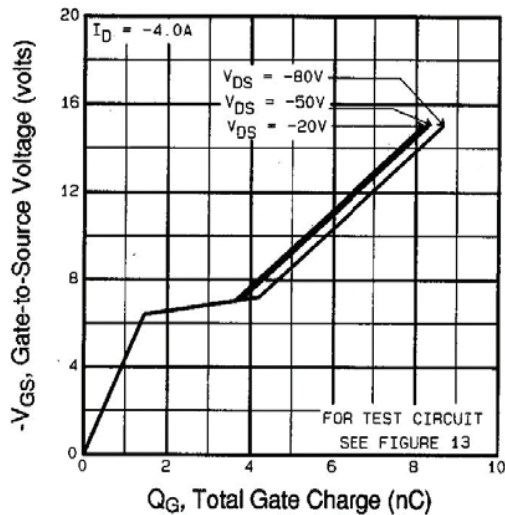


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

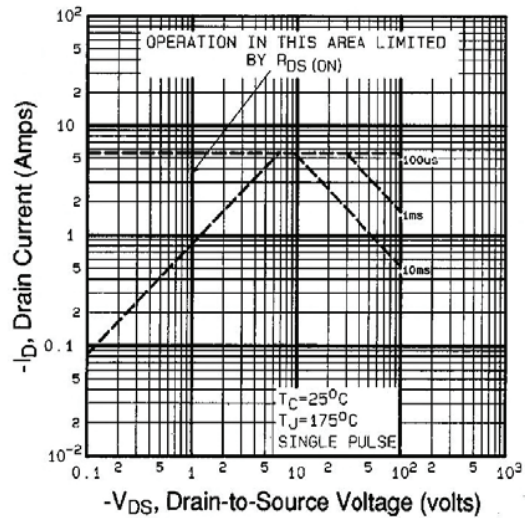


Fig. 8 - Maximum Safe Operating Area

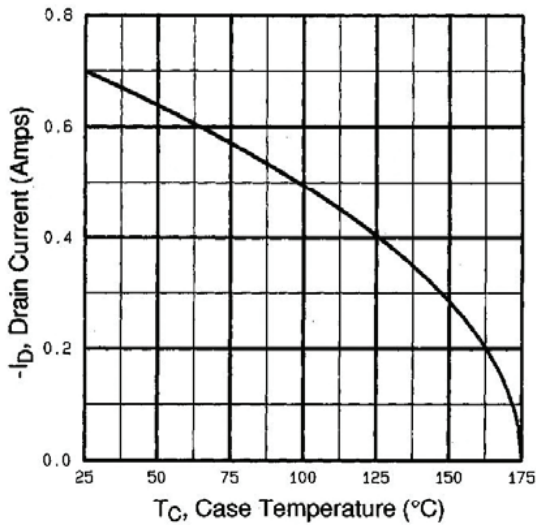


Fig. 9 - Maximum Drain Current vs. Case Temperature

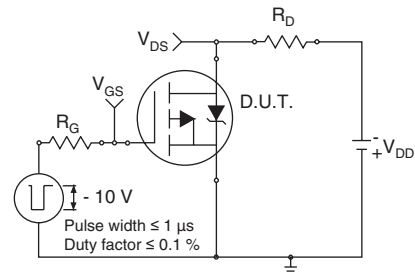


Fig. 10a - Switching Time Test Circuit

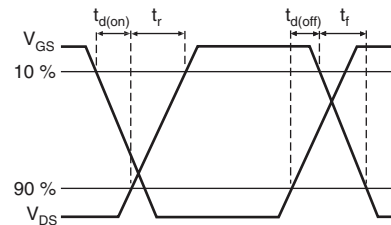


Fig. 10b - Switching Time Waveforms

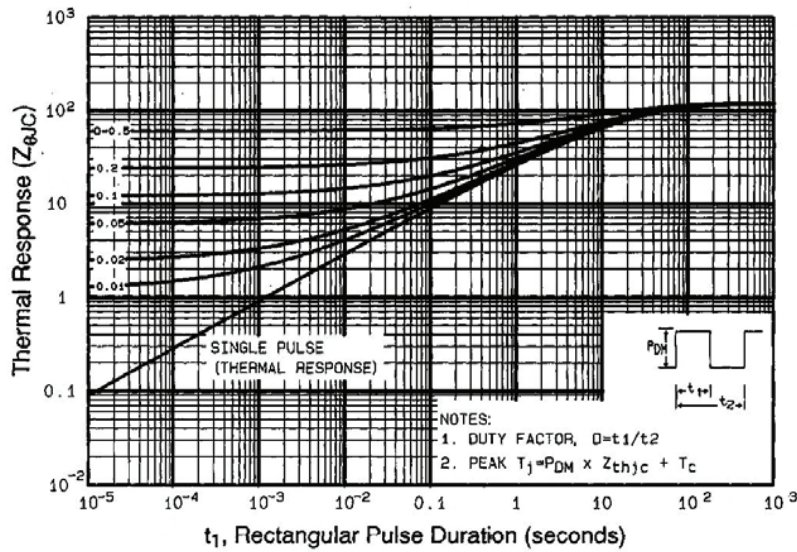


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

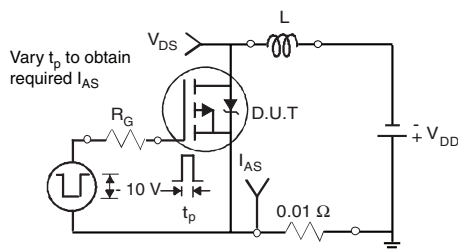


Fig. 12a - Unclamped Inductive Test Circuit

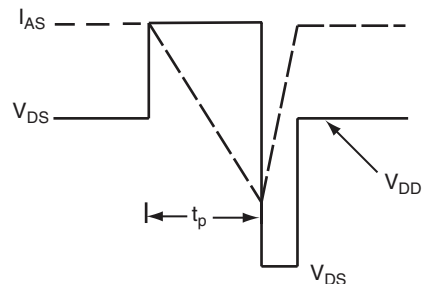


Fig. 12b - Unclamped Inductive Waveforms

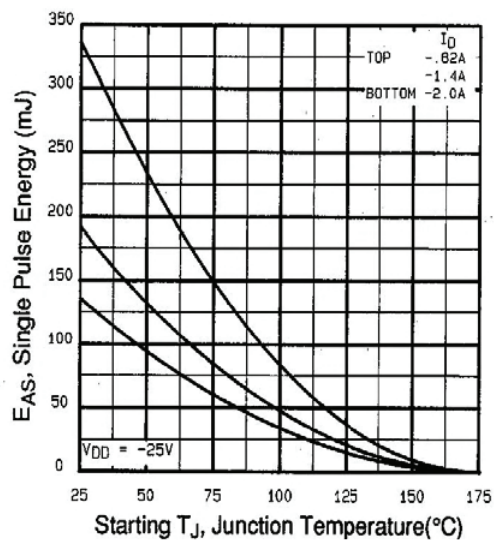


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

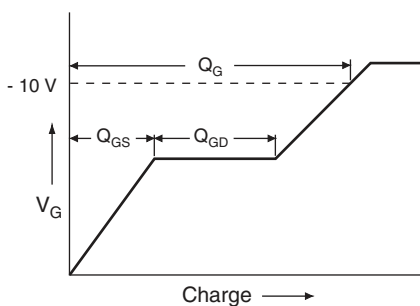


Fig. 13a - Basic Gate Charge Waveform

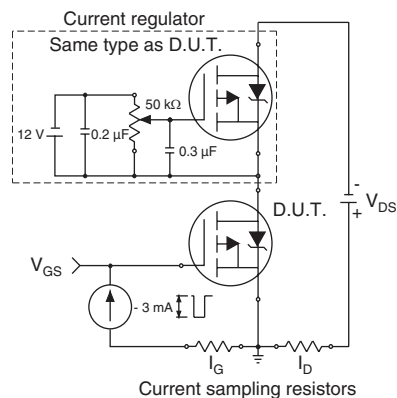
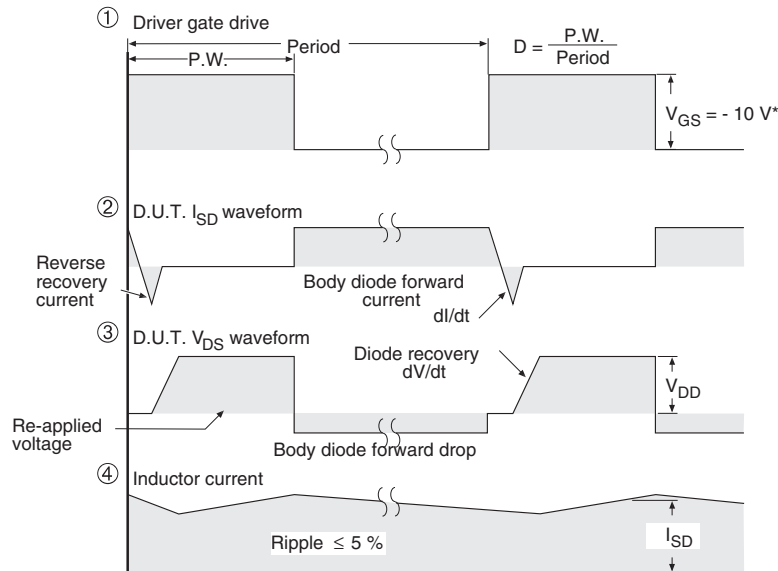
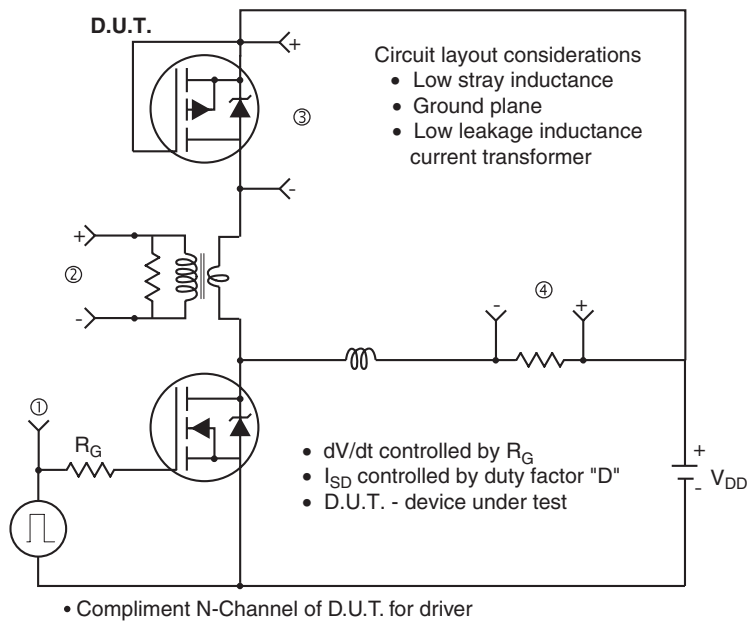


Fig. 13b - Gate Charge Test Circuit

**Peak Diode Recovery dV/dt Test Circuit**


\*  $V_{GS} = -5 V$  for logic level and  $-3 V$  drive devices

**Fig. 14 - For P-Channel**

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