Features

General
- **High-performance, Low-power secure AVR® RISC Architecture**
  - **137 Powerful Instructions (Most Executed in a Single Clock Cycle)**
- **Low Power Idle and Power-down Modes**
- **Bond Pad Locations Conforming to ISO 7816-2**
- **ESD Protection to ± 6000V**
- **Operating Ranges: 2.7V to 5.5V**
- **Compliant with GSM, 3GPP and EMV 2000 Specifications; PC Industry Compatible**
- **Available in Wafers, Modules, and Industry-standard Packages**

Memory
- **320K Bytes of ROM Program Memory**
- **288K Bytes of EEPROM, Including 128 OTP Bytes and 384-byte Bit-addressable Area**
  - **1 to 128-byte Program / Erase**
  - **1.25 ms Program / 1.25 ms Erase**
  - **Typically More than 500,000 Write/Erase Cycles at a Temperature of 25°C**
  - **10 Years Data Retention**
  - **EEPROM Erase Only Mode**
  - **Write EEPROM With or Without Autoerase**
- **8K Bytes of RAM**
- **32K Bytes of ROM Dedicated to Atmel's Crypto-library**

Peripherals
- **Two I/O Ports**
  - **Configurable to Support Communication Protocols, Including ISO7816-3 and 2-wire protocols**
- **ISO7816 Controller**
  - **Up to 625 kbps at 5 MHz**
  - **Compliant with T=0 and T=1 Protocols**
- **Serial Peripheral Interface (SPI) Contoller (up to 12 MHz)**
- **Programmable Internal Oscillator**
  - **Up to 20 MHz on ROM**
  - **Up to 40 MHz for Cryptographic Accelerator**
- **Two 16-bit Timers**
- **Random Number Generator (RNG)**
- **2-level, 8-vector Interrupt Controller**
- **32-bit Cryptographic Accelerator for Public Key Operations Including**
  - **RSA, DSA, ECC, Diffie-Hellman**
- **Hardware DES and Triple DES (DPA Resistant)**
- **Checksum Accelerator**
- **CRC 16 and 32 Engine (Compliant with ISO/IEC 3309)**

Security
- **Dedicated Hardware for Protection Against SPA/DPA Attacks**
- **Advanced Protection Against Physical Attack, Including Active Shield**
- **Environmental Protection Systems**
- **Voltage Monitor**
- **Frequency Monitor**
- **Light Protection**
- **Temperature Monitor**
- **Secure Memory Management/Access Protection (Supervisor Mode)**

Secure Microcontroller for Smart Cards

AT90SC 320288RCT Summary

6507CS–SCIC–20Dec06

Note: This is a summary document. A complete document will be available under NDA. For more information, please contact your local Atmel sales office.

Development Tools

- **Voyager Emulation Platform (ATV4 Standard) to Support Software Development**
- **IAR Embedded Workbench® V3.20c Debugger or Atmel's AVR Studio® Version 4.07 or Above**
- **Software Libraries and Application Notes**

Certification

- **EAL4+**
- **VISA**
- **CAST**
- **FIPS**

Description

The AT90SC320288RCT is a low-power, high-performance, 8/16-bit microcontroller with ROM program memory, EEPROM data memory, based on the secureAVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the AT90SC320288RCT achieves throughputs close to 1 MIPS per MHz. Its Harvard architecture includes 32 general-purpose working registers directly connected to the ALU, allowing two independent registers to be accessed in one single instruction executed in one clock cycle.

The ability to map the EEPROM in the code space allows parts of the program memory to be reprogrammed in-system. This technology combined with the versatile 8/16-bit CPU on a monolithic chip provides a highly flexible and cost-effective solution to many smart card applications. The AT90SC320288RCT benefits of advanced EEPROM functions (XP Mode), but can also be configured to offer compatibility with previous product generations (e.g. AT90SC25672R or AT90SC19236R).

The cryptographic accelerator, running with the secureAVR core, featured in the AT90SC320288RCT series is the new AdvX‰. It is based on a 32-bit multiplier-accumulator architecture which is designed to perform fast encryption and authentication functions. This enables fast computation and low-power operation. The controlling firmware is located either in the dedicated ROM memory (Atmel's cryptolibrary supports standard finite field arithmetic functions including RSA, DSA, DH and ECC) or in the ROM program memory (customer specific).

Additional security features include power and frequency protection logic, logical scrambling on program data and addresses, Power Analysis countermeasures and memory accesses controlled by a supervisor mode.

Figure 1 shows the AT90SC320288RCT block diagram.

Figure 1. AT90SC320288RCT secureAVR Enhanced RISC Architecture
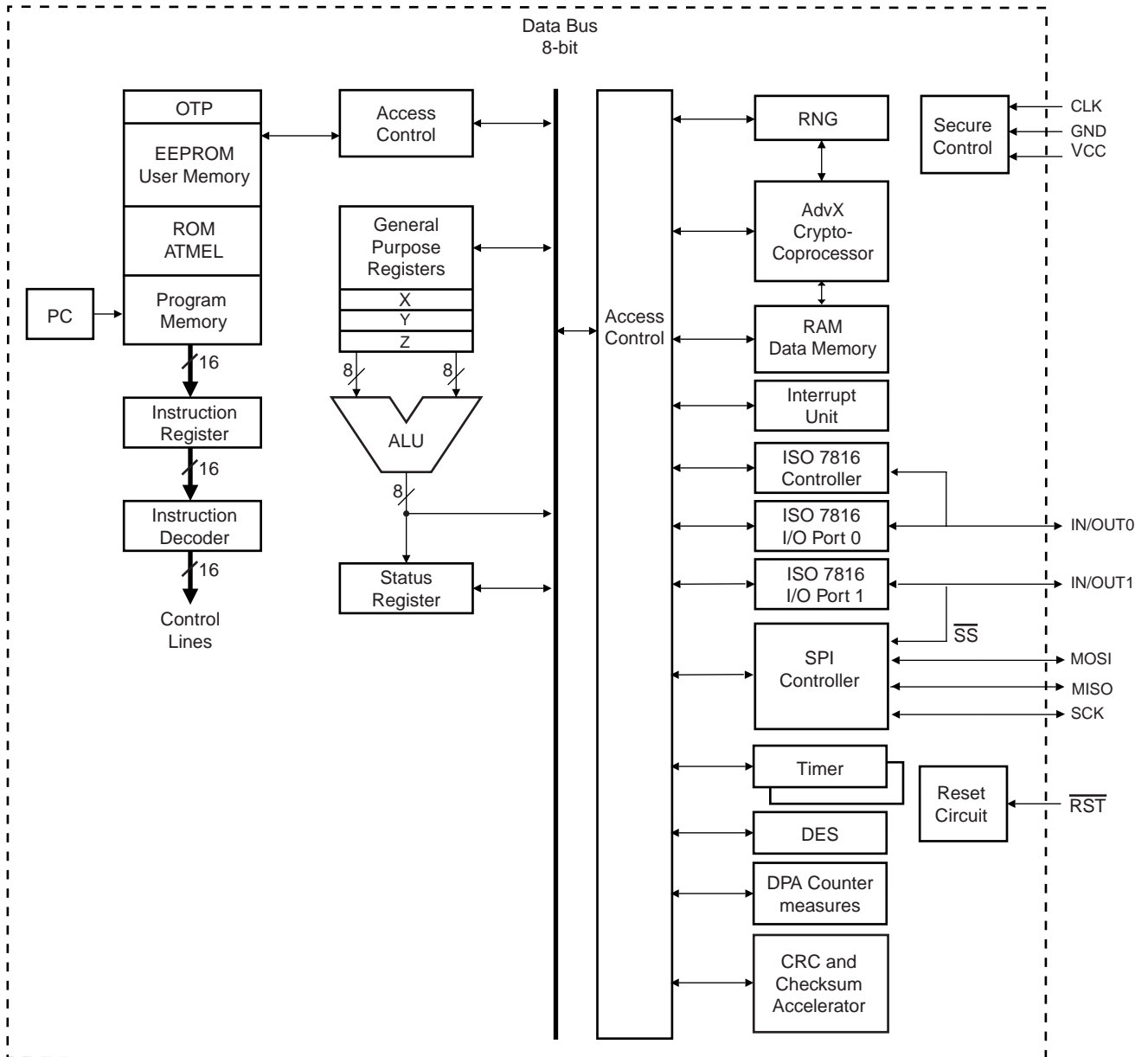
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