1. General Description

This ROM-Based 8-bit micro-controller uses a fully static CMOS technology process to achieve high speed, small size, the low power and high noise immunity.

On chip memory includes 2K words EPROM, and 80 bytes static RAM.

2. Features

The followings are some of the features on the hardware and software :

- Fully CMOS static design
- 8-bit data bus
- On chip EPROM size : 2.0 K words
- Internal RAM size : 80 bytes
  (73 general purpose registers, 7 special registers)
- 36 single word instructions
- 14-bit instructions
- 2-level stacks
- Operating voltage : 2.3 V ~ 6.0 V
- Operating frequency : 0 ~ 20 MHz
- The most fast execution time is 200 ns under 20 MHz in all single cycle instructions except the branch instruction
- Addressing modes include direct, indirect and relative addressing modes
- Power-on Reset (POR),only available while PED is Disable
- Power edge-detector Reset
- Sleep Mode for power saving
- 4 types of oscillator can be selected by programming option:
  RC－Low cost RC oscillator
  LFXT－Low frequency crystal oscillator
  XTAL－Standard crystal oscillator
  HFXT－High frequency crystal oscillator
- 4 oscillator start-up time can be selected by programming option:
  150 μs, 20 ms, 40 ms, 80 ms
- 8-bit real time clock/counter(RTCC) with 8-bit programmable prescaler
- On-chip RC oscillator based Watchdog Timer(WDT)
- 12 I/O pins with their own independent direction control

3. Applications

The application areas of this MDT2030 range from appliance motor control and high speed automotive to low power remote transmitters /receivers, pointing devices, and telecommunications processors, such as Remote controller, small instruments, chargers, toy, automobile and PC peripheral … etc.

4. Pin Assignment

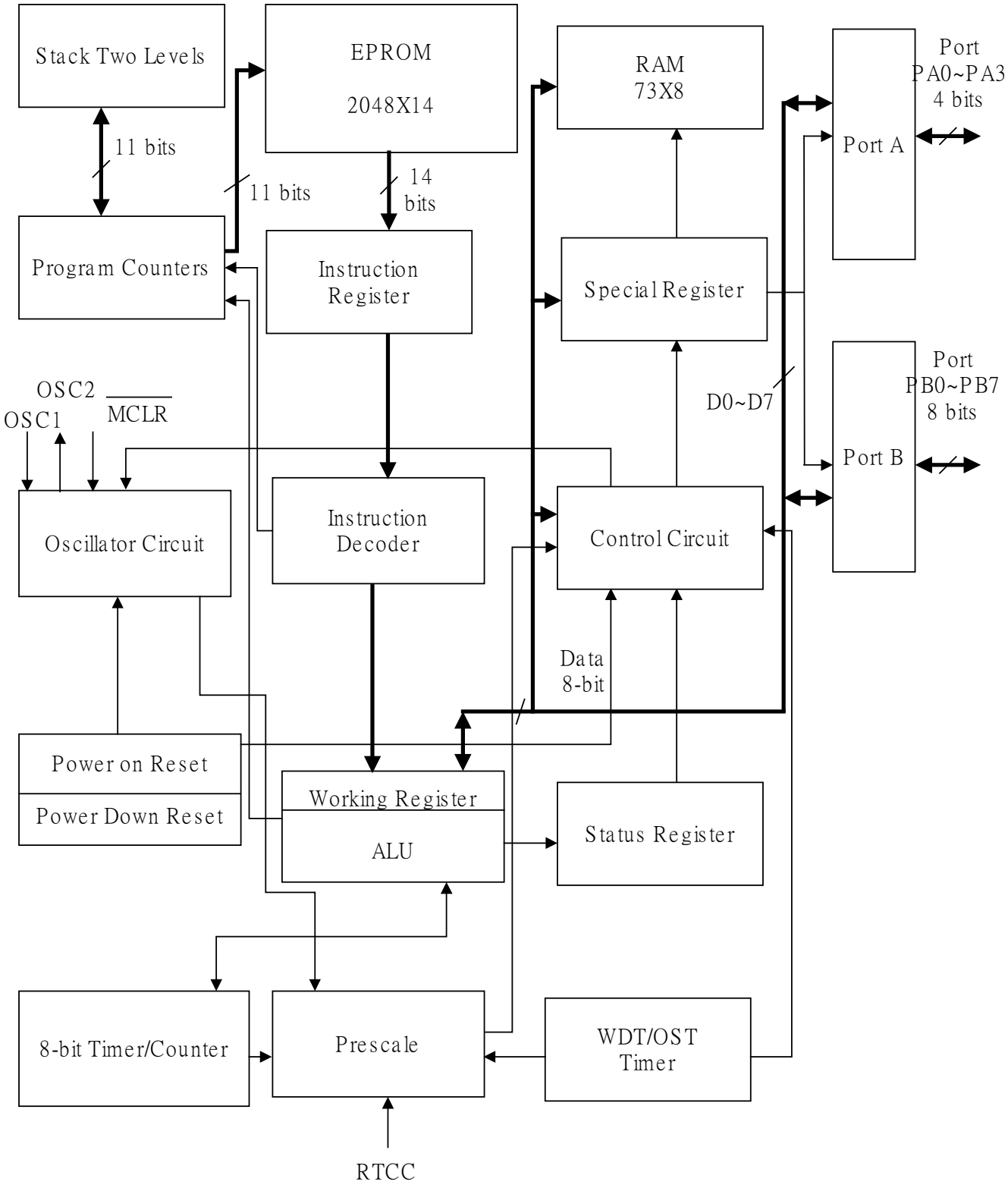
DIP / SOP

PA2	1	18	PA1
PA3	2	17	PA0
RTCC	3	16	OSC1
/MCLR	4	15	OSC2
V_{ss}	5	14	V_{dd}
PB0	6	13	PB7
PB1	7	12	PB6
PB2	8	11	PB5
PB3	9	10	PB4

SSOP

PA2	1	20	PA1
PA3	2	19	PA0
RTCC	3	18	OSC1
/MCLR	4	17	OSC2
VSS	5	16	VDD
VSS	6	15	VDD
PB0	7	14	PB7
PB1	8	13	PB6
PB2	9	12	PB5
PB3	10	11	PB4

5. Block Diagram



6. Pin Function Description

Pin Name	I/O	Function Description
PA0~PA3	I/O	Port A, TTL input level
PB0~PB7	I/O	Port B, TTL input level
RTCC	I	Real Time Clock/Counter, Schmitt Trigger input levels
/MCLR	I	Master Clear, Schmitt Trigger input levels
OSC1	I	Oscillator Input
OSC2	O	Oscillator Output
V_{dd}		Power supply
V_{ss}		Ground

7. Memory Map

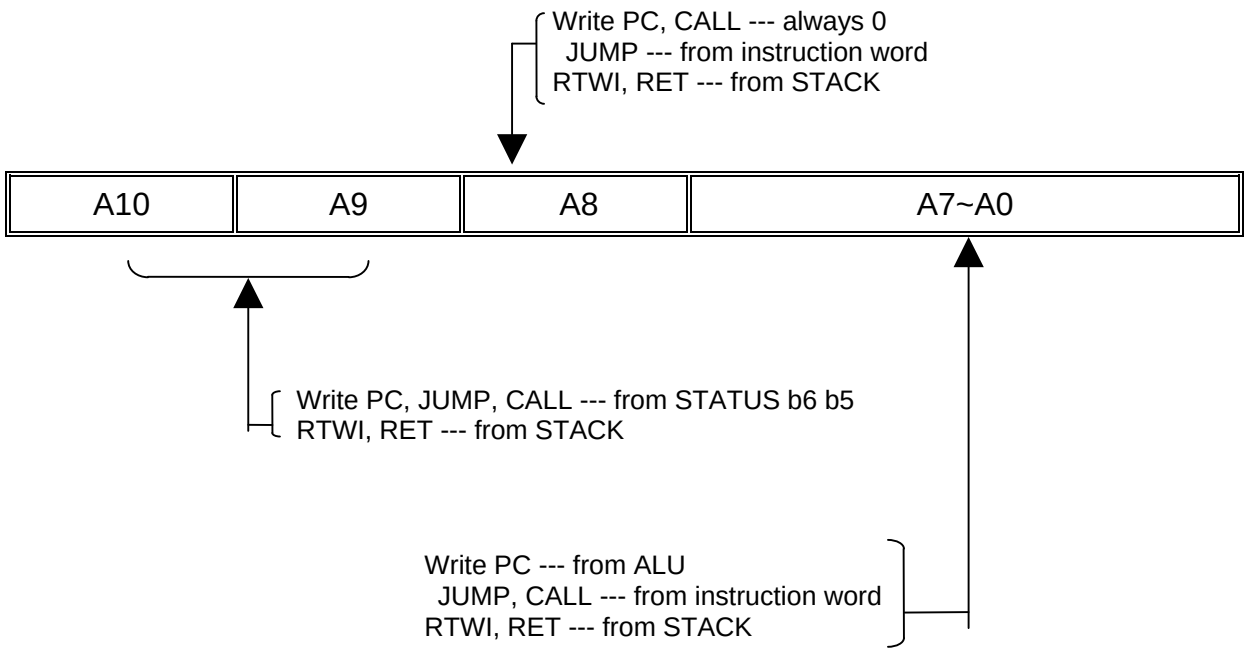
(A) Register Map

Address	Description
00	Indirect Addressing Register
01	RTCC
02	PC
03	STATUS
04	MSR
05	Port A
06	Port B
07~1F	Internal RAM, Memory bank 0
30~3F	Internal RAM, Memory bank 1
50~5F	Internal RAM, Memory bank 2
70~7F	Internal RAM, memory bank 3

(1) IAR (Indirect Address Register) : R0

(2) RTCC (Real Time Counter/Counter Register) : R1

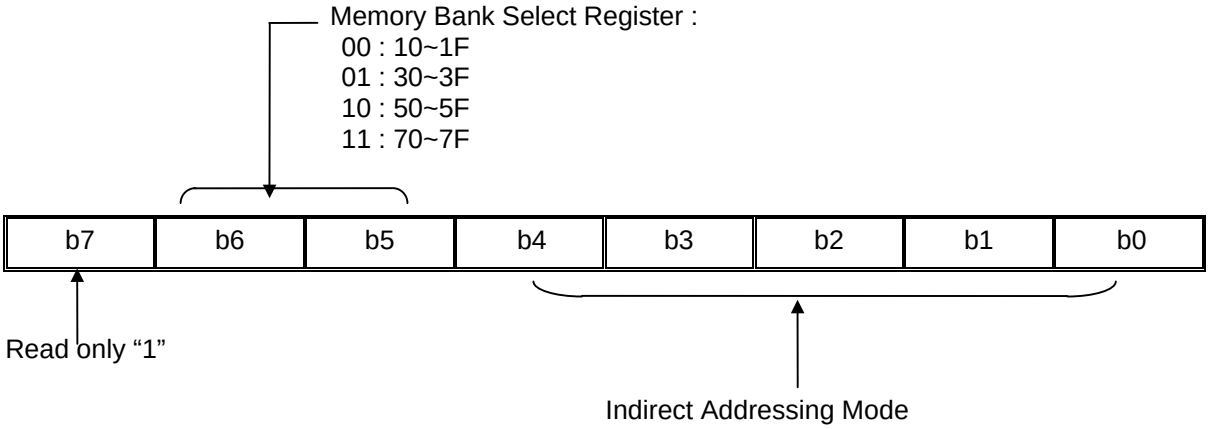
(3) PC (Program Counter) : R2



(4) STATUS (Status register) : R3

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	PF	Power loss Flag bit
4	TF	WDT Timer overflow Flag bit
6—5	page	ROM page select bit : 00 : Page 0, 000H --- 1FFH 01 : Page 1, 200H --- 3FFH 10 : Page 2, 400H --- 5FFH 11 : Page 3, 600H --- 7FFH
7	——	General purpose bit

(5) MSR (Memory Bank Select Register) : R4



(6) PORT A : R5

PA3~PA0, I/O Register

(7) PORT B : R6

PB7~PB0, I/O Register

(8) TMR (Time Mode Register)

Bit	Symbol	Function		
		Prescaler Value	RTCC rate	WDT rate
2—0	PS2—0	0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 1 0	1 : 128	1 : 64
		1 1 1	1 : 256	1 : 128
3	PSC	Prescaler assignment bit : 0 — RTCC 1 — Watchdog Timer		
4	TCE	RTCC signal Edge : 0 — Increment on low-to-high transition on RTCC pin 1 — Increment on high-to-low transition on RTCC pin		
5	TCS	RTCC signal set : 0 — Internal instruction cycle clock 1 — Transition on RTCC pin		

(9) CPIO A, CPIO B (Control Port I/O Mode Register)

The CPIO register is "write-only"

＝"0", I/O pin in output mode;

＝"1", I/O pin in input mode.

(10) Configurable options for EPROM (Set by writer) :

Oscillator Type	Oscillator Start-up Time
RC Oscillator	150 μs,20ms,40ms,80ms
HFXT Oscillator	20 ms,40ms,80ms
XTAL Oscillator	20ms,40 ms,80ms
LFXT Oscillator	40 ms,80 ms

Watchdog Timer control
Watchdog timer disable all the time
Watchdog timer enable all the time

Power Edge Detect
PED Disable
PED Enable

Security state
Security weak Disable
Security Disable
Security Enable

The default security state of EPROM is weak disable. Once the IC was set to enable or disable, it's forbidden to change.

(B) Program Memory

Address	Description
000-7FF	Program memory
7FF	The starting address of power on, external reset or WDT time-out reset.

8. Reset Condition for all Registers

Register	Address	Power-On Reset	/MCLR or WDT Reset
CPIO A	— —	1111 1111	1111 1111
CPIO B	— —	1111 1111	1111 1111
TMR	— —	--11 1111	--11 1111
IAR	00h	—	—
RTCC	01h	xxxx xxxx	uuuu uuuu
PC	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	000# #uuu
MSR	04h	100x xxxx	100u uuuu

Register	Address	Power-On Reset	/MCLR or WDT Reset
PORT A	05h	- - - - xxxx	- - - - uuuu
PORT B	06h	xxxx xxxx	uuuu uuuu

Note : u＝unchanged, x＝unknown, - ＝unimplemented, read as “0”

#＝value depends on the condition of the following table

Condition	Status: bit 4	Status: bit 3
/MCLR reset (not during SLEEP)	u	u
/MCLR reset during SLEEP	1	0
WDT reset (not during SLEEP)	0	1
WDT reset during SLEEP	0	0

9. Instruction Set :

Instruction Code	Mnemonic Operands	Function	Operating	Status
010000 00000000	NOP	No operation	None	
010000 00000001	CLRWT	Clear Watchdog timer	0→WT	TF, PF
010000 00000010	SLEEP	Sleep mode	0→WT, stop OSC	TF, PF
010000 00000011	TMODE	Load W to TMODE register	W→TMODE	None
010000 00000100	RET	Return	Stack→PC	None
010000 00000rrr	CPIO R	Control I/O port register	W→CPIO r	None
010001 1rrrrrrr	STWR R	Store W to register	W→R	None
011000 trrrrrrr	LDR R, t	Load register	R→t	Z
111010 iiiiiiii	LDWI I	Load immediate to W	I→W	None
010111 trrrrrrr	SWAPR R, t	Swap halves register	[R(0~3) ↔R(4~7)] →t	None
011001 trrrrrrr	INCR R, t	Increment register	R + 1→t	Z
011010 trrrrrrr	INCRSZ R, t	Increment register, skip if zero	R + 1→t	None
011011 trrrrrrr	ADDWR R, t	Add W and register	W + R→t	C, HC, Z
011100 trrrrrrr	SUBWR R, t	Subtract W from register	R – W→t or (R+/W+1→t)	C, HC, Z
011101 trrrrrrr	DECR R, t	Decrement register	R – 1→t	Z
011110 trrrrrrr	DECRSZ R, t	Decrement register, skip if zero	R – 1→t	None
010010 trrrrrrr	ANDWR R, t	AND W and register	R ∩ W→t	Z
110100 iiiiiiii	ANDWI i	AND W and immediate	i ∩ W→W	Z
010011 trrrrrrr	IORWR R, t	Inclu. OR W and register	R ∪ W→t	Z
110101 iiiiiiii	IORWI i	Inclu. OR W and immediate	i ∪ W→W	Z

Instruction Code	Mnemonic Operands	Function	Operating	Status
010100 trrrrrrr	XORWR R, t	Exclu. OR W and register	R ⊕ W→t	Z
110110 iiiiiiii	XORWI i	Exclu. OR W and immediate	i ⊕ W→W	Z
011111 trrrrrrr	COMR R, t	Complement register	/R→t	Z
010110 trrrrrrr	RRR R, t	Rotate right register	R(n) →R(n-1), C→R(7), R(0)→C	C
010101 trrrrrrr	RLR R, t	Rotate left register	R(n)→r(n+1), C→R(0), R(7)→C	C
010000 1xxxxxxx	CLRW	Clear working register	0→W	Z
010001 0rrrrrrr	CLRR R	Clear register	0→R	Z
0000bb brrrrrrr	BCR R, b	Bit clear	0→R(b)	None
0010bb brrrrrrr	BSR R, b	Bit set	1→R(b)	None
0001bb brrrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if R(b)=0	None
0011bb brrrrrrr	BTSS R, b	Bit Test, skip if set	Skip if R(b)=1	None
1000nn nnnnnnnn	LCALL n	Long CALL subroutine	n→PC, PC+1→Stack	None
1010nn nnnnnnnn	LJUMP n	Long JUMP to address	n→PC	None
110000 nnnnnnnn	CALL n	Call subroutine	n→PC, PC+1→Stack	None
110001 iiiiiiii	RTWI i	Return, place immediate to W	Stack→PC,i→W	None
11001n nnnnnnnn	JUMP n	JUMP to address	n→PC	None

Note :

W	:	Working register	b	:	Bit position
WT	:	Watchdog timer	t	:	Target
TMODE	:	TMODE mode register		0	: Working register
CPIO	:	Control I/O port register		1	: General register
TF	:	Timer overflow flag	R	:	General register address
PF	:	Power loss flag	C	:	Carry flag
PC	:	Program Counter	HC	:	Half carry
OSC	:	Oscillator	Z	:	Zero flag
Inclu.	:	Inclusive '∪'	/	:	Complement
Exclu.	:	Exclusive '⊕'	x	:	Don't care
AND	:	Logic AND '∩'	i	:	Immediate data (8 bits)
			n	:	Immediate address

10. Electrical Characteristics

(Operating temperature at 25℃).

Sym	Description	Condition	Min	Typ	Max	Unit
Vdd	Operating voltage		2.3		6.0	V
V_{IL}	Input Low Voltage					
	PA, PB	Vdd=5V	-0.6		1.0	V
	RTCC, /MCLR	Vdd=5V	-0.6		1.0	V
V_{IH}	Input high Voltage					
	PA, PB	Vdd=5V	2.0		Vdd	V
	RTCC, /MCLR	Vdd=5V	3.3		Vdd	V
I_{IL}	Input leakage current	Vdd=5V			+/-1	μA
V_{OL}	Output Low Voltage					
	PA, PB	Vdd=5V, I_{OL}=20mA		0.5		V
		Vdd=5V, I_{OL}=5mA		0.1		V
V_{OH}	Output High Voltage					
	PA, PB	Vdd=5V, I_{OH}=		3.8		V
		-20mA		4.5		V
		Vdd=5V, I_{OH}= -5mA				
I_{slp}	Sleep current (WDT disable)	V_{dd}＝2.3 ~ 6.0 V		0.1	1.0	μA
I_{slp}	Sleep current (WDT enable)	V_{dd}＝2.3 V		1		μA
		V_{dd}＝3.0 V		3		μA
		V_{dd}＝4.0 V		6		μA
		V_{dd}＝5.0 V		11		μA
		V_{dd}＝6.0 V		17		μA
V_{pr}	Power Edge-detector Reset Voltage		1.1		1.3	V
Twdt	The basic WDT time-out cycle time	V_{dd}＝2.3 V		25.2		mS
		V_{dd}＝3.0 V		22.4		mS
		V_{dd}＝4.0 V		20.4		mS
		V_{dd}＝5.0 V		18.8		mS
		V_{dd}＝6.0 V		18.0		mS
T_{FLT}	/MCLR filter	V_{dd}＝5.0 V		600		nS
Icc	Comparator Supply current (one comparator)	Vdd=5.0v		15		μA
Vref	Input reference voltage	Vdd=2.5v ~6.0 V			Vdd-0.8v	V

Sym	Description	Condition	Min	Typ	Max	Unit
	Comparator Response time	Vdd=5.0v , V- = Vref				
	V-=Vdd/4, V+=V- ± 0.2v	V+ = (PA0~PA3)		8		μS
---	V-=Vdd/2, V+=V- ± 0.2v			8		μS
	V-=Vdd3/4, V+=V- ± 0.2v			8		μS
	V-=VDD-0.8,V+=V± 0.2v			8		μS

11. Operating Current

Temperature＝25 ℃, the typical value as followings :

11.1 OSC Type＝RC ； WDT－Enable; @V_{dd}＝5.0 V； PED=Disable

Cext. (F)	Rext. (Ohm)	Frequency (Hz)	Current (A)
3P	4.7 K	11.2 M	1.2 mA
	10.0 K	5.94 M	650 μA
	47.0 K	1.40M	235 μA
	100.0 K	660 K	165 μA
	300.0 K	225 K	140 μA
	470.0 K	140 K	120 μA
20P	4.7 K	5.43 M	620 μA
	10.0 K	2.74 M	368 μA
	47.0 K	622 K	170 μA
	100.0 K	295 K	140 μA
	300.0 K	100 K	125 μA
	470.0 K	64 K	120 μA
100P	4.7 K	1.76 M	292 μA
	10.0 K	886 K	205μA
	47.0 K	193 K	145 μA
	100.0 K	92 K	130 μA
	300.0 K	31 K	130 μA
	470.0 K	20 K	125 μA

Cext. (F)	Rext. (Ohm)	Frequency (Hz)	Current (A)
300P	4.7 K	685 K	192 μA
	10.0 K	335 K	156 μA
	47.0 K	75 K	133 μA
	100.0 K	35 K	130 μA
	300.0 K	12 K	126 μA
	470.0 K	7 K	125 μA

11.2 OSC Type＝LF (OSC1&OSC2 External Cap about 10P); WDT－Disable ; PED=Disable

Voltage/Frequency	32 K (Ext100p)	455 K (Ext50P)	1 M	Sleep
2.3 V	7.0μA	2.6V@25.0 μA	40μA	＜1.0 μA
3.0 V	15.0μA	50μA	68μA	＜1.0 μA
4.0 V	35.0μA	88μA	120μA	＜1.0 μA
5.0 V	72.0μA	142μA	180μA	＜1.0 μA
6.0 V	130.0μA	220μA	260μA	＜1.0 μA

11.3 OSC Type＝XT (OSC1&OSC2 External Cap about 10P); WDT－Enable ;PED=Disable

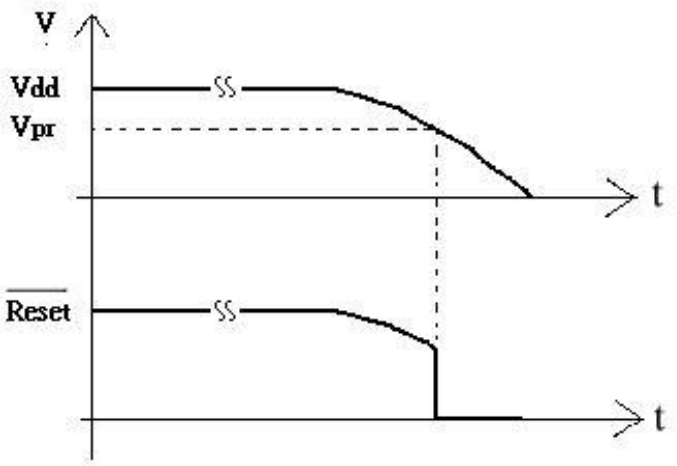
Voltage/Frequency	1 M	4 M	10 M	Sleep
2.1 V	50μA	120μA	290μA	＜1.0 μA
3.0 V	102μA	235μA	500μA	3 μA
4.0 V	215μA	405μA	650μA	6 μA
5.0 V	378μA	600μA	1.3mA	11 μA
6.0 V	650μA	855μA	1.6mA	17 μA

11.4 OSC Type＝HF (OSC1&OSC2 External Cap about 10P); WDT－Enable ; PED=Disable

Voltage/Frequency	4 M	10 M	20 M	Sleep
2.1 V	150μA	320μA	X	＜1.0 μA
3.0 V	288μA	555μA	925μA	3 μA
4.0 V	510μA	910μA	1.5mA	6 μA
5.0 V	800μA	1.5mA	2.3mA	11 μA
6.0 V	1.3mA	1.9mA	3.2mA	17 μA

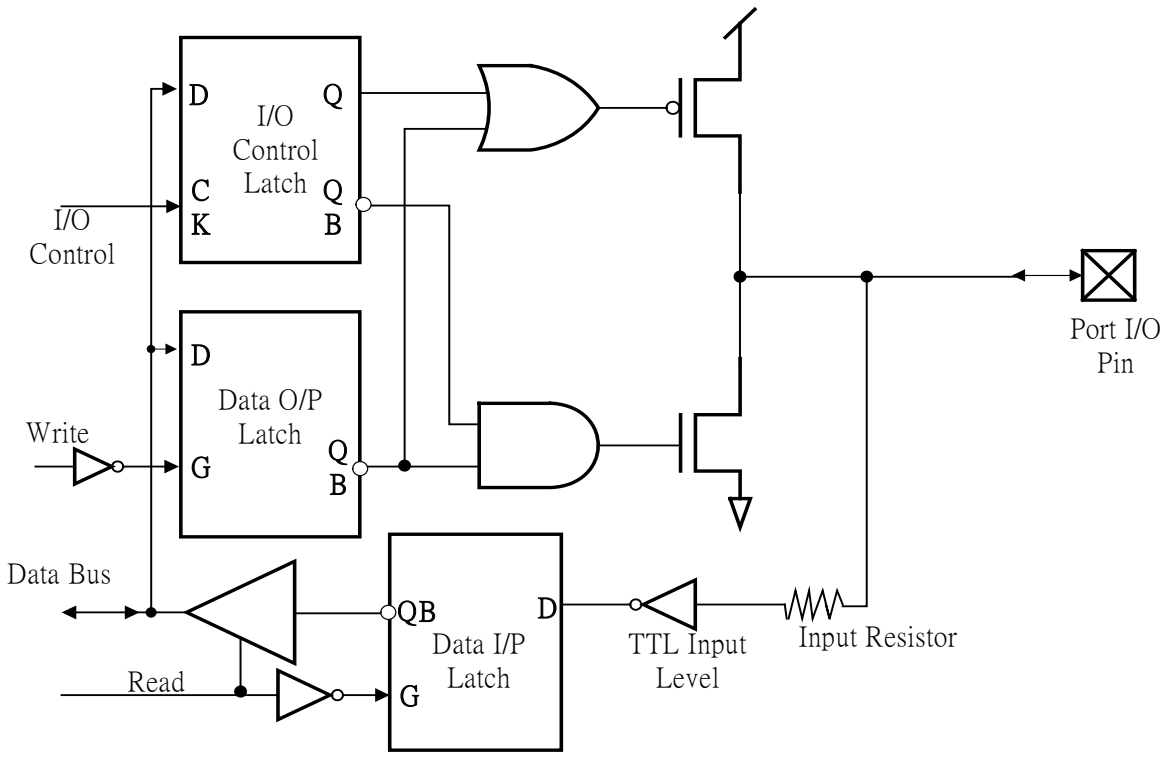
11.5 Power Edge-detector Reset Voltage (Not in Sleep Mode), @ V_{dd}＝5.0 V (PED:Enable)

V_{pr}≦1.6~1.8 V　　V_{pr} ： V_{dd} (Power Supply)

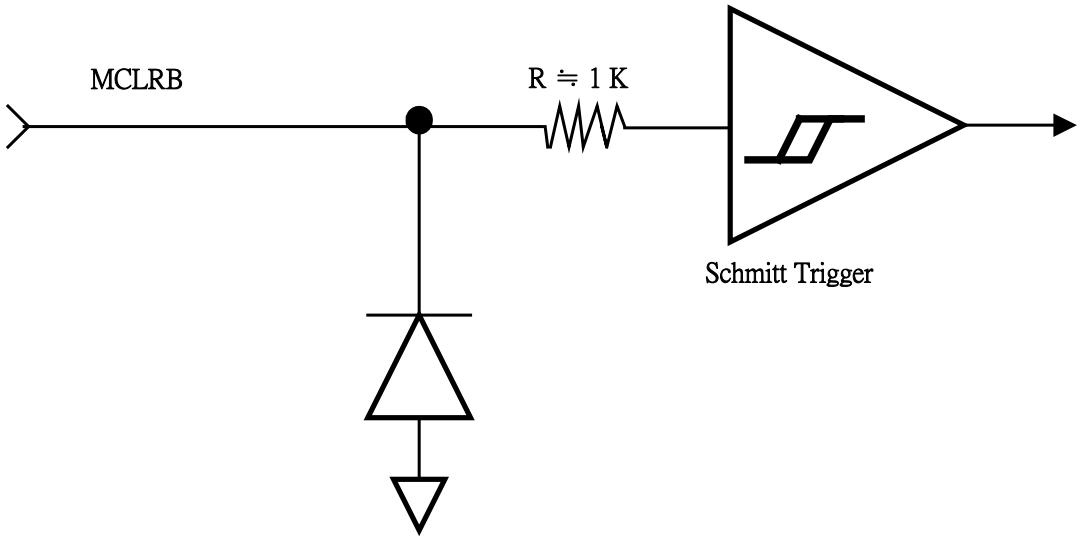


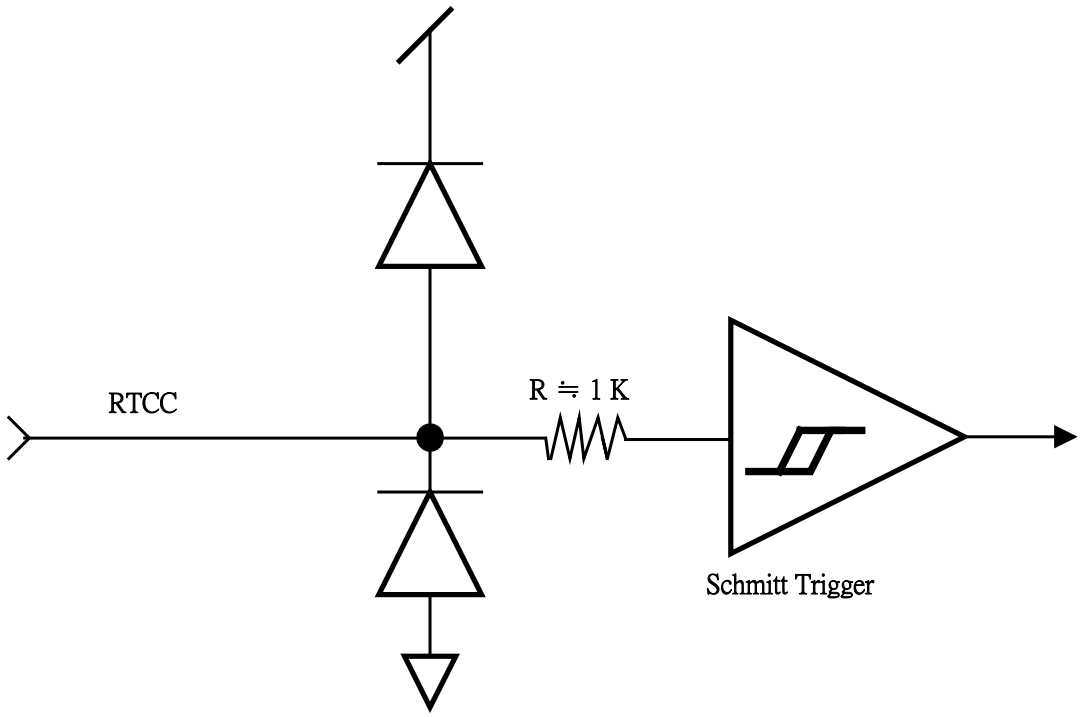
PS. If PED_Enable then Internal Power_on_reset will be off

12. Port A and Port B Equivalent Circuit



13. MCLRB and RTCC Input Equivalent Circuit

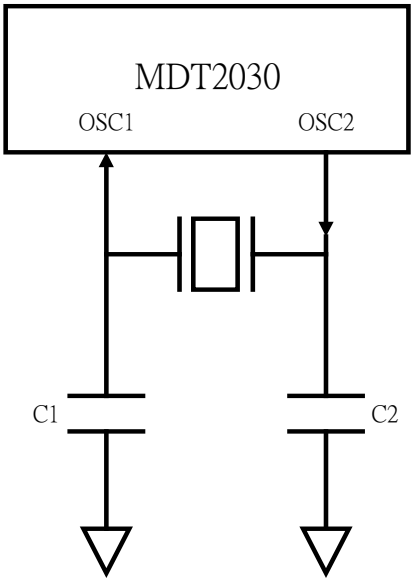




14. External Capacitor Selection For Crystal Oscillator

@ V_{dd}=5.0 V

Osc. Type	Resonator Freq.	Capacity Range
HF	20 MHz	10 pF ~ 50 pF
	10 MHz	20 pF ~ 50 pF
	4 MHz	10 pF ~ 30 pF
XT	10 MHz	10 pF ~ 50 pF
	4 MHz	10 pF ~ 50 pF
	1 MHz	20 pF ~50 pF
LF	1 MHz	20 pF ~ 30 pF
	455 K	20 pF ~30 pF
	32 K	20 pF ~30 pF



To increase the stability of oscillator and the ability of anti-noise, the above values of the external capacitor are for reference only, but the higher capacitance also increases the start-up time.