FEATURES

- **Cost-effective, High-performance 32-bit DSP**
  - 300,000,000 MAC/S (multiply accumulates per second)
  - Dual MAC cycles per clock
  - 72-bit accumulators are the most accurate in the industry
  - 32K x 32-bit SRAM with three 2K blocks assignable to either Y data or program memory.
- **Integrated DAC & ADC Functionality**
  - 8 Channels of DAC output: 108dB DR, 98dB THD+N
  - 4 Channels of ADC input: 105dB DR, 98dB THD+N
  - Integrated 5:1 analog mux feeds one stereo ADC
- **Configurable Serial Audio Inputs/Outputs**
  - Integrated 192 kHz S/PDIF Rx
  - Integrated 192 kHz S/PDIF Tx
  - Supports 32-bit Serial Data @ 192 kHz
  - Supports 32-bit audio sample I/O between DSP chips
  - TDM I/O modes (Up to 8 channels per line)
- **Supports Different Fs Sample Rates**
  - Three Integrated hardware SRC blocks
  - Output can be master or slave
  - Supports dual-domain Fs on inputs (S/PDIF Rx and I^2S)
  - Supports dual-domain Fs on outputs (S/PDIF Tx and I^2S)
- **DSP Tool Set w/ Private Keys Protect Customer IP**
- **Integrated Clock Manager/PLL**
  - Flexibility to operate from internal PLL, external crystal, external oscillator
- **Input Fs Auto Detection w/ µC Acknowledgement**
- **Host & Boot via SPI / I^2C Serial Interface**
- **Configurable GPIOs and External Interrupt Input**
- **1.8V Core and a 3.3V I/O that is tolerant to 5V input**
- **Low-power Mode: 620µW**

The CS47048 family is a new generation of audio system-on-a-chip (ASOC) processors targeted at high fidelity, cost sensitive designs. Derived from the highly successful CS48500 32-bit fixed point audio enhancement processor family, the CS47048 further simplifies system design and reduces total system cost by integrating the S/PDIF Rx, S/PDIF Tx, analog inputs, analog outputs, and SRCs to simplify system design. For example, a hardware SRC can down-sample a 192kHz S/PDIF stream to a lower Fs to reduce memory and MIPS requirements for processing. This integration effectively reduces the chip count from 3 to 1 which allows smaller, less expensive board designs.

Target applications are:

- Automotive Head Units & Outboard Amplifiers
- Automotive Processors & Automotive Integration Hubs
- Digital TV
- MP3 Docking Stations
- AVR and DVD RX
- DSP Controlled Speakers (e.g. Subwoofers, Sound Bars)

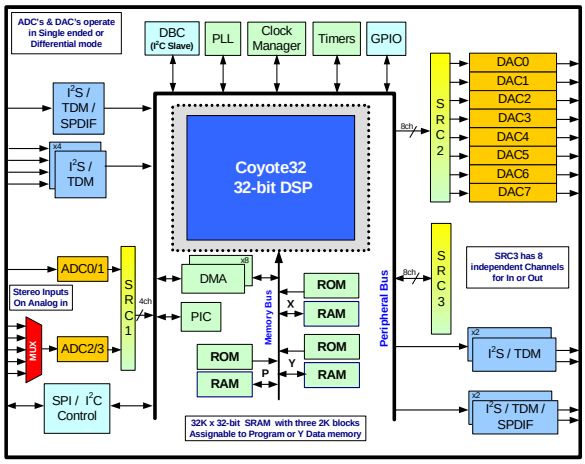
The CS47048 is programmed using the simple yet powerful Cirrus proprietary DSP Composer™ GUI development and pre-production tuning tool. Processing chains may be designed using a drag-and-drop interface to place/utilize functional macro audio DSP primitives and custom audio filtering blocks. The end result is a software image that is downloaded to the DSP via serial control port.

DSP programming could not be easier for the novice or small engineering development group. DSP Composer provides the programmer with faster time-to-market opportunities and the ability to implement custom code.

The CS47048 is available in a 100-pin LQFP package with exposed pad for better thermal characteristics. Both Commercial (0°C to +70°C) and Automotive (-40°C to +85°C) temperature grades.

Ordering Information:

See page 30 for ordering information



Advance Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to www.cirrus.com.

Table of Contents

Figures

Tables

1. Documentation Strategy

The *CS47048 Data Sheet* describes the CS47048 audio processors. This document should be used in conjunction with the following documents when evaluating or designing a system around the CS47048 processors

Table 1. CS47048 Related Documentation

Document Name	Description
CS47048 Data Sheet	This document
CS47048 System Designer's Guide	Includes detailed system design information including Typical Connection Diagrams, Boot-Procedures, Pin Descriptions, Etc.
AN333 - CS47048 Firmware User's Manual	Includes detailed firmware design information including signal processing flow diagrams and control API information
DSP Composer User's Manual	Includes detailed configuration and usage information for the GUI development tool.

The scope of the *CS47048 Data Sheet* is primarily the hardware specifications of the CS47048 family of devices. This includes hardware functionality, characteristic data, pinout, and packaging information.

The intended audience for the *CS47048 Data Sheet* is the system PCB designer, MCU programmer, and the quality control engineer.

2. Overview

The CS47048 DSP is designed to provide high-performance post-processing and mixing of analog and digital audio. The dual clock domain provided on the PCM inputs allows for the mixing of audio streams with different sampling frequencies. The low-power standby preserves battery life for applications which are always on, but not necessarily processing audio, such as automotive audio systems.

The CS47048 utilizes voltage-out DACs and is capable of supporting dual input clock domains and dual output clock domains through the use of the internal SRCs. The CS47048 is available in a 100-pin LQFP package. Refer to Table 2 on page 7 for the input, output, and firmware configurations for the CS47048 DSP.

2.1 Licensing

Licenses are required for any 3rd party audio processing algorithms provided for the CS47048. Please contact your local Cirrus Logic Sales representative for more information.

3. Code Overlays

The suite of software available for the CS47048 family consists of an operating system (OS) and a library of overlays. The overlays for the CS47048 are currently limited to post-processors. All software components are defined below:

1. *OS/Kernel* - Encompasses all non-audio processing tasks, including loading data from external serial memory, processing host messages, calling audio-processing subroutines, error concealment, etc.
2. *Post-processors* - Any module that processes audio I/O buffer PCM data. Examples are bass management, audio manager, tone control, EQ, delay, customer-specific effects, and any post-processing algorithms available for the CS485xx.

The bulk of standard overlays are stored in ROM within the CS47048, but a small image is required to configure the overlays and boot the DSP. This small image can either be stored in an external serial FLASH/EEPROM, or downloaded via a host controller through the SPI™/I²C® serial port.

The overlay structure reduces the time required to reconfigure the DSP when a processing change is requested. Each overlay can be reloaded independently without disturbing the other overlays. For example, when a different post-processor is selected, the OS, does not need to be reloaded — only the new post-processor.

Table 2 lists the different configuration options available. Please refer to the *CS47048 Firmware User's Manual* for the latest listing of application codes and Cirrus Framework™ modules available.

Table 2. Device Selection Guide

Device	Suggested Application	Channel Count Input/Output	Package
CS47048-CQZ CS47048-DQZ	Automotive Head Units Automotive Outboard Amplifiers Automotive Processors Automotive Integration Hubs Digital TV MP3 Docking Stations AVR DVD Rx DSP Controlled Speakers	Up to 12 Channels Analog In (4 simultaneously) Up to 10 Channels PCM In (Stand-Alone) Up to 8 Channels PCM In (w/ Host) Up to 40 Channels TDM In Up to 8 Channels Analog Out Up to 8 Channels PCM Out Up to 32 Channels TDM Out	100-pin QFP

4. Hardware Functional Description

The CS47048 is a true system-on-a-chip that combines a powerful 32-bit DSP engine with analog/digital audio inputs and analog/digital audio outputs. It can be integrated into a complex multi-DSP processing system, or stand alone in an audio product that requires analog-in and analog-out. A top level block diagram is shown below in Figure 1.

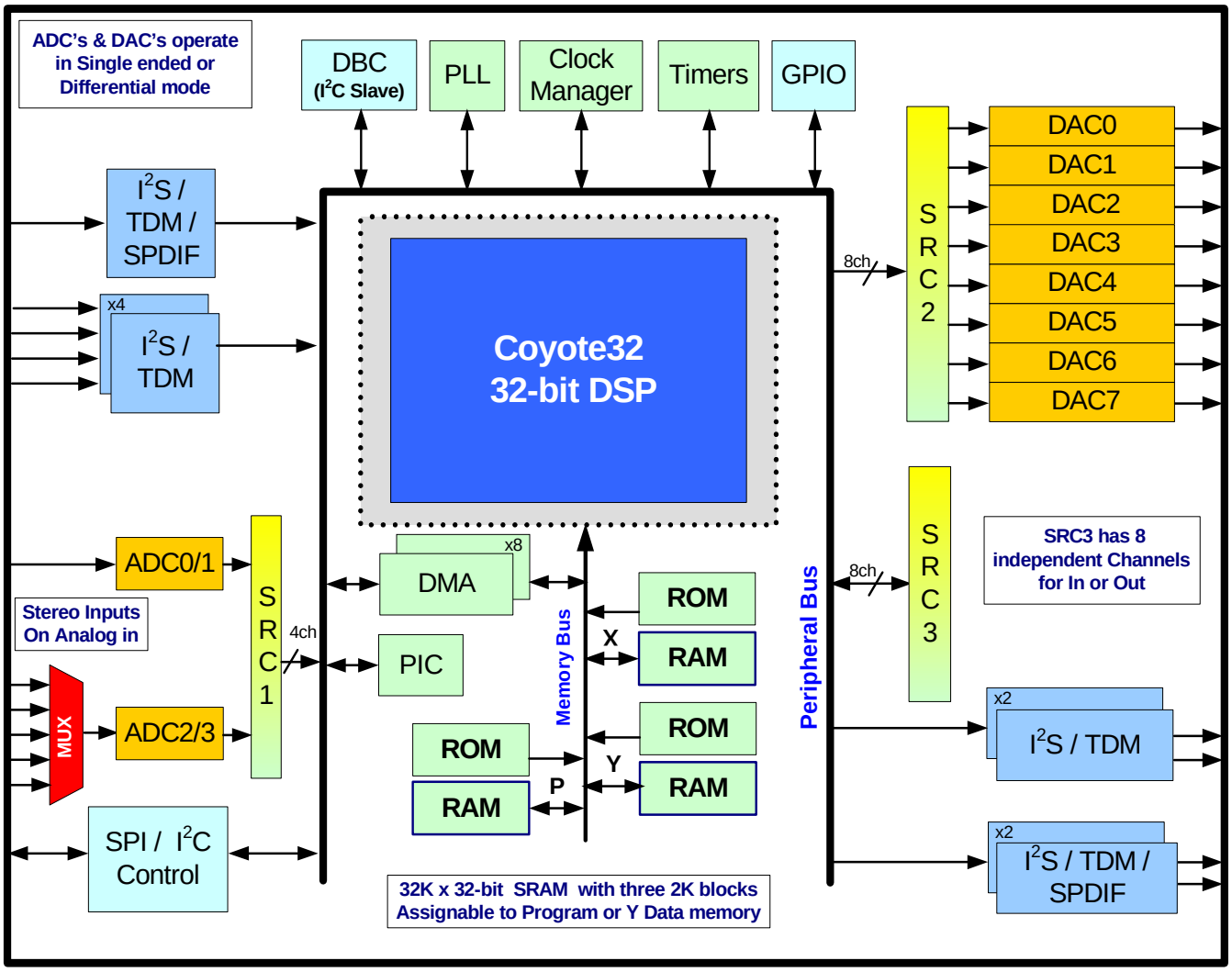


Figure 1. CS47048 Top-Level Block Diagram

4.1 DSP Core

The CS47048 is a single-core DSP with separate X and Y data and P code memory spaces. The DSP core is a high-performance, 32-bit, user-programmable, fixed-point DSP that is capable of performing two multiply-and-accumulate (MAC) operations per clock cycle. The DSP core has eight 72-bit accumulators, four X-data and four Y-data registers, and 12 index registers.

The DSP core is coupled to a flexible 8-channel DMA engine. The DMA engine can move data between peripherals such as the serial control port (SCP), digital audio input (DAI) and digital audio output (DAO), sample rate converters (SRC), analog-to-digital converters (ADC), digital-to-analog converters (DAC), or any DSP core memory, all without the intervention of the DSP. The DMA engine off-loads data move instructions from the DSP core, leaving more MIPS available for signal processing instructions.

CS47048 functionality is controlled by application codes that are stored in on-chip ROM or downloaded to the CS47048 from a host controller or external serial FLASH/EEPROM.

Users can develop their applications using DSP Composer™ to create the processing chain and then compile the image into a series of commands that are sent to the CS47048 through the SCP. The processing application can either load modules (post-processors) from the DSP's on-chip ROM, or custom firmware can be downloaded through the SCP.

The CS47048 is suitable for a variety of audio post-processing applications where sound quality via sound enhancement and speaker/cabinet tuning is required to achieve the sound quality consumers expect. Examples of such applications include automotive head-ends, automotive amplifiers, docking stations, sound bars, subwoofers, and boom boxes.

4.2 DSP Memory

The DSP core has its own on-chip data and program RAM and ROM and does not require external memory for post-processing applications.

The Y-RAM and P-RAM share a single block of memory that includes three 2K word blocks (32 bits/word) that are assignable to either Y-RAM or P-RAM as shown in Table 3.

Table 3. Memory Configurations for CS47048

P-RAM	X-RAM	Y-RAM
14K words	10K words	8K words
12K words	10K words	10K words
10K words	10K words	12K words
8K words	10K words	14K words

4.2.1 DMA Controller

The powerful 8-channel DMA controller can move data between 8 on-chip resources. Each resource has its own arbiter: X, Y, and P RAMs/ROMs and the peripheral bus. Modulo and linear addressing modes are supported, with flexible start address and increment controls. The service intervals for each DMA channel, as well as up to 6 interrupt events, are programmable.

4.3 On-chip DSP Peripherals

4.3.1 Analog to Digital Converter Port (ADC)

The CS47048 features ADCs with dynamic range performance in excess of 100 dB, and they can support up to 4 simultaneous channels of analog-to-digital conversion. Analog inputs AIN_1A and AIN_1B are connected directly to one stereo ADC (ADC0-1). The analog input capability of the second stereo ADC (ADC2-3) is expanded through a 5:1 analog stereo mux (analog inputs AIN_2A/B through AIN_6A/B). This gives the CS47048 the ability to select from six stereo pairs of analog input. A single programmable bit selects single-ended or differential mode signals for all inputs.

The conversions are performed with either Fs=96 kHz or Fs=192 kHz.

4.3.2 Digital to Analog Converter Port (DAC)

The CS47048 can support up to 8 simultaneous channels of digital-to-analog conversion and features DACs with dynamic range performance in excess of 100 dB. The DACs have voltage mode outputs that can be connected either as single-ended or differential signals. The conversions are performed with Fs=96 kHz.

4.3.3 Digital Audio Input Port (DAI)

The input capabilities for each version of the CS47048 are summarized in Table 2 on page 7.

Up to five DAI ports are available. Two of the DAI ports can be programmed to implement other functions. The S/PDIF Rx function, if used, takes over the DAI_DATA3 pin. If the SPI mode is used, the DAI_DATA4 pin becomes the SCP_CS input.

The DAI port supports PCM format with word lengths up to 32 bits and sample rates as high as 192 kHz.

The DAI also supports a time division multiplexed (TDM) one-line data mode that packs PCM audio on a single data line. The total number possible depends on the ratio of SCLK to LRCLK. The CS47048 hardware supports up to 40 channels in one line mode @ 48 kHz. There is also a practical limitation set by the amount of processing required per channel.

The DAI port has two independent slave-only clock domains. The PCM inputs can be on one clock domain, and the S/PDIF Rx on another. The output of the S/PDIF Rx can then be converted through one of the internal SRC blocks to synchronize with the PCM input.

The sample rate of the input clock domains can be determined automatically by the DSP, off-loading the task of monitoring the S/PDIF Rx from the host. A time-stamping feature provides the ability to also sample-rate convert the input data via software.

4.3.4 S/PDIF RX Input Port (DAI)

One of the PCM pins of the DAI can also be used as a DC-coupled, TTL-level S/PDIF Rx input capable of receiving and demodulating bi-phase encoded S/PDIF signals with Fs ≤ 192 kHz.

4.3.5 Digital Audio Output Port (DAO)

The output capabilities of the CS47048 are summarized in Table 2 on page 7.

DAO port supports PCM resolutions of up to 32-bits. The port supports sample rates (Fs) as high as 192 kHz. The port can be configured as an independent clock domain mastered by the DSP, or as a clock slave if an external MCLK or SCLK/LRCLK source is available.

The DAO also supports a time division multiplexed (TDM) one-line data mode, that packs multiple channels of PCM audio on a single data line. The total number possible depends on the ratio of SCLK to LRCLK and the version of chip. For example, the CS47048 hardware supports up to 32 channels in one line mode @ 48 kHz. There is also a practical limitation set by the amount of processing required per channel.

4.3.6 S/PDIF TX Output Port (DAO)

Two of the serial audio pins can be re-configured as S/PDIF TX pins that drive a bi-phase encoded S/PDIF signal (data with embedded clock on a single line). The S/PDIF engine can be driven by a clock domain independent of the PCM output port by utilizing one of the internal SRCs.

4.3.7 Sample Rate Converters (SRC)

The CS47048 has 3 internal SRC modules. Two of the SRC modules are capable of converting 8 Channels, and one SRC has 4-Channel capability.

The ADCs are directly associated with a 4-Channel SRC which is used to transfer data from the fixed 96/192 kHz Fs domain into an Fs appropriate for mixing with other audio in the system. When the Analog Inputs are not being used, this SRC can be used to convert digital data within the DSP from the input Fs (Fsi) to the output Fs (Fso).

The DACs are directly associated with an 8-Channel SRC which is used to transfer data from the Fs being processed by the DSP to a fixed 96 kHz Fs domain for conversion to analog. When the Analog Outputs are not being used, this SRC can be used to convert digital data within the DSP from Fsi to Fso.

The second 8-Channel SRC is a stand-alone digital-to-digital conversion module. It can be used to make independent input clock domains synchronous (different Fs on PCM input and S/PDIF Rx) or to drive the S/PDIF Tx at a different Fs than the PCM output of the DSP.

4.3.8 Serial Control Port ($I^2C^{®}$ or SPI™)

The on-chip serial control port is capable of operating as master or slave in either SPI™ or $I^2C^{®}$ modes. Master/Slave operation is chosen by mode select pins when the CS47048 comes out of reset. The serial clock pin can support frequencies as high as 25 MHz in SPI mode (SPI clock speed must always be ≤ (DSP Core Frequency/2)). The CS47048 serial control port also includes a pin for flow control of the communications interface ($\overline{\text{SCP\_BSY}}$) and a pin to indicate when the DSP has a message for the host ($\overline{\text{SCP\_IRQ}}$).

4.3.9 GPIO

Many of the CS47048 peripheral pins are multiplexed with GPIO. Each GPIO can be configured as an output, an input, or an input with interrupt. Each input-pin interrupt can be configured as rising edge, falling edge, active-low, or active-high.

4.3.10 PLL-based Clock Generator

The low-jitter PLL generates integer or fractional multiples of a reference frequency which are used to clock the DSP core and peripherals. Through a second PLL divider chain, a dependent clock domain can be output on the DAO port for driving audio converters. The CS47048 defaults to running from the external reference frequency and is switched to use the PLL output after overlays have been loaded and configured, either through master boot from an external FLASH or through host control. A built-in crystal oscillator circuit with a buffered output is provided. The buffered output frequency ratio is selectable between 1:1 (default) or 2:1.

4.3.11 Hardware Watchdog Timer

The CS47048 has an integrated watchdog timer that acts as a “health” monitor for the DSP. The watchdog timer must be reset by the DSP before the counter expires, or the entire chip is reset. This peripheral ensures that the CS47048 will reset itself in the event of a temporary system failure. In stand-alone mode (i.e. no host MCU), the DSP will reboot from external FLASH. In slave mode (i.e. host MCU present) a GPIO will be used to signal the host that the watchdog has expired and the DSP should be rebooted and re-configured.

4.4 DSP I/O Description

4.4.1 Multiplexed Pins

Many of the CS47048 pins are multi-functional. For details on pin functionality please refer to the *CS47048 System Designer’s Guide*.

4.4.2 Termination Requirements

Open-drain pins on the CS47048 must be pulled high for proper operation. Please refer to the *CS47048 System Designer’s Guide* to identify which pins are open-drain and what value of pull-up resistor is required for proper operation.

Mode select pins on the CS47048 are used to select the boot mode upon the rising edge from reset. A detailed explanation of termination requirements for each communication mode select pin can be found in the *CS47048 System Designer’s Guide*.

4.4.3 Pads

The CS47048 Digital I/Os operate from the 3.3 V supply and are 5 V tolerant.

4.5 Application Code Security

The external program code may be encrypted by the programmer to protect any intellectual property it may contain. A secret, customer-specific key is used to encrypt the program code that is to be stored external to the device. Please contact your local Cirrus representative for details.

5. Characteristics and Specifications

Note: All data sheet minimum and maximum timing parameters are guaranteed over the rated voltage and temperature. All data sheet typical parameters are measured under the following conditions: T = 25 °C, VDD = 1.8 V, VDDIO = VDDA =3.3 V, GND = GNDIO = GNDA = 0 V.

5.1 Absolute Maximum Ratings

(GND = GNDIO = GNDA = 0 V; all voltages with respect to 0 V)

Parameter	Symbol	Min	Max	Unit
DC power supplies: Core supply	VDD	–0.3	2.0	V
Analog supply	VDDA	–0.3	3.6	V
I/O supply	VDDIO	–0.3	3.6	V
|VDDA – VDDIO|		-	0.3	V
Input pin current, any pin except supplies	I_{in}	-	+/- 10	mA
Input voltage on PLL_REF_RES	V_{filt}	-0.3	3.6	V
Input voltage on digital I/O pins	V_{inio}	-0.3	5.0	V
Analog Input Voltage	V_{in}	AGND - 0.7	VA + 0.7	V
Storage temperature	T_{stg}	–65	150	°C

Caution: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

5.2 Recommended Operating Conditions

(GND = GNDIO = GNDA = 0 V; all voltages with respect to 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
DC power supplies: Core supply	VDD	1.71	1.8	1.89	V
Analog supply	VDDA	3.13	3.3	3.46	V
I/O supply	VDDIO	3.13	3.3	3.46	V
|VDDA – VDDIO|			0		V
Ambient operating temperature	T_A		-		°C
Commercial - CQZ		0		+ 70	
Automotive - DQZ		- 40		+ 85	

Note: It is recommended that the 3.3 V IO supply come up ahead of or simultaneously with the 1.8 V core supply.

5.3 Digital DC Characteristics

(Measurements performed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	2.0	-	-	V
Low-level input voltage, except XTI	V_{IL}	-	-	0.8	V
Low-level input voltage, XTI	V_{ILXTI}	-	-	0.6	V
Input Hysteresis	V_{hys}		0.4		V
High-level output voltage (I_O = -2mA), except XTO	V_{OH}	VDDIO * 0.9	-	-	V
Low-level output voltage (I_O = 2mA), except XTO	V_{OL}	-	-	VDDIO * 0.1	V
Input leakage XTI	I_{LXTI}	-	-	5	µA
Input leakage current (all digital pins with internal pull-up resistors enabled)	I_{LEAK}	-	-	70	µA

5.4 Power Supply Characteristics

Note: Measurements performed under operating conditions)

Parameter	Min	Typ	Max	Unit
Operational Power Supply Current:				
VDD: Core and I/O operating[1]	-	325	-	mA
VDDA: PLL operating current	-	16	-	mA
VDDA: DAC operating current (all 8 channels enabled)	-	56	-	mA
VDDA: ADC operating current (all 4 channels enabled)	-	34	-	mA
VDDIO: With most ports operating	-	27	-	mA
Total Operational Power Dissipation:		1025		mW
Standby Power Supply Current:				
VDD: Core and I/O not clocked	-	140	-	µA
VDDA: PLLs halted	-	1.2	-	µA
VDDA: DAC disabled	-	100	-	µA
VDDA: ADC disabled	-	10	-	µA
VDDIO: All connected I/O pins 3-stated by other ICs in system	-	0.4	-	µA
Total Standby Power Dissipation:		620		µW

1. Dependent on application firmware and DSP clock speed.

5.5 Thermal Data (100-Pin LQFP with Exposed Pad)

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance (Junction to Ambient)	θ_{ja}				°C / Watt
Two-layer Board[1]		-	34	-	
Four-layer Board[2]		-	18	-	
Thermal Resistance (Junction to Top of Package)	Ψ_{jt}				°C / Watt
Two-layer Board[1]		-	0.54	-	
Four-layer Board[2]		-	.28	-	

1. To calculate the die temperature for a given power dissipation:

$$T_j = \text{Ambient temperature} + [\ (\text{Power Dissipation in Watts}) * \theta_{ja}\ ]$$

2. To calculate the case temperature for a given power dissipation:

$$T_c = T_j - [\ (\text{Power Dissipation in Watts}) * \psi_{jt}\ ]$$

Note: Two-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz. copper covering 20% of the top & bottom layers.

Note: Four-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz. copper covering 20% of the top & bottom layers and 0.5-oz. copper covering 90% of the internal power plane & ground plane layers.

5.6 Digital Switching Characteristics— RESET

Parameter	Symbol	Min	Max	Unit
$\overline{\text{RESET}}$ minimum pulse width low	T_{rstl}	1	-	µs
All bidirectional pins high-Z after $\overline{\text{RESET}}$ low	T_{rst2z}	-	100	ns
Configuration pins setup before $\overline{\text{RESET}}$ high	T_{rstsu}	50	-	ns
Configuration pins hold after $\overline{\text{RESET}}$ high	T_{rsthld}	20	-	ns

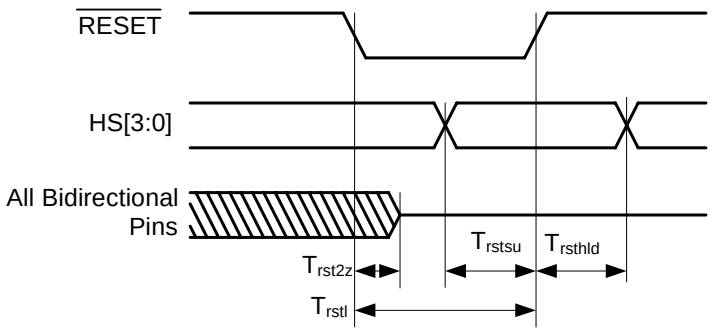


Figure 2. RESET Timing

5.7 Digital Switching Characteristics — XTI

Parameter	Symbol	Min	Max	Unit
External Crystal operating frequency[1]	F_{xtal}	11.2896	27	MHz
XTI period	T_{clki}	37	89	ns
XTI high time	T_{clkih}	13.3	-	ns
XTI low time	T_{clkil}	13.3	-	ns
External Crystal Load Capacitance (parallel resonant)[2]	C_L	10	18	pF
External Crystal Equivalent Series Resistance	ESR		50	Ω

1. Part characterized with the following crystal frequency values: 11.2896, 12.288, 18.432, 24.576, & 27 MH.z
2. C_L refers to the total load capacitance as specified by the crystal manufacturer. Crystals which require a C_L outside this range should be avoided. The crystal oscillator circuit design should follow the crystal manufacturer's recommendation for load capacitor selection.

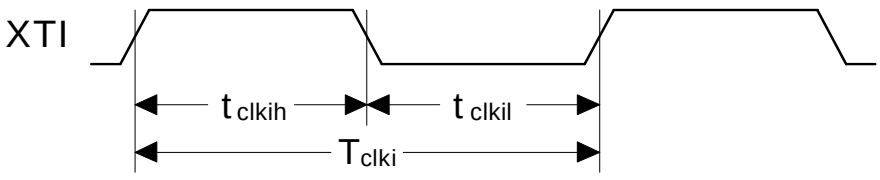


Figure 3. XTI Timing

5.8 Digital Switching Characteristics — Internal Clock

Parameter	Symbol	Min	Max	Unit
Internal DSP_CLK frequency[1]	F_{dclk}	-		MHz
CS47048-CQZ		F_{xtal}[2]	150	
CS47048-DQZ		F_{xtal}	150	
Internal DSP_CLK period[1]	DCLKP	-		ns
CS47048-CQZ		6.7	$1/F_{xtal}$	
CS47048-DQZ		6.7	$1/F_{xtal}$	

1. After initial power-on reset, $F_{dclk} = F_{xtal}$. After initial kickstart commands, the PLL is locked to max F_{dclk} and remains locked until the next power-on reset.

2.See Section 5.7.

5.9 Digital Switching Characteristics — Serial Control Port - SPI Slave Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{spisck}	-		25	MHz
$\overline{\text{SCP\_CS}}$ falling to SCP_CLK rising	t_{spicss}	24		-	ns
SCP_CLK low time	t_{spickl}	20		-	ns
SCP_CLK high time	t_{spickh}	20		-	ns
Setup time SCP_MOSI input	t_{spidsu}	5		-	ns
Hold time SCP_MOSI input	t_{spidh}	5		-	ns
SCP_CLK low to SCP_MISO output valid	t_{spidov}	-		11	ns
SCP_CLK falling to $\overline{\text{SCP\_IRQ}}$ rising	$t_{spiirqh}$	-		20	ns
$\overline{\text{SCP\_CS}}$ rising to $\overline{\text{SCP\_IRQ}}$ falling	$t_{spiirql}$	0			ns
SCP_CLK low to $\overline{\text{SCP\_CS}}$ rising	t_{spicsh}	24		-	ns
$\overline{\text{SCP\_CS}}$ rising to SCP_MISO output high-Z	$t_{spicsdz}$	-	20		ns
SCP_CLK rising to $\overline{\text{SCP\_BSY}}$ falling	$t_{spicbsyl}$	-	3*DCLKP+20		ns

1. f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the $\overline{\text{SCP\_BSY}}$ pin should be implemented to prevent overflow of the input data buffer. At boot the maximum speed is $F_{xtal}/3$.

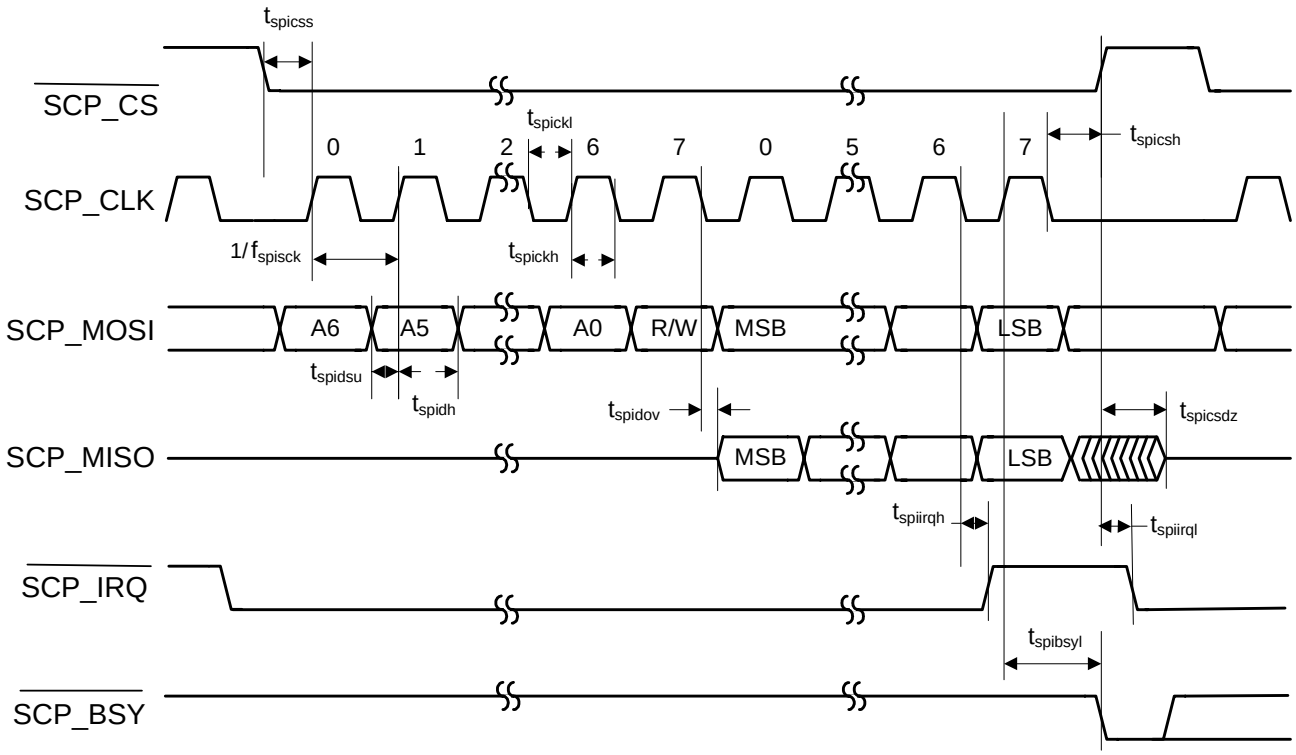


Figure 4. Serial Control Port - SPI Slave Mode Timing

5.10 Digital Switching Characteristics — Serial Control Port - SPI Master Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{spisck}	-		$F_{xtal}/2^2$	MHz
$\overline{SCP\_CS}$ falling to SCP_CLK rising [3]	t_{spicss}	-	11*DCLKP + (SCP_CLK PERIOD)/2	-	ns
SCP_CLK low time	t_{spickl}	18		-	ns
SCP_CLK high time	t_{spickh}	18		-	ns
Setup time SCP_MISO input	t_{spidsu}	9		-	ns
Hold time SCP_MISO input	t_{spidh}	5		-	ns
SCP_CLK low to SCP_MOSI output valid	t_{spidov}	-		8	ns
SCP_CLK low to $\overline{SCP\_CS}$ falling	t_{spicsl}	7		-	ns
SCP_CLK low to $\overline{SCP\_CS}$ rising	t_{spicsh}	-	11*DCLKP + (SCP_CLK PERIOD)/2	-	ns
Bus free time between active $\overline{SCP\_CS}$	t_{spicsx}		3*DCLKP	-	ns
SCP_CLK falling to SCP_MOSI output high-Z	t_{spidz}	-		20	ns

1. f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application.
2. See Section 5.7.
3. SCP_CLK PERIOD refers to the period of SCP_CLK as being used in a given application. It does not refer to a tested parameter

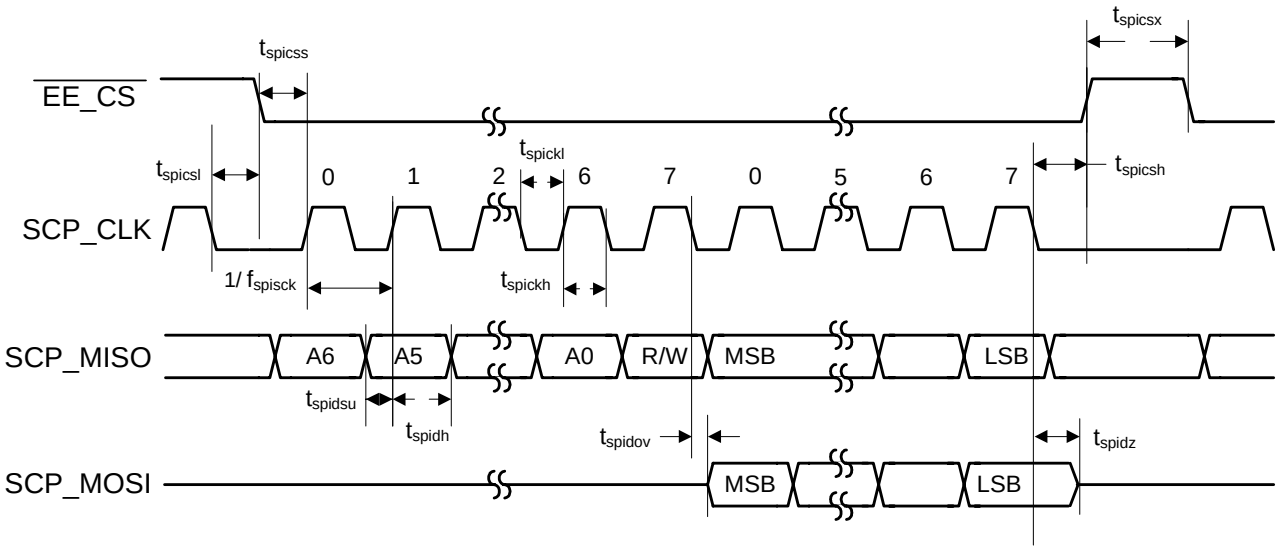


Figure 5. Serial Control Port - SPI Master Mode Timing.

5.11 Digital Switching Characteristics — Serial Control Port - I²C Slave Mode[2]

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{iicck}	-		400	kHz
SCP_CLK rise time	t_{iicr}			150	ns
SCP_CLK fall time	t_{iicf}			150	ns
SCP_CLK low time	t_{iicckl}	1.25		-	µs
SCP_CLK high time	t_{iicckh}	1.25		-	µs
SCP_CLK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25			µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25		-	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5		-	µs
Bus free time between STOP and START conditions	t_{iicbft}	3		-	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	100			ns
Hold time SCP_SDA input after SCP_CLK falling	t_{iich}	20		-	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	-		18	ns
SCP_CLK falling to $\overline{\text{SCP\_IRQ}}$ rising	$t_{iicirqh}$	-		3∗DCLKP + 40	ns
NAK condition to $\overline{\text{SCP\_IRQ}}$ low	$t_{iicirql}$		3∗DCLKP + 20		ns
SCP_CLK rising to $\overline{\text{SCB\_BSY}}$ low	$t_{iicbsyl}$	-	3∗DCLKP + 20		ns

1. f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the $\overline{\text{SCP\_BSY}}$ pin should be implemented to prevent overflow of the input data buffer.

2. I²C Slave Address = 0x82

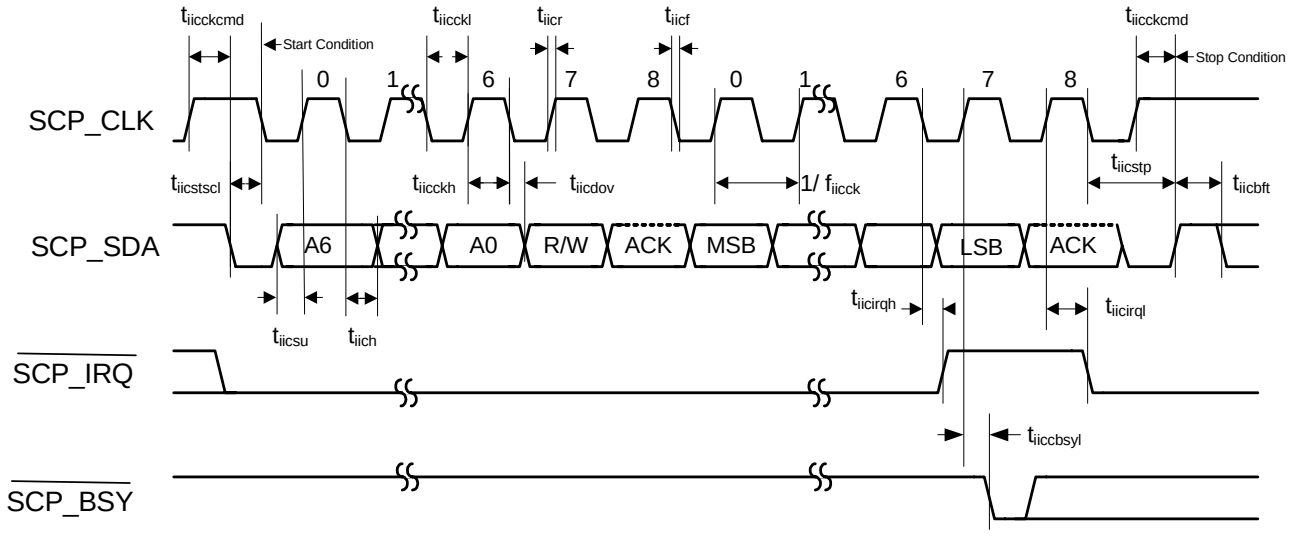


Figure 6. Serial Control Port - I²C Slave Mode Timing

5.12 Digital Switching Characteristics — Serial Control Port - I²C Master Mode

Parameter	Symbol	Min	Max	Units
SCP_CLK frequency[1]	f_{iicck}	-	400	kHz
SCP_CLK rise time	t_{iicr}	-	150	ns
SCP_CLK fall time	t_{iicf}	-	150	ns
SCP_CLK low time	t_{iicckl}	1.25	-	µs
SCP_CLK high time	t_{iicckh}	1.25	-	µs
SCP_CLK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25		µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25	-	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5	-	µs
Bus free time between STOP and START conditions	t_{iicbft}	3	-	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	100		ns
Hold time SCP_SDA input after SCP_CLK falling	t_{iich}	20	-	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	-	18	ns

1. f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application.

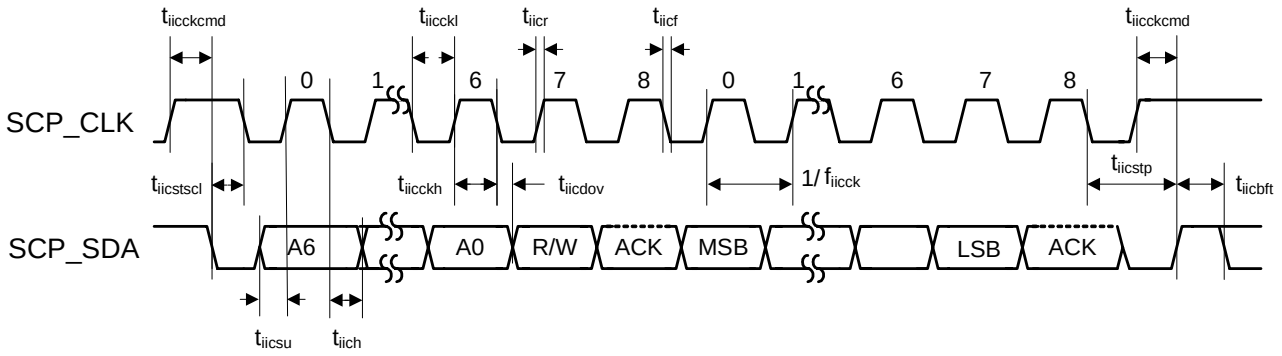


Figure 7. Serial Control Port - I²C Master Mode Timing

5.13 Digital Switching Characteristics — Digital Audio Slave Input Port

Parameter	Symbol	Min	Max	Unit
DAI_SCLK period	$T_{daiclkp}$	20	-	ns
DAI_SCLK duty cycle	-	45	55	%
Setup time DAI_DATAn	t_{daidsu}	8	-	ns
Hold time DAI_DATAn	t_{daidh}	5	-	ns

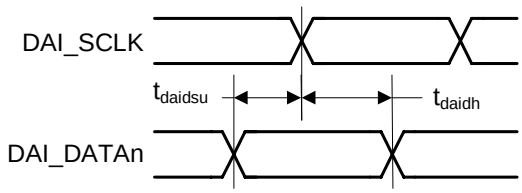
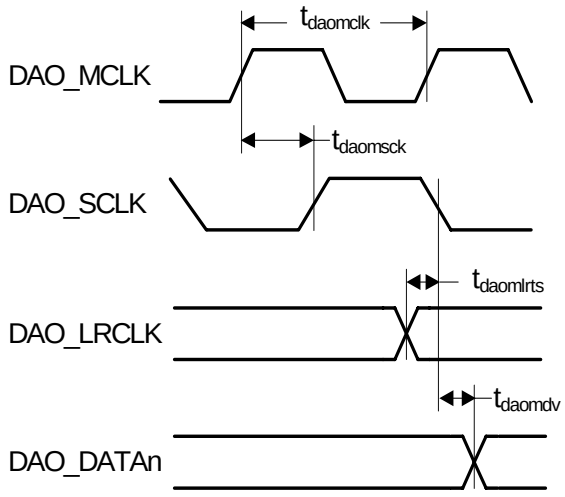


Figure 8. Digital Audio Input (DAI) Port Timing Diagram

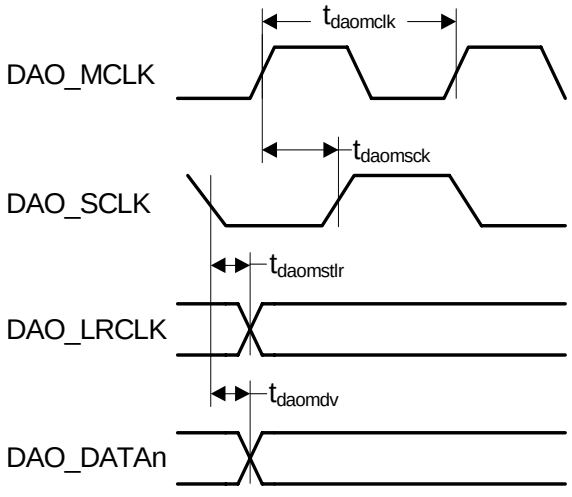
5.14 Digital Switching Characteristics — Digital Audio Output Port

Parameter	Symbol	Min	Max	Unit
DAO_MCLK period	$T_{daomclk}$	20	-	ns
DAO_MCLK duty cycle	-	45	55	%
DAO_SCLK period for Master or Slave mode[1]	$T_{daosclk}$	20	-	ns
DAO_SCLK duty cycle for Master or Slave mode[1]	-	40	60	%
Master Mode (Output A1 Mode)[1,2]				
DAO_SCLK delay from DAO_MCLK rising edge, DAO_MCLK as an input	$t_{daomsck}$	-	19	ns
DAO_LRCLK to DAO_SCLK non-active edge[3], See Figure 9A.	$t_{daomlrts}$	-	8	ns
DAO_SCLK non-active edge[3] to DAO_LRCLK, See Figure 9B	$t_{daomstlr}$	-	8	ns
DAO_DATA[3..0] delay from DAO_SCLK non-active edge[3]	t_{daomdv}	-	8	ns
Slave Mode (Output A0 Mode)[4]				
DAO_LRCLK to DAO_SCLK non-active edge[3], See Figure 10A.	$t_{daoslrts}$	-	15	ns
DAO_SCLK non-active edge[3] to DAO_LRCLK, See Figure 10B.	$t_{daosstlr}$	-	30	ns
DAO1_DATA[3..0] delay from DAO_SCLK non-active edge[3]	t_{daosdv}	-	8	ns

1. Master mode timing specifications are characterized, not production tested.
2. Master mode is defined as the CS47048 driving both DAO_SCLK, DAO_LRCLK. When MCLK is an input, it is divided to produce DAO_SCLK, DAO_LRCLK.
3. The DAO_LRCLK transition may occur on either side of the non-active edge of DAO_LRCLK. The active edge of DAO_SCLK is the point at which the data is valid.
4. Slave mode is defined as DAO_SCLK, DAO_LRCLK driven by an external source.

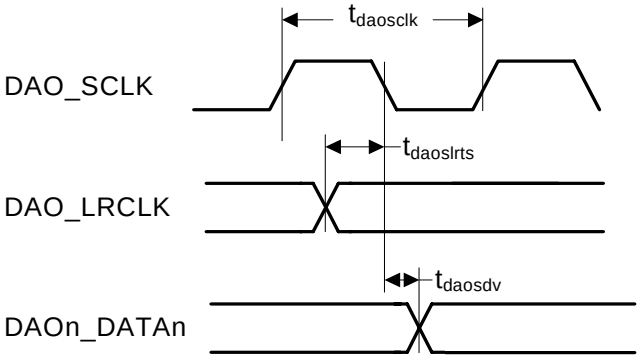


A. DAO_LRCLK transition before DAO_SCLK non-active edge. See Footnote 3 on page 22.

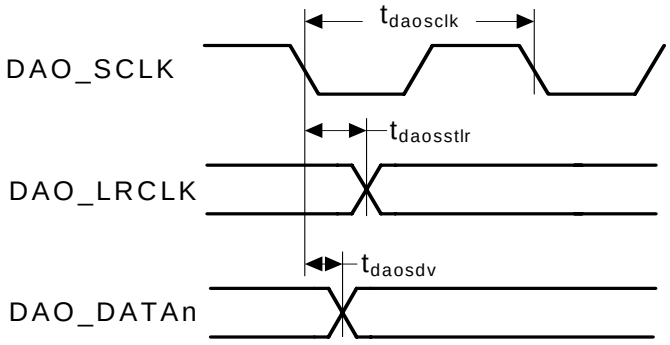


B. DAO_LRCLK transition after DAO_SCLK non-active edge. See Footnote 3 on page 22.

Figure 9. Digital Audio Output Port Timing, Master Mode



A. DAO_LRCLK transition before DAO_SCLK non-active edge. See Footnote 3 on page 22.



B. DAO_LRCLK transition after DAO_SCLK non-active edge. See Footnote 3 on page 22.

Figure 10. Digital Audio Output Port Timing, Slave Mode

5.15 Digital Switching Characteristics — S/PDIF RX Port

(Inputs: Logic 0 = V_{IL}, Logic 1 = V_{IH}; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Units
PLL Clock Recovery Sample Rate Range		30	-	200	kHz

5.16 ADC Characteristics

5.16.1 Analog Input Characteristics (Commercial)

(Test Conditions (unless otherwise specified): T_A = 0 to +70°C; VDD = 1.8 V±5%, VDDA (VA)= 3.3 V±5%; 1 kHz sine wave driven through the passive input filter (R_i=10kΩ) in Figure 11 on page 26 or Figure 12 on page 26; DSP running test application; Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter	Differential Min	Differential Typ	Differential Max	Single-Ended Min	Single-Ended Typ	Single-Ended Max	Unit
Fs= 96 kHz, 192 kHz							
Dynamic Range[1,6,7] A-weighted	99	105	-	96	102	-	dB
unweighted	96	102	-	93	99	-	dB
40 kHz bandwidth unweighted	-	99	-		96	-	dB
Total Harmonic Distortion + Noise[6,7] -1 dB	-	-98	-92	-	-95	-89	dB
-20 dB	-	-82	-	-	-79	-	dB
-60 dB	-	-42	-	-	-39	-	dB
40 kHz bandwidth -1 dB	-	-90	-	-	-90	-	dB
AIN_1A/B Interchannel Isolation	-	95	-	-	95	-	dB
AIN_[2..6]A/B MUX Interchannel Isolation	-	95	-	-	95	-	dB
DC Accuracy							
Interchannel Gain Mismatch	-	0.1	-	-	0.1	-	dB
Gain Drift	-	±120	-	-	±120	-	ppm/°C
Analog Input							
Full-Scale Input Voltage[2,3]	3.3•VA	3.5•VA	3.7•VA	1.65•VA	1.75•VA	1.85•VA	V_{PP}
Differential Input Impedance[4]	-	400	-	-	-	-	Ω
Single-Ended Input Impedance[5]	-	-	-	-	200	-	Ω
Common Mode Rejection Ratio (CMRR)[8]	-	60	-	-	-	-	dB
Parasitic Load Capacitance (C_L)[9]	-	-	20	-	-	20	pF

5.16.2 Analog Input Characteristics (Automotive)

(Test Conditions (unless otherwise specified): T_A = -40 to +85°C; VDD = 1.8 V±5%, VDDA (VA)= 3.3 V±5%; 1 kHz sine wave driven through the passive input filter (R_i=10kΩ) in Figure 11 on page 26 or Figure 12 on page 26; DSP running test application; Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter	Differential Min	Differential Typ	Differential Max	Single-Ended Min	Single-Ended Typ	Single-Ended Max	Unit
Fs=96 kHz, 192 kHz							
Dynamic Range[1,6,7] A-weighted	97	105	-	94	102	-	dB
unweighted	94	102	-	91	99	-	dB
40 kHz bandwidth unweighted	-	99	-		96	-	dB
Total Harmonic Distortion + Noise[6,7] -1 dB	-	-98	-90	-	-95	-87	dB
-20 dB	-	-82	-	-	-79	-	dB
-60 dB	-	-42	-	-	-39	-	dB
40 kHz bandwidth -1 dB	-	-90	-	-	-90	-	dB
AIN_1A/B Interchannel Isolation	-	95	-	-	95	-	dB
AIN_[2..6]A/B MUX Interchannel Isolation	-	95	-	-	95	-	dB
DC Accuracy							
Interchannel Gain Mismatch	-	0.1	-	-	0.1	-	dB
Gain Drift	-	±120	-	-	±120	-	ppm/°C
Analog Input							
Full-Scale Input Voltage[2,3]	3.24•VA	3.5•VA	3.76•VA	1.62•VA	1.75•VA	1.88•VA	V_{PP}
Differential Input Impedance[4]	-	400	-	-	-	-	Ω
Single-Ended Input Impedance[5]	-	-	-	-	200	-	Ω
Common Mode Rejection Ratio (CMRR)[8]	-	60	-	-	-	-	dB
Parasitic Load Capacitance (C_L)[9]	-	-	20	-	-	20	pF

Notes:

1. dB units referred to the typical full-scale voltage.
2. These full-scale values were measured with R_i=10k for both the single-ended and differential mode input circuits.
3. The full-scale voltage can be changed be scaling R_i.
   Differential Full-Scale (Vpp) = (R_i+200)/(10k+200)*3.5*VDDA
   Single-Ended Full-Scale (Vpp) = (R_i+200)/(10k+200)*1.75*VDDA
4. Measured between AIN_xx+ and AN_xx-.
5. Measured between AIN_xx+ and AGND.
6. Decreasing Full-Scale voltage by reducing R_i will cause the noise floor to increase.
7. Common mode input current should be kept to less than +/- 160uA to avoid performance degradation: $|(I_{ip}+I_{in})/2| <$ 160uA. This corresponds to +/- 1.6V for R_i=10kΩ in the differential case.
8. This number was measured using perfectly matched external resistors (R_i). Mismatch in the external resistors will typically reduce CMRR by 20 log ($|\Delta R_i|/R_i$ + 0.001).
9. C_L represents the parasitic load capacitance between R_i on the input circuit and the input pin of the CS47048 package.

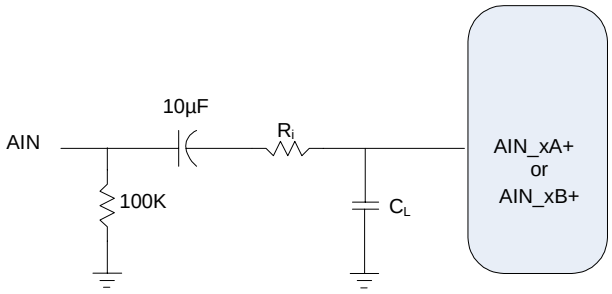


Figure 11. ADC Single-Ended Input Test Circuit

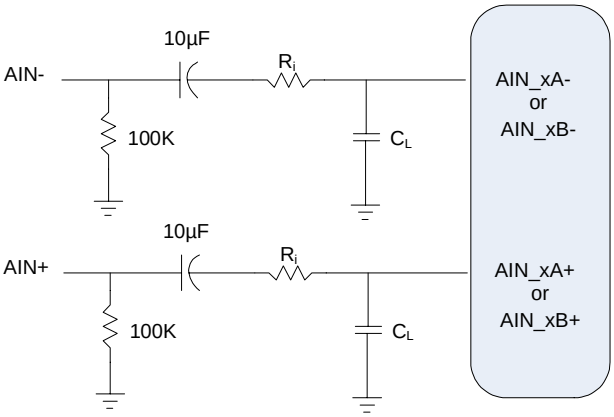


Figure 12. ADC Differential Input Test Circuit

5.16.3 ADC Digital Filter Characteristics

Parameter[1, 2]		Min	Typ	Max	Unit
Fs = 96 kHz, 192 kHz					
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.4896	Fs
Passband Ripple		-	-	0.08	dB
Stopband		0.5688	-	-	Fs
Stopband Attenuation		70	-	-	dB
Total Group Delay		-	12/Fs	-	s
High-Pass Filter Characteristics					
Frequency Response	-3.0 dB -0.13 dB	-	1 20	- -	Hz Hz
Phase Deviation	@ 20 Hz	-	10	-	Deg
Passband Ripple		-	-	0	dB
Filter Settling Time		-	10^5/Fs	0	s

Notes:

1. Filter response is guaranteed by design.
2. Response is clock-dependent and will scale with Fs.

5.17 DAC Characteristics

5.17.1 Analog Output Characteristics (Commercial)

(Test Conditions (unless otherwise specified): T_A = 0 to +70°C; VDD = 1.8V±5%, VDDA(VA) = 3.3V±5%; 1 kHz sine wave driven through a filter shown in Figure 13 on page 28 or Figure 14 on page 29; DSP running test application; Measurement Bandwidth is 20 Hz to 20 kHz.)

Parameter	Differential			Single-Ended			Unit
	Min	Typ	Max	Min	Typ	Max	
Fs = 96 kHz							
Dynamic Range							
A-weighted	102	108	-	99	105	-	dB
unweighted	99	105	-	96	102	-	dB
Total Harmonic Distortion + Noise							
0 dB	-	-98	-90	-	-95	-87	dB
-20 dB	-	-88	-	-	-85	-	dB
-60 dB	-	-48	-	-	-45	-	dB
Interchannel Isolation (1 kHz)	-	95	-	-	95	-	dB
Analog Output							
Full-Scale Output	TBD	1.35•VA	TBD	TBD	0.68•VA	TBD	V_{PP}
Interchannel Gain Mismatch	-	0.1	-	-	0.1	-	dB
Gain Drift	-	±120	-	-	±120	-	ppm/°C
Output Impedance	-	100	-	-	100	-	Ω
DC Current draw from an AOUT pin[1]	-	-	10	-	-	10	µA
AC-Load Resistance (R_L)[2]	3	-	-	3	-	-	kΩ
Load Capacitance (C_L)[2]	-	-	100	-	-	100	pF

5.17.2 Analog Output Characteristics (Automotive)

(Test Conditions (unless otherwise specified): T_A = -40 to +85°C; VDD = 1.8V±5%, VDDA(VA) = 3.3V±5%; 1 kHz sine wave driven through a filter shown in Figure 13 on page 28 or Figure 14 on page 29; DSP running test application; Measurement Bandwidth is 20 Hz to 20 kHz.)

Parameter	Differential Min	Differential Typ	Differential Max	Single-Ended Min	Single-Ended Typ	Single-Ended Max	Unit
Fs = 96 kHz							
Dynamic Range							
A-weighted	100	108	-	97	105	-	dB
unweighted	97	105	-	94	102	-	dB
Total Harmonic Distortion + Noise							
0 dB	-	-98	-90	-	-95	-87	dB
-20 dB	-	-88	-	-	-85	-	dB
-60 dB	-	-48	-	-	-45	-	dB
Interchannel Isolation (1 kHz)	-	95	-	-	95	-	dB
Analog Output							
Full-Scale Output	TBD	1.35•VA	TBD	TBD	0.68•VA	TBD	V_{PP}
Interchannel Gain Mismatch	-	0.1	-	-	0.1	-	dB
Gain Drift	-	±120	-	-	±120	-	ppm/°C
Output Impedance	-	100	-	-	100	-	Ω
DC Current draw from an AOUT pin[1]	-	-	10	-	-	10	µA
AC-Load Resistance (R_L)[2]	3	-	-	3	-	-	kΩ
Load Capacitance (C_L)[2]	-	-	100	-	-	100	pF

Notes:

1. Guaranteed by design. The DC current draw represents the allowed current draw from the AOUT pin due to typical leakage through the electrolytic DC-blocking capacitors.
2. Guaranteed by design. R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. In this circuit topology, C_L represents any capacitive loading that appears *before* the 560Ω series resistor (typically parasitic), and will effectively move the dominant pole of the two-pole amp in the output stage. Increasing this value beyond the recommended 100 pF can cause the internal op-amp to become unstable.

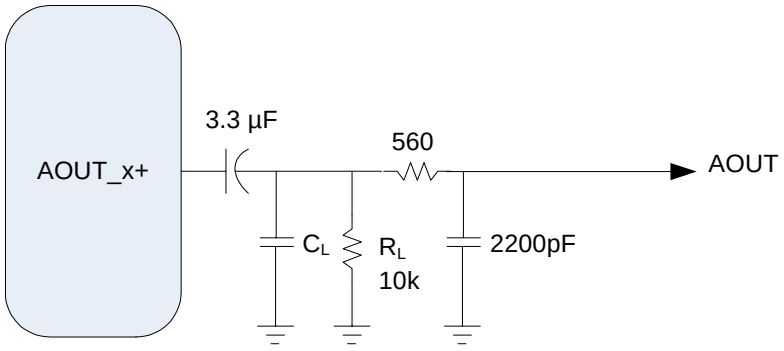
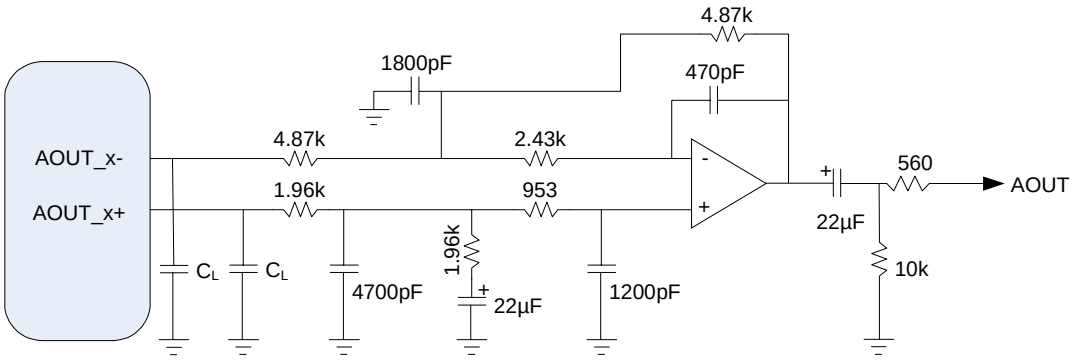


Figure 13. DAC Single-Ended Output Test Circuit



P output: $R_L = 1.96k + ([2\pi F*4700^{-12}]^{-1} || (1.96k + [2\pi F*22^{-6}]^{-1}) || (953 + [2\pi F*1200^{-12}]^{-1}))$

N output: $R_L = 4.87k + ([2\pi F*1800^{-12}]^{-1} || ((2.43k + [2\pi F*470^{-12}]^{-1}) || 4.87k))$

Figure 14. DAC Differential Output Test Circuit

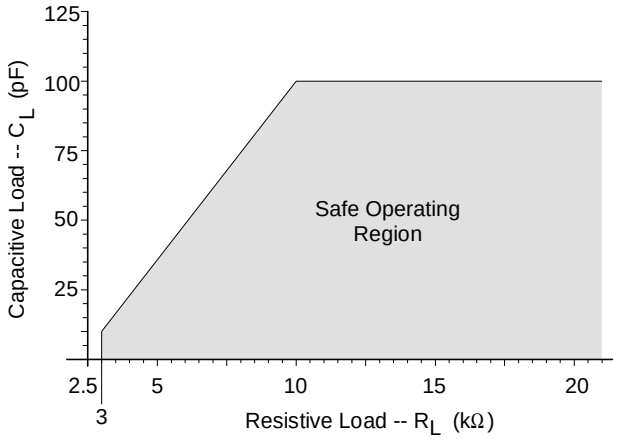


Figure 15. Maximum Loading

5.17.3 Combined DAC Interpolation & On-chip Analog Filter Response

Parameter		Min	Typ	Max	Unit
Passband (Frequency Response)	to 0.22 dB corner	0	-	0.4125	Fs
	to -3 dB corner	0	-	0.4979	Fs
Frequency Response 10 Hz to 20 kHz		-0.02	-	+0.02	dB
StopBand		0.5465	-	-	Fs
StopBand Attenuation		100	-	-	dB
Group Delay		-	10/Fs	-	s

6. Ordering Information

The CS47048 DSP part numbers are described as follows:

CS47048I-XYZR

where

I - ROM ID Letter

X - Product Grade

Y - Package Type

Z - Lead (Pb) Free

R - Tape and Reel Packaging

Table 4. Ordering Information

Part No.	Grade	Temp. Range	Package
CS47048B-CQZ	Commercial	0 to +70 °C	100-pin LQFP
CS47048B-DQZ	Automotive	-40 to +85 °C	

NOTE: Please contact the factory for availability of the -D (automotive grade) package.

7. Environmental, Manufacturing, & Handling Information

Table 5. Environmental, Manufacturing, & Handling Information

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS47048B-CQZ	260 °C	3	7 days
CS47048B-DQZ			

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

8. Device Pinout Diagram

8.1 CS47048, 100-Pin LQFP Pinout Diagram

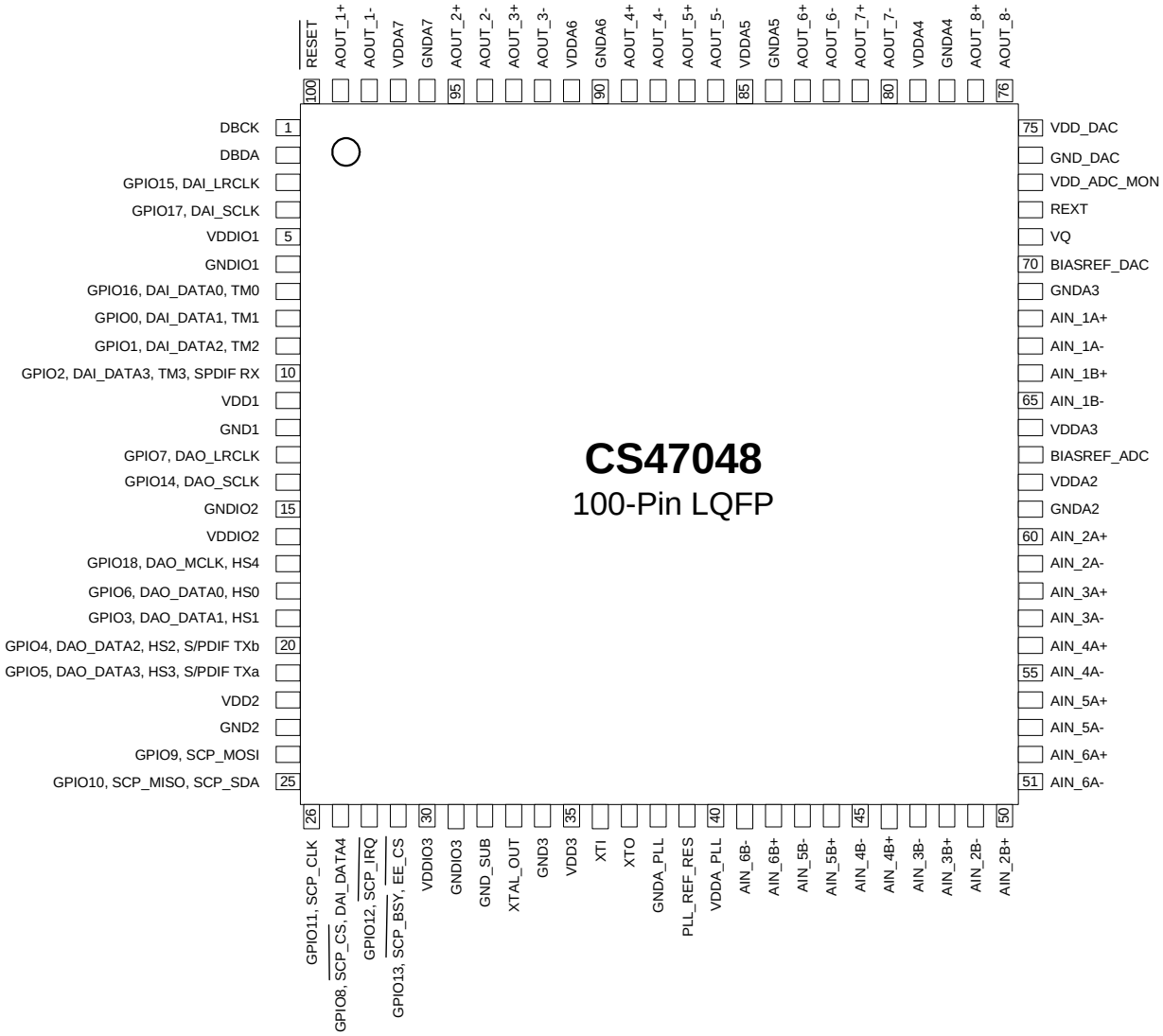
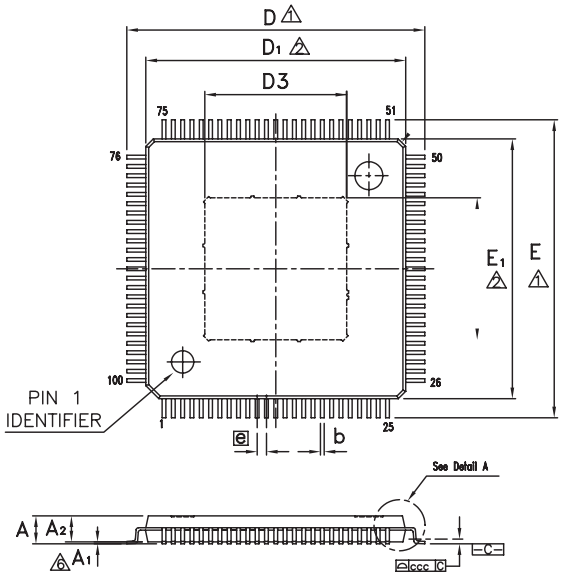
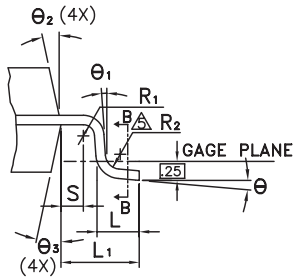


Figure 16. CS47048 Pinout Diagram

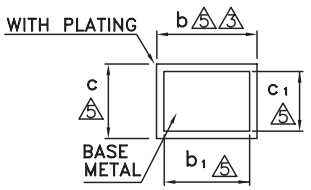
9. 100-pin LQFP with Exposed Pad Package Drawing

Figure 17 shows the CS47048 100-pin LQFP package with exposed pad.





DETAIL A



SECTION B–B

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b_1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D_1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E_1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	12°TYP					
$θ_3$						
ccc	0.08			0.003		

NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS–026.
9. **SPECIAL CHARACTERISTICS C CLASS: ccc**

Exposed Pad Size		
L/F	Dimension in mm	Dimension in inch
D3/E3	7.62 REF	0.300 REF

100LD E–PAD LQFP (14x14x1.4mm) PACKAGE OUTLINE
–Cu L/F,FOOTPRINT 2.0mm

Figure 17. 100-Pin LQFP Package Drawing

10. Parameter Definitions

10.1 Dynamic Range

The ratio of the RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

10.2 Total Harmonic Distortion + Noise

The ratio of the RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

10.3 Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

10.4 Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

10.5 Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

10.6 Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

10.7 Gain Drift

The change in gain value with temperature. Units in ppm/°C.

11. Revision History

Revision	Date	Changes
A7	October 16, 2008	Initial Release