

Structure Silicon Monolithic Integrated Circuit

Product Name Charge Pump Regulator with Selectable 5.0V/4.5V Output for mobile

Type **BD1603NUV**

**Under
Development**

Features Charge Pump LED driver
Selectable 5.0V or 4.5V output voltage

○Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Rating	Unit	Condition
Supply Voltage	V _{IN}	7.0	V	
Output Voltage	V _{OUT}	7.0	V	
Power Dissipation	P _b	TBD (*1)	mW	
Operating Ambient	T _A	-30 to +85	°C	
Storage Temperature Range	T _{STG}	-55 to +150	°C	

(*1) The measurement value which was mounted on the PCB by ROHM.
Temperature degrading : TBD W/°C from Ta>25 °C

○Recommended operating conditions (Ta=-30 to 85 °C)

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
Input Voltage Range	V _{IN}	2.7	3.6	5.5	V	

This product isn't designed to protect itself against radioactive rays.

Status of this document

The Japanese version of this document is the formal specification.
A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

Application example

- ROHM cannot provide adequate confirmation of patents.
- The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys). Should you intend to use this product with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.
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○Electrical Characteristics

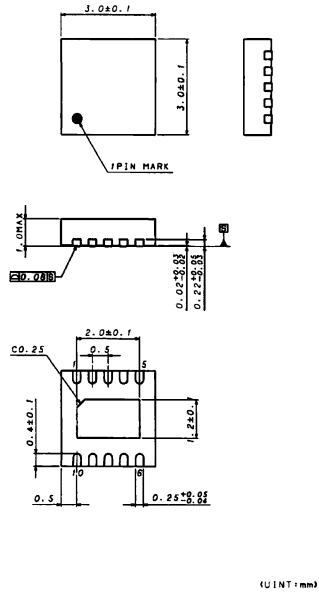
Unless otherwise specified, Ta=25 °C, VIN=3.6V

Parameter	Symbol	Spec			Unit	Condition
		Min.	Typ.	Max.		
Input Supply Voltage	V _{IN}	2.7	-	5.5	V	
Quiescent Current	I _Q	-	3.1	4.3	mA	Freq=262kHz, I _{OUT} =0mA V _{IN} =3.7V
		-	5.0	7.0	mA	Freq=650kHz, I _{OUT} =0mA V _{IN} =3.7V
		-	-	2	μA	EN=0
Output Voltage	V _{OUT}	4.75	5.0	5.25	V	Static Load Regulation with VSEL=1
		4.275	4.5	4.725	V	Static Load Regulation with VSEL=0
Output Current	I _{OUT}	-	-	150	mA	VSEL=1, 3.2V < V _{IN} < 5.5V
		-	-	190	mA	VSEL=0, 3.2V < V _{IN} < 5.5V
		-	-	60	mA	VSEL=1, 2.85V < V _{IN} < 5.5V
		-	-	120	mA	VSEL=0, 2.85V < V _{IN} < 5.5V
Pump Frequency	f _{PUMP}	-15%	262	+15%	kHz	EN=1, FSEL=0
		-20%	650	+20%	kHz	EN=1, FSEL=1
Frequency Mode Transition Time	T _{CLOCK}	-	1	-	Period	Transition time from one frequency mode to any other frequency mode guaranteed by design
Short Circuit Current	I _{SC}	-	-	600	mA	V _{OUT} =0V, I _{OUT} =I _{IN}
Input High Threshold	V _{IH}	1.3	-	-	V	All input pins (EN, VSEL, FSEL)
Input Low Threshold	V _{IL}	-	-	0.4	V	All input pins (EN, VSEL, FSEL)
Input High Current	I _{IH}	-	-	10	μA	All input pins (EN, VSEL, FSEL)
Input Low Current	I _{IL}	-	-	10	μA	All input pins (EN, VSEL, FSEL)
Power Efficiency from Battery to Regulated Charge Pump Output	η	-	75.0	-	%	V _{IN} =3.3V, V _{OUT} =5.0V, I _{OUT} =60mA Freq=262kHz
		-	74.5	-	%	V _{IN} =3.3V, V _{OUT} =5.0V, I _{OUT} =60mA Freq=650kHz
Output Ripple Voltage	V _{PP}	-	25	45	mV	Freq=262kHz, I _{OUT} =60mA ⁽¹⁾⁽²⁾

Note (1) Peak to peak output ripple voltage with C_{OUT}=C_{BUCKET}=1μF and X5R dielectric

(2) Guaranteed by design

External dimensions



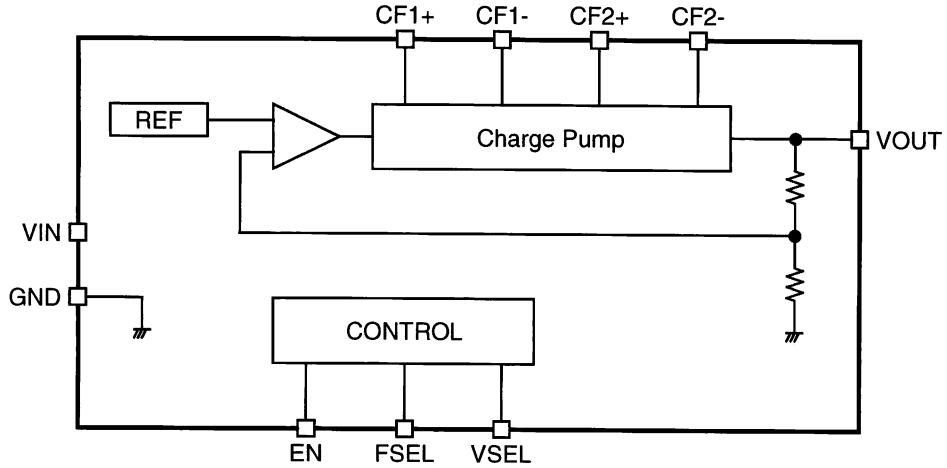
Drawing No. EX184-6001

Terminals

PIN	PIN Name	PIN	PIN Name
1	VOUT		
2	CF1+		
3	VIN		
4	FSEL		
5	VSEL		
6	EN		
7	CF2-		
8	GND		
9	CF1-		
10	CF2+		

VSON010V3030(10PIN) (Unit : mm)

Block diagram



○Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Power supply and GND line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and GND lines. Especially, when there are GND pattern for small signal and GND pattern for large current included the external circuits, please separate each GND pattern. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(4) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(5) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(8) Thermal shutdown circuit (TSD)

This LSI builds in a thermal shutdown (TSD) circuit. When junction temperatures become detection temperature or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(9) Thermal design

Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

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