

HD74LV4040A

12-stage Binary Counter

REJ03D0337-0200Z
 (Previous ADE-205-282 (Z))
 Rev.2.00
 Jul. 20, 2004

Description

The HD74LV4040A is a 12 stage counter. This device is incremented on the falling edge (negative transition) of the input clock, and all its output is reset to a low level by applying a logical high on its reset input. Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

Features

- $V_{CC} = 2.0\text{ V}$ to 5.5 V operation
- All inputs $V_{IH}(\text{Max.}) = 5.5\text{ V}$ ($@V_{CC} = 0\text{ V}$ to 5.5 V)
- All outputs $V_O(\text{Max.}) = 5.5\text{ V}$ ($@V_{CC} = 0\text{ V}$)
- Typical V_{OL} ground bounce $< 0.8\text{ V}$ ($@V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Typical V_{OH} undershoot $> 2.3\text{ V}$ ($@V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Output current $\pm 6\text{ mA}$ ($@V_{CC} = 3.0\text{ V}$ to 3.6 V), $\pm 12\text{ mA}$ ($@V_{CC} = 4.5\text{ V}$ to 5.5 V)
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV4040AFPEL	SOP-16 pin (JEITA)	FP-16DAV	FP	EL (2,000 pcs/reel)
HD74LV4040ARPEL	SOP-16 pin (JEDEC)	FP-16DNV	RP	EL (2,500 pcs/reel)
HD74LV4040ATELL	TSSOP-16 pin	TTP-16DAV	T	ELL (2,000 pcs/reel)

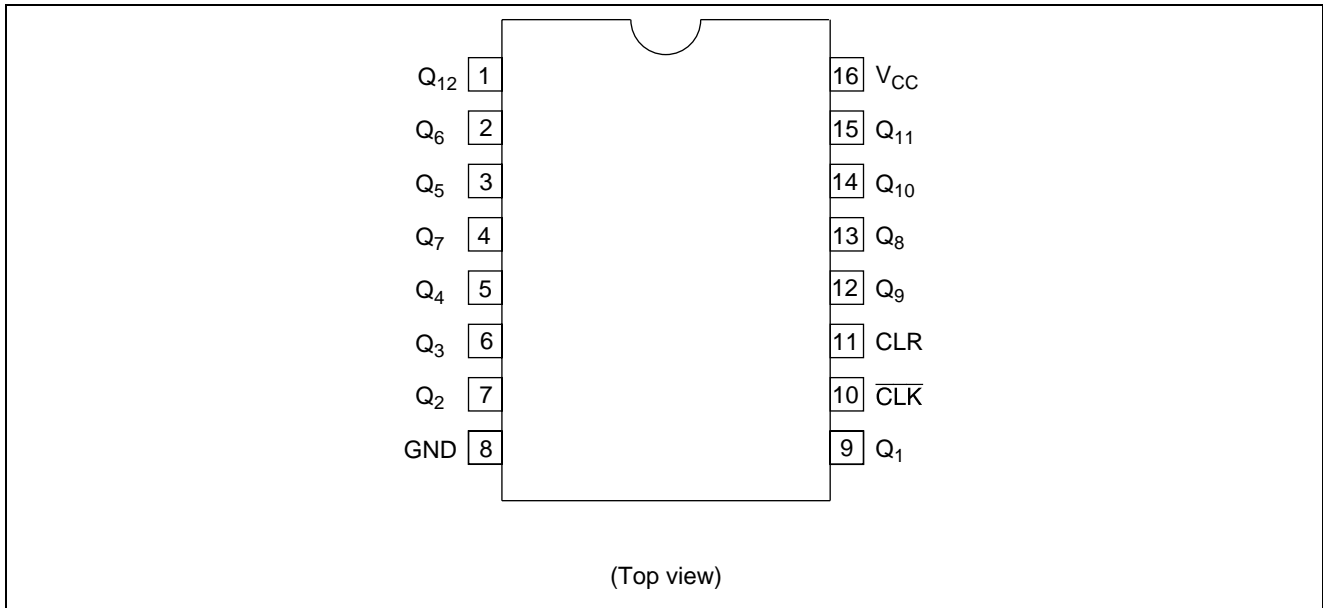
Note: Please consult the sales office for the above package availability.

Function Table

Inputs		Output
CLK	CLR	Q_n
↑	L	Remains unchanged
↓	L	Changed
X	H	All outputs low

Note: H: High level
 L: Low level
 X: Immaterial
 ↑: Low to high transition
 ↓: High to low transition

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	-0.5 to 7.0	V	
Input voltage range* ¹	V_I	-0.5 to 7.0	V	
Output voltage range* ^{1, 2}	V_O	-0.5 to $V_{CC} + 0.5$ -0.5 to 7.0	V	Output: H or L V_{CC} : OFF
Input clamp current	I_{IK}	-20	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±25	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±50	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air)* ³	P_T	785 500	mW	SOP TSSOP
Storage temperature	T_{stg}	-65 to 150	°C	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

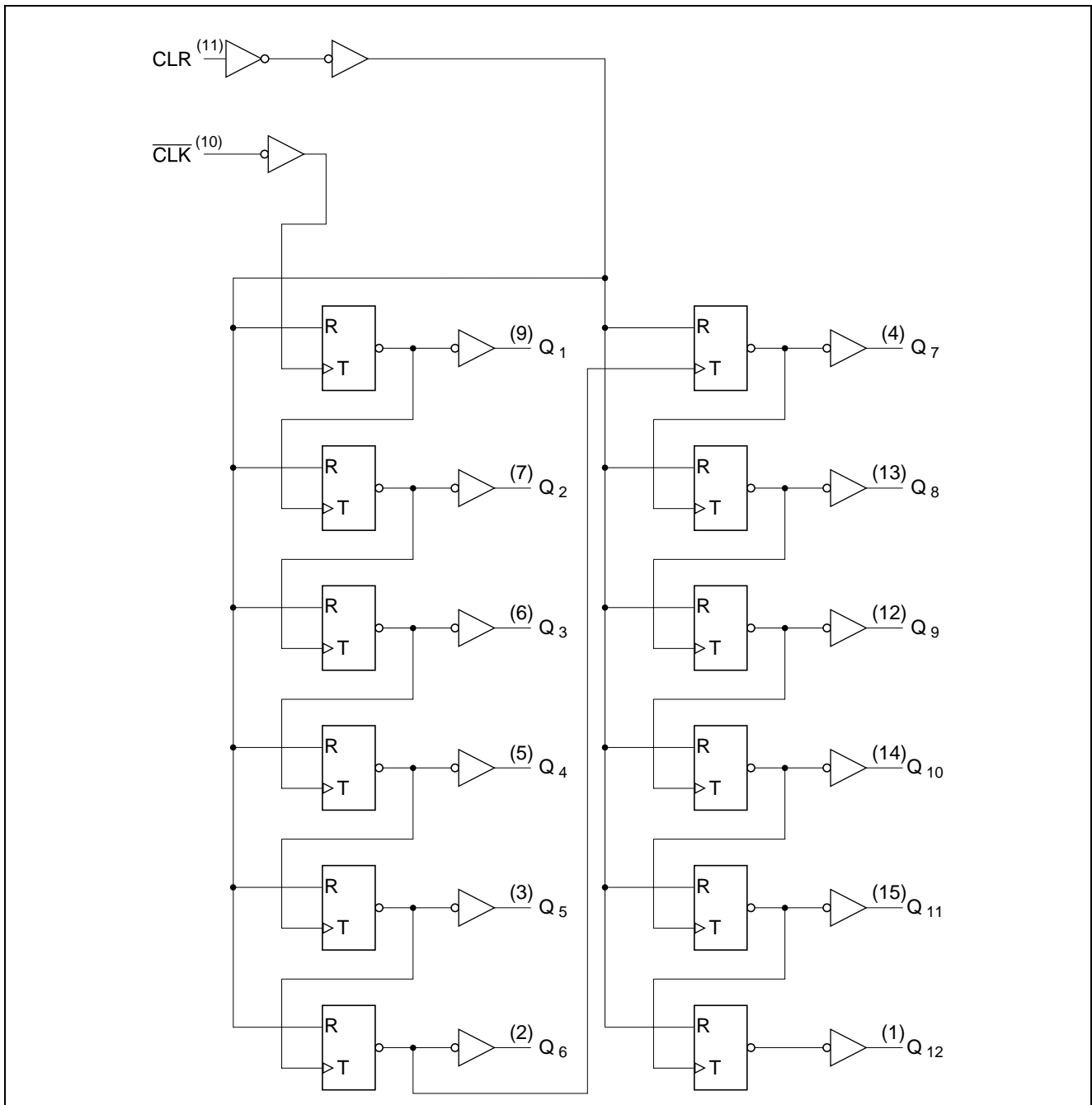
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

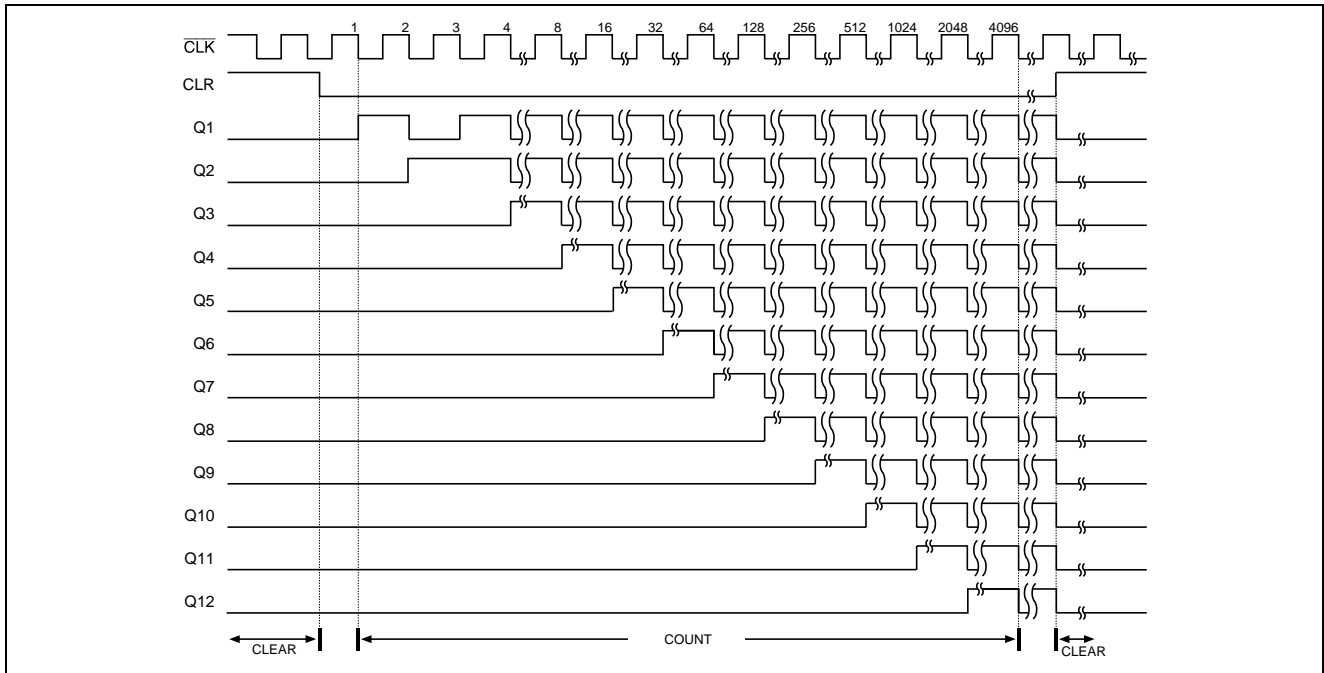
Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	V_{CC}	V	H or L
Output current	I_{OH}	—	-50	μA	$V_{CC} = 2.0 V$
		—	-2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	-6		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	-12		$V_{CC} = 4.5 \text{ to } 5.5 V$
	I_{OL}	—	50	μA	$V_{CC} = 2.0 V$
		—	2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	6		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	12		$V_{CC} = 4.5 \text{ to } 5.5 V$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	200	ns/V	$V_{CC} = 2.3 \text{ to } 2.7 V$
		0	100		$V_{CC} = 3.0 \text{ to } 3.6 V$
		0	20		$V_{CC} = 4.5 \text{ to } 5.5 V$
Operating free-air temperature	T_a	-40	85	$^{\circ}C$	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



Timing Diagram



DC Electrical Characteristics

Ta = -40 to 85°C

Item	Symbol	V _{CC} (V)*	Min	Typ	Max	Unit	Test Conditions
Input voltage	V _{IH}	2.0	1.5	—	—	V	
		2.3 to 2.7	V _{CC} ×0.7	—	—		
		3.0 to 3.6	V _{CC} ×0.7	—	—		
		4.5 to 5.5	V _{CC} ×0.7	—	—		
	V _{IL}	2.0	—	—	0.5		
		2.3 to 2.7	—	—	V _{CC} ×0.3		
		3.0 to 3.6	—	—	V _{CC} ×0.3		
		4.5 to 5.5	—	—	V _{CC} ×0.3		
Output voltage	V _{OH}	Min to Max	V _{CC} -0.1	—	—	V	I _{OH} = -50 μA
		2.3	2.0	—	—		I _{OH} = -2 mA
		3.0	2.48	—	—		I _{OH} = -6 mA
		4.5	3.8	—	—		I _{OH} = -12 mA
	V _{OL}	Min to Max	—	—	0.1		I _{OL} = 50 μA
		2.3	—	—	0.4		I _{OL} = 2 mA
		3.0	—	—	0.44		I _{OL} = 6 mA
		4.5	—	—	0.55		I _{OL} = 12 mA
Input current	I _{IN}	0 to 5.5	—	—	±1	μA	V _{IN} = 5.5 V or GND
Quiescent supply current	I _{CC}	5.5	—	—	20	μA	V _{IN} = V _{CC} or GND, I _O = 0
Output leakage current	I _{OFF}	0	—	—	5	μA	V _I or V _O = 0 to 5.5 V
Input capacitance	C _{IN}	3.3	—	3.7	—	pF	V _I = V _{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

V_{CC} = 2.5 ± 0.2 V

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f _{max}	50	90	—	40	—	MHz	C _L = 15 pF		
		30	60	—	25	—		C _L = 50 pF		
Propagation delay time	t _{PLH} /t _{PHL}	—	10.0	16.0	1.0	18.3	ns	C _L = 15 pF	CLK	Q ₁
		—	12.7	19.6	1.0	22.2		C _L = 50 pF		
	t _{PHL}	—	9.9	15.4	1.0	17.5	ns	C _L = 15 pF	CLR	
		—	11.8	18.0	1.0	20.4		C _L = 50 pF		
Propagation delay time skew	Δt _{pd}	—	3.0	5.5	—	6.3	ns	C _L = 50 pF	Q _n	Q _{n+1}
Setup time	t _{SU}	7.0	—	—	7.0	—	ns		CLR inactive before CLK ↓	
Pulse width	t _w	7.0	—	—	7.0	—	ns		CLK high or low	
		7.0	—	—	7.0	—		CLR high		

V_{CC} = 3.3 ± 0.3 V

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f _{max}	75	140	—	70	—	MHz	C _L = 15 pF		
		55	80	—	50	—		C _L = 50 pF		
Propagation delay time	t _{PLH} /t _{PHL}	—	7.5	11.9	1.0	14.0	ns	C _L = 15 pF	CLK	Q ₁
		—	10.0	15.4	1.0	17.5		C _L = 50 pF		
	t _{PHL}	—	8.3	12.8	1.0	15.0	ns	C _L = 15 pF	CLR	
		—	10.8	16.3	1.0	18.5		C _L = 50 pF		
Propagation delay time skew	Δt _{pd}	—	2.4	4.4	—	5.0	ns	C _L = 50 pF	Q _n	Q _{n+1}
Setup time	t _{SU}	5.0	—	—	5.0	—	ns		CLR inactive before CLK ↓	
Pulse width	t _w	5.0	—	—	5.0	—	ns		CLK high or low	
		5.0	—	—	5.0	—		CLR high		

Switching Characteristics (Cont.)

V_{CC} = 5.0 ± 0.5 V

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f _{max}	150	210	—	125	—	MHz	C _L = 15 pF		
		95	125	—	80	—		C _L = 50 pF		
Propagation delay time	t _{PLH} /t _{PHL}	—	4.8	7.3	1.0	8.5	ns	C _L = 15 pF	CLK	Q ₁
		—	6.3	9.3	1.0	10.5		C _L = 50 pF		
	t _{PHL}	—	5.6	8.6	1.0	10.0	ns	C _L = 15 pF	CLR	
		—	7.1	10.6	1.0	12.0		C _L = 50 pF		
Propagation delay time skew	Δt _{pd}	—	1.6	3.1	—	3.5	ns	C _L = 50 pF	Q _n	Q _n + 1
Setup time	t _{SU}	5.0	—	—	5.0	—	ns		CLR inactive before CLK ↓	
Pulse width	t _w	5.0	—	—	5.0	—	ns		CLK high or low	
		5.0	—	—	5.0	—		CLR high		

Operating Characteristics

C_L = 50 pF

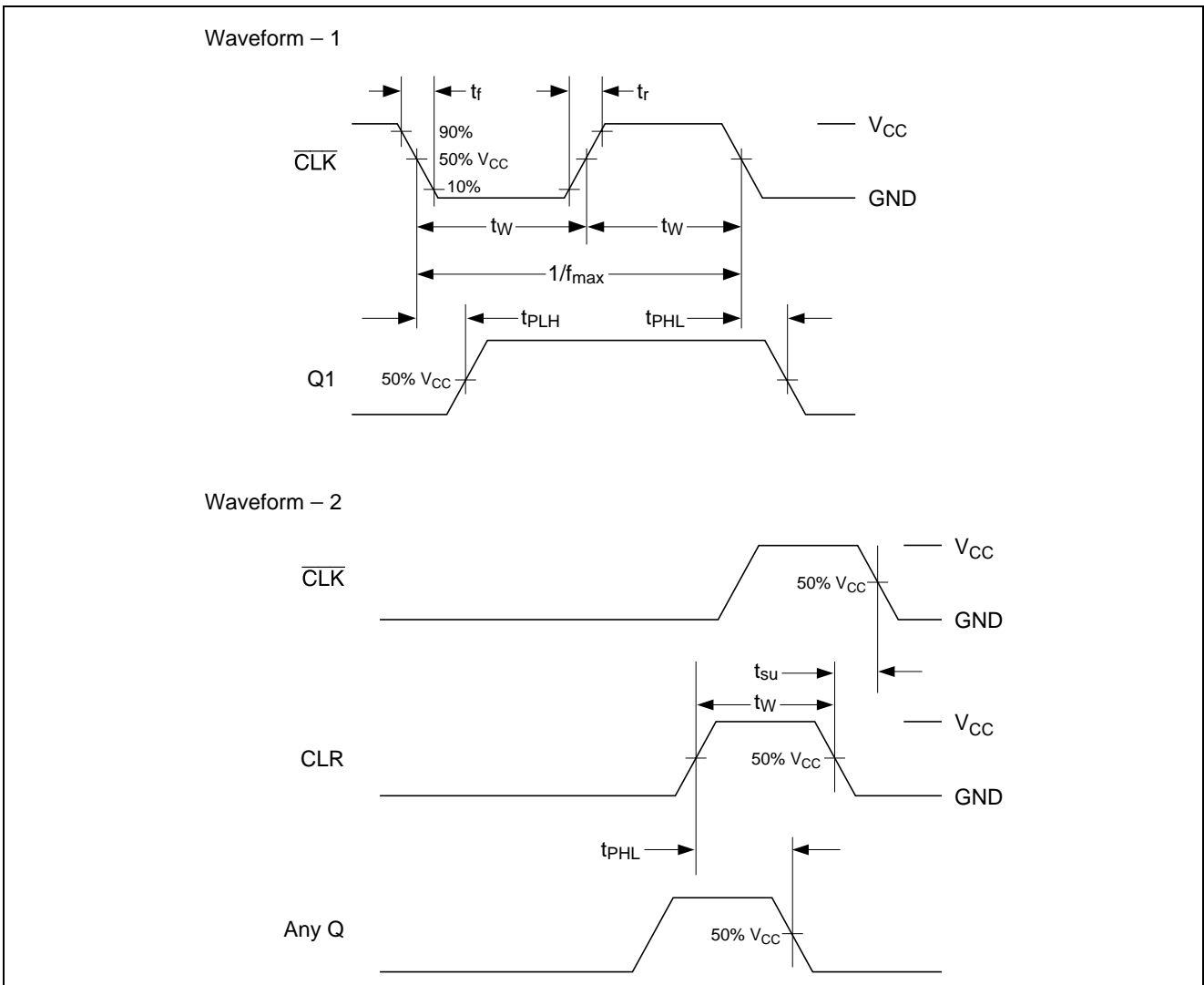
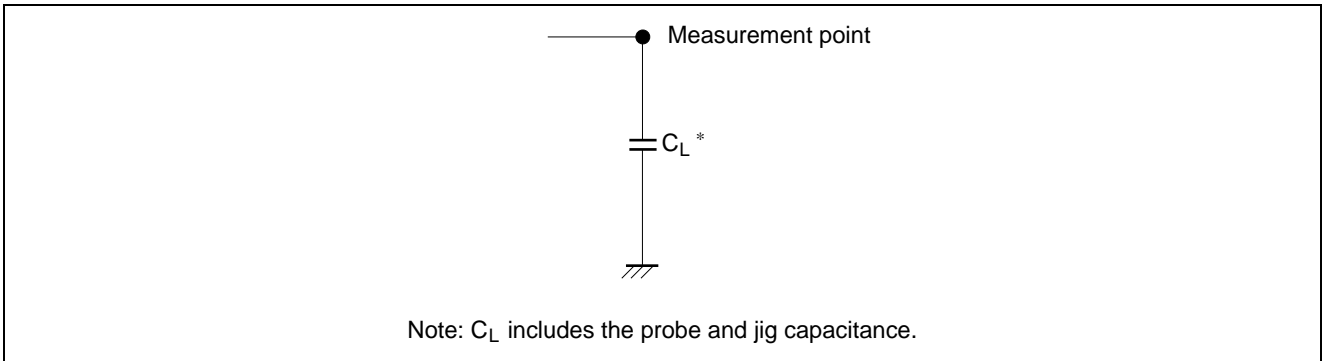
Item	Symbol	V _{CC} = (V)	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C _{PD}	3.3	—	17.3	—	pF	f = 10 MHz
		5.0	—	19.0	—		

Noise Characteristics

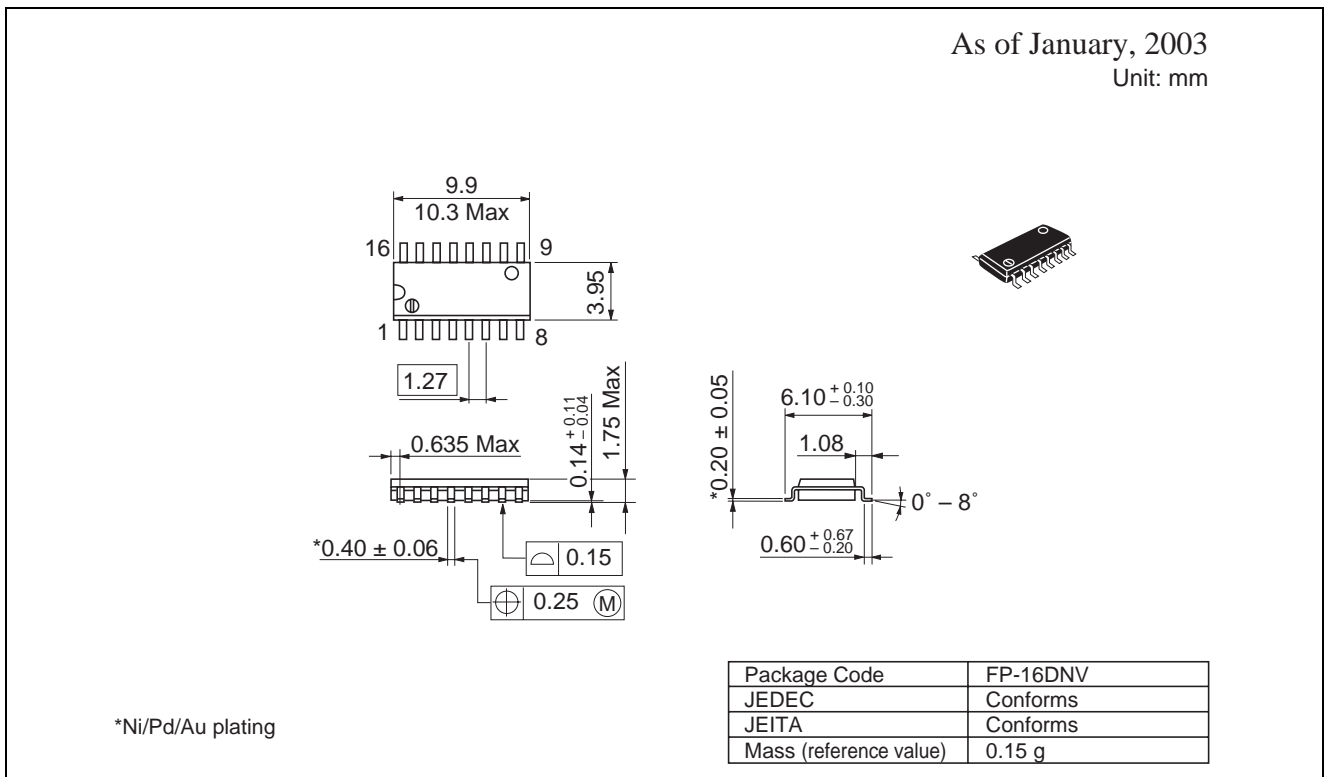
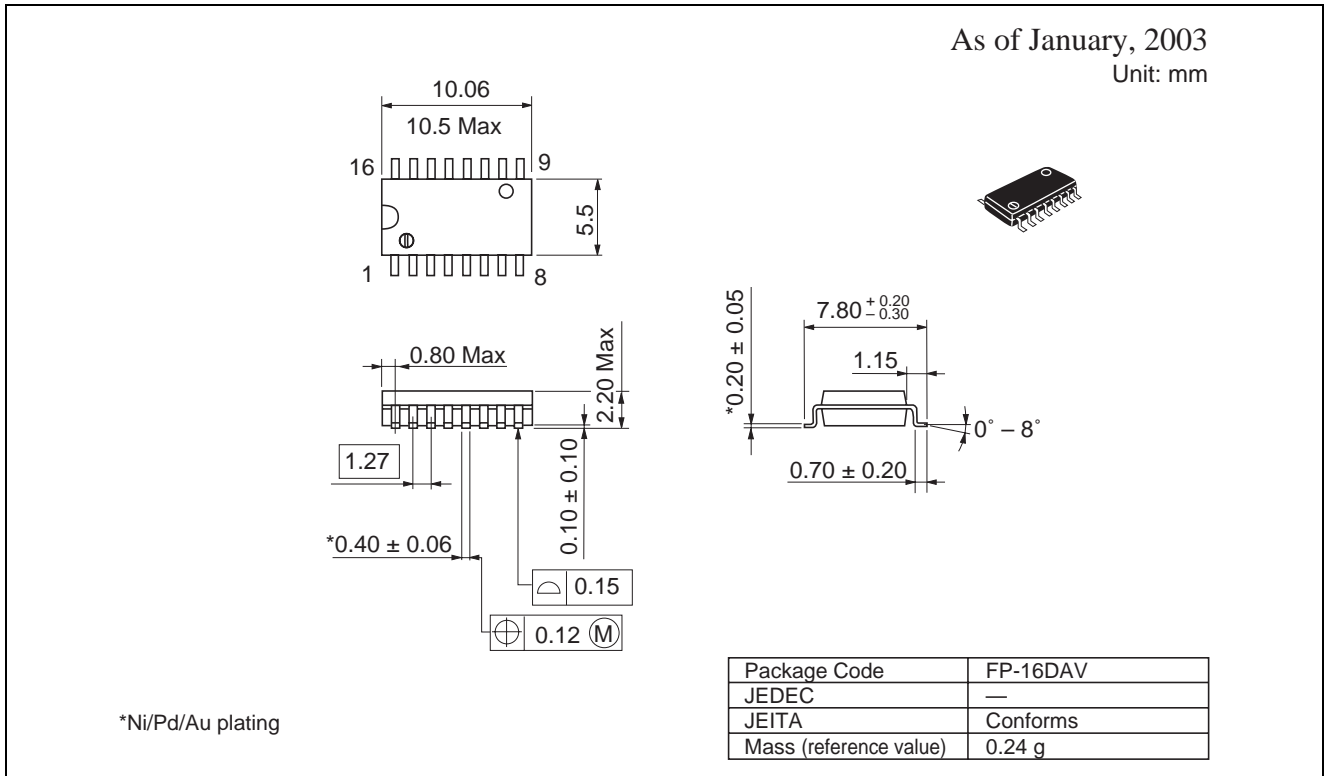
C_L = 50 pF

Item	Symbol	V _{CC} = (V)	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Quiet output, maximum dynamic V _{OL}	V _{OL(P)}	3.3	—	0.4	0.8	V	
Quiet output, minimum dynamic V _{OL}	V _{OL(V)}	3.3	—	-0.5	-0.8	V	
Quiet output, minimum dynamic V _{OH}	V _{OH(V)}	3.3	—	3.0	—	V	
High-level dynamic input voltage	V _{IH(D)}	3.3	2.31	—	—	V	
Low-level dynamic input voltage	V _{IL(D)}	3.3	—	—	0.99	V	

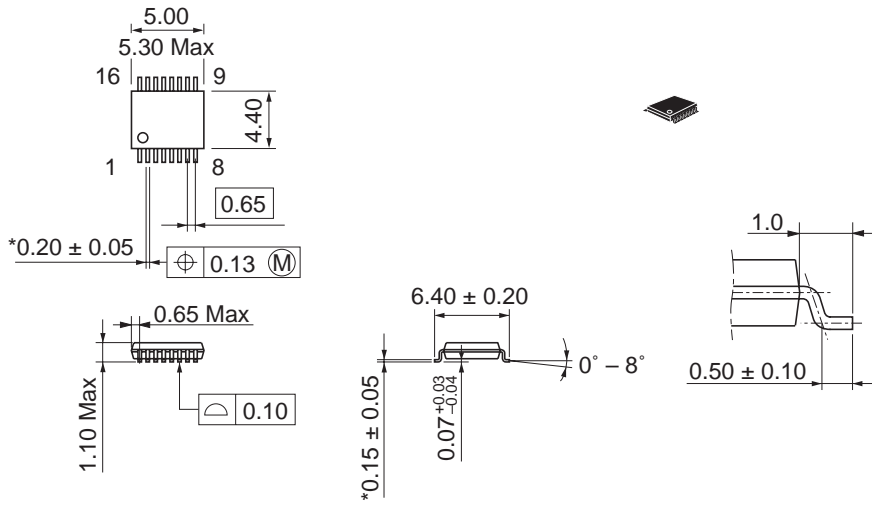
Test Circuit



Package Dimensions



As of January, 2003
Unit: mm



*Ni/Pd/Au plating

Package Code	TTP-16DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

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