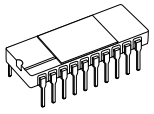
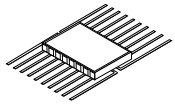
M54HC573

RAD-HARD OCTAL D-TYPE LATCH WITH 3 STATE OUTPUT NON INVERTING

- HIGH SPEED:
  t_{PD} = 13ns (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  I_{CC} = 4µA(MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY:
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 6mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 54 SERIES 573
- SPACE GRADE-1: ESA SCC QUALIFIED
- 50 krad QUALIFIED, 100 krad AVAILABLE ON REQUEST
- NO SEL UNDER HIGH LET HEAVY IONS IRRADIATION
- DEVICE FULLY COMPLIANT WITH SCC-9202-072



DILC-20



FPC-20

ORDER CODES

PACKAGE	FM	EM
DILC	M54HC573D	M54HC573D1
FPC	M54HC573K	M54HC573K1

DESCRIPTION

The M54HC573 is an high speed CMOS OCTAL LATCH WITH 3-STATE OUTPUTS fabricated with silicon gate C^2MOS technology.

This 8-BIT D-Type latches is controlled by a latch enable input (LE) and output enable input ($\overline{OE}$).

While the LE input is held at a high level, the Q outputs will follow the data input precisely. When LE is taken low, the Q outputs will be latched precisely at the logic level of D input data.

While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while is at high level the outputs will be in a high impedance state.

The 3-State output configuration and the wide choice of outline make bus organized system simple.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION

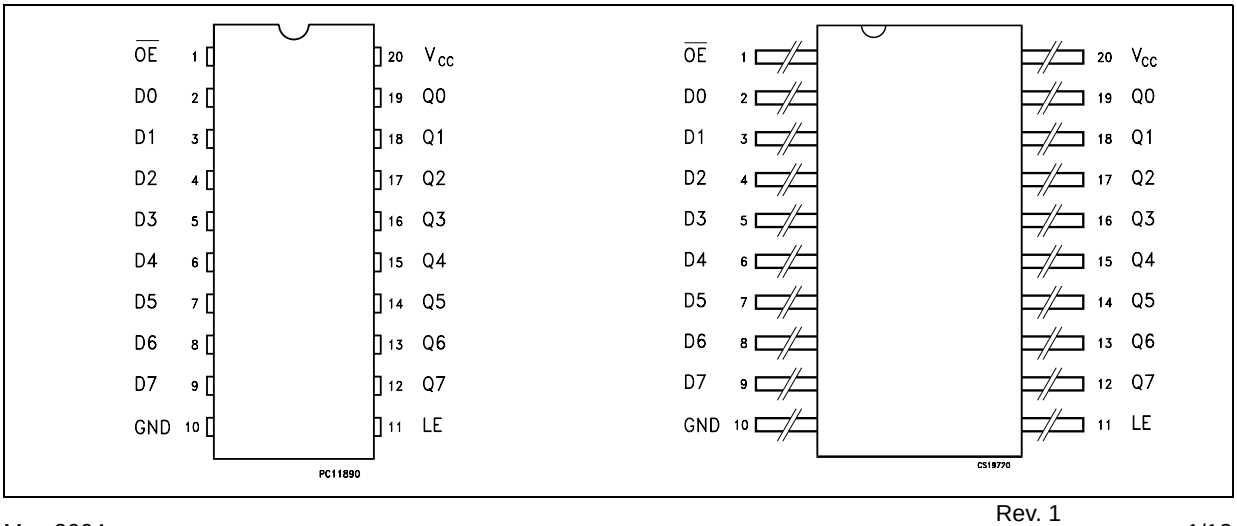


Figure 1: IEC Logic Symbols

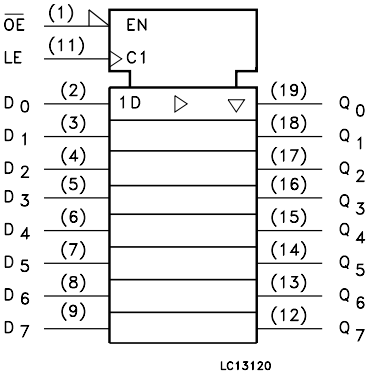


Figure 2: Input And Output Equivalent Circuit

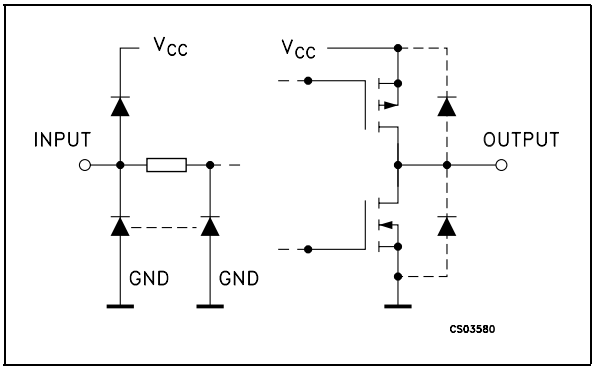


Table 1: Pin Description

PIN N°	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State Output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	Q0 to Q7	3 State Latch Outputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

Table 2: Truth Table

INPUTS			OUTPUTS
$\overline{OE}$	LE	D	Q
H	X	X	Z
L	L	X	NO CHANGE (*)
L	H	L	L
L	H	H	H

X: Don't Care
Z: High Impedance
(*): Q Outputs are latched at the time when the LE input is taken low logic level.

Figure 3: Logic Diagram

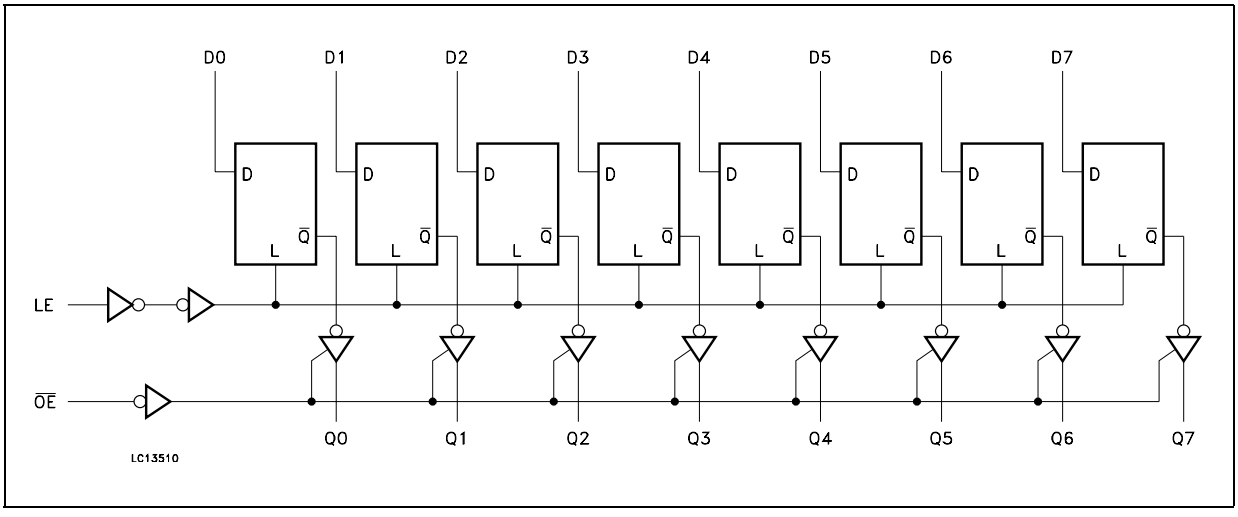


Table 3: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	420	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	265	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

Table 4: Recommended Operating Conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

Table 5: DC Specifications

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	I_O=20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O=6.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O=7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA
I_{OZ}	High Impedance Output Leakage Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND			± 0.5		± 5		± 10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND			4		40		80	µA

Table 6: AC Electrical Characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6ns)

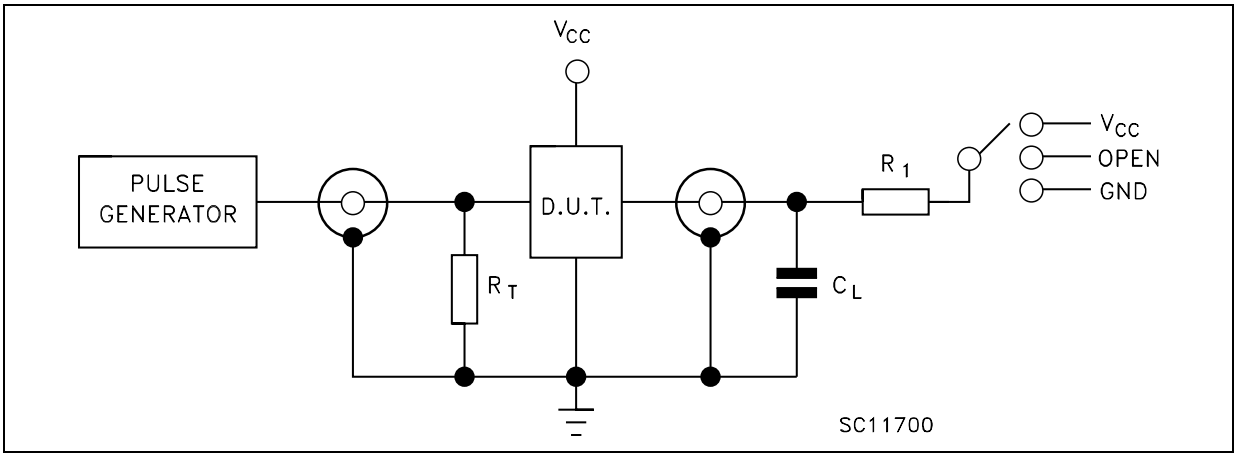
Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time (LE - Q)	2.0	50			50	115		145		175	ns
		4.5				15	23		29		35	
		6.0				13	20		25		30	
		2.0	150			60	155		195		235	ns
		4.5				20	31		39		47	
		6.0				17	26		33		40	
t_{PLH} t_{PHL}	Propagation Delay Time (D - Q)	2.0	50			42	110		140		165	ns
		4.5				14	22		28		33	
		6.0				12	19		24		28	
		2.0	150			57	150		190		225	ns
		4.5				19	30		38		45	
		6.0				16	26		32		38	
t_{PZL} t_{PZH}	High Impedance Output Enable Time	2.0	50	R_L = 1 KΩ		55	140		175		210	ns
		4.5				17	28		35		42	
		6.0				14	24		30		36	
		2.0	150	R_L = 1 KΩ		66	180		225		270	ns
		4.5				22	36		45		54	
		6.0				19	31		38		46	
t_{PLZ} t_{PHZ}	High Impedance Output Disable Time	2.0	50	R_L = 1 KΩ		40	125		155		190	ns
		4.5				17	25		31		38	
		6.0				15	21		26		32	
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width	2.0	50			40	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
t_s	Minimum Set-up Time	2.0	50			16	50		65		75	ns
		4.5				5	10		13		15	
		6.0				3	9		11		13	
t_h	Minimum Hold Time	2.0	50				5		5		5	ns
		4.5					5		5		5	
		6.0					5		5		5	

Table 7: Capacitive Characteristics

Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)			T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{OUT}	Output Capacitance					10						pF
C_{PD}	Power Dissipation Capacitance (note 1)					51						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per Flip Flop) and the C_{PD} when n pcs of Flip Flop operate, can be gained by the following equation: $C_{PD(TOTAL)} = 33 + 18 \times n$ (pF)

Figure 4: Test Circuit



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{CC}
t_{PZH}, t_{PHZ}	GND

C_L = 50pF/150pF or equivalent (includes jig and probe capacitance)
R_1 = 1KΩ or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

Figure 5: Waveform - LE To Qn Propagation Delays, LE Minimum Pulse Width, Dn To LE Setup And Hold Times (f=1MHz; 50% duty cycle)

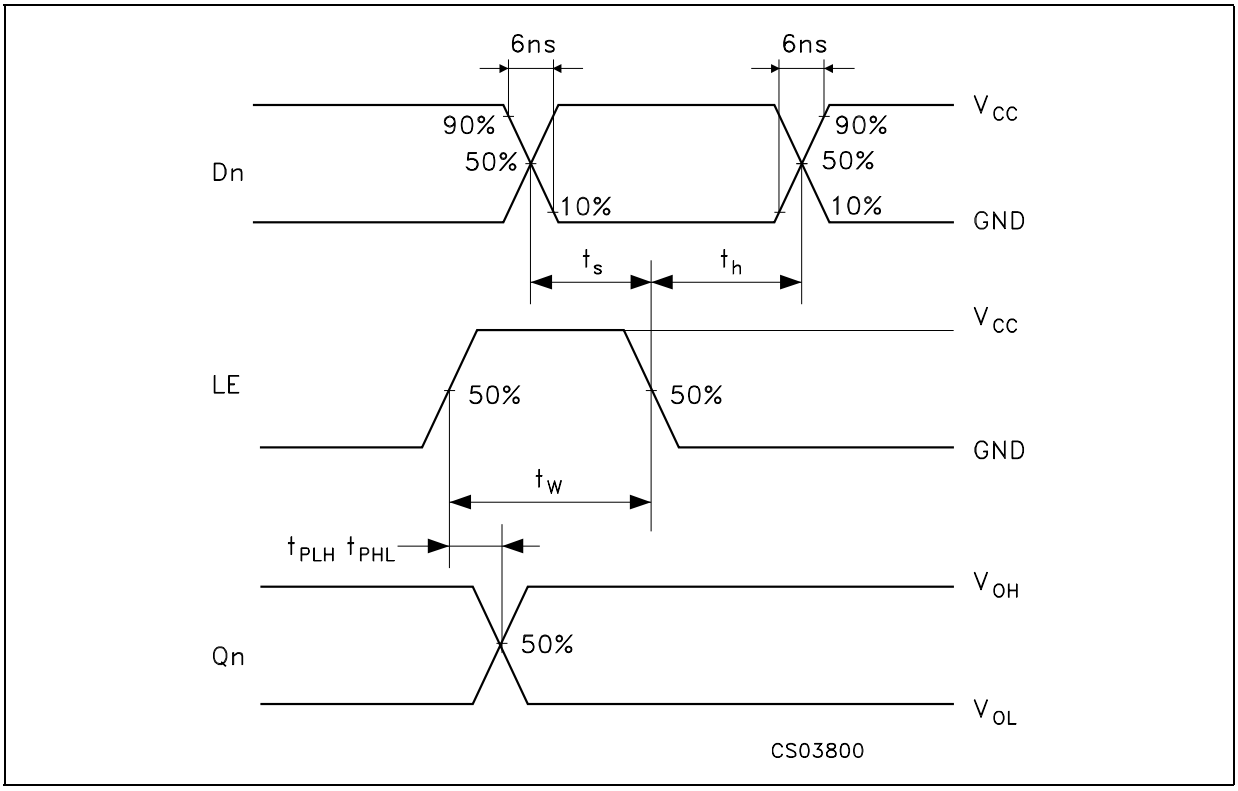


Figure 6: Waveform - Output Enable And Disable Times (f=1MHz; 50% duty cycle)

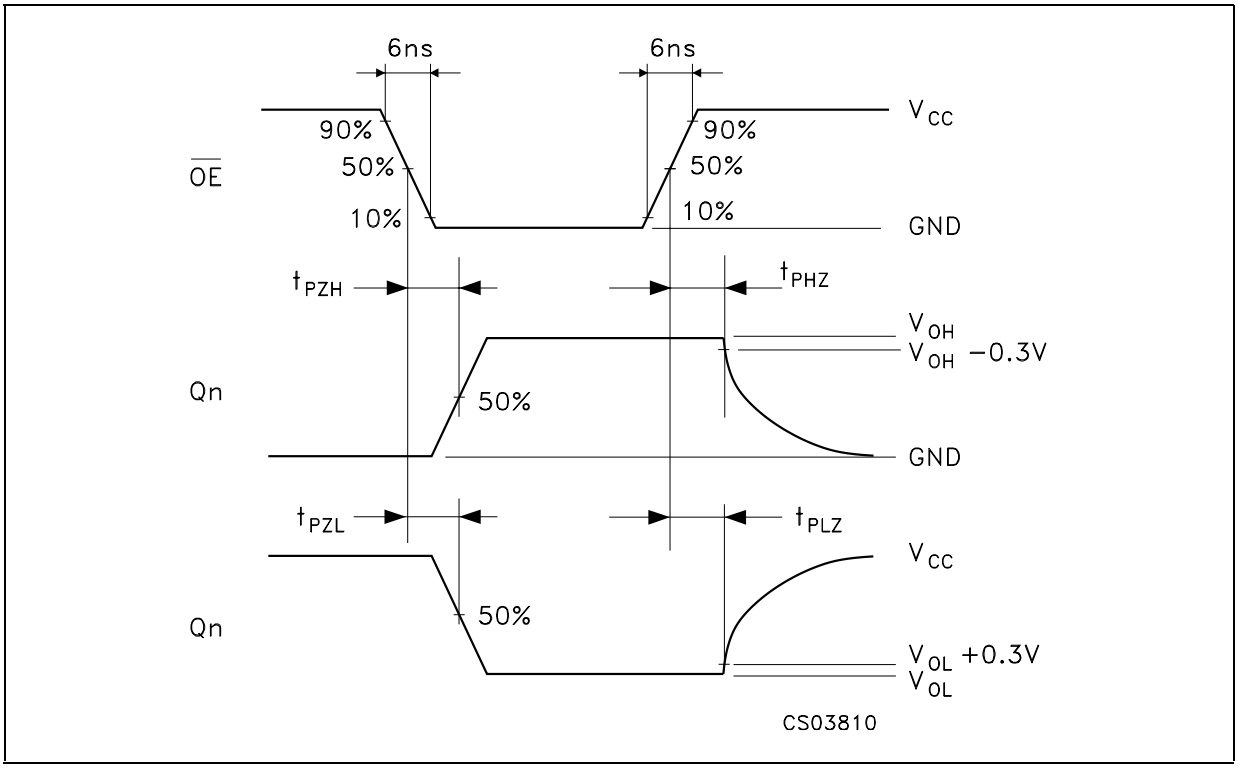
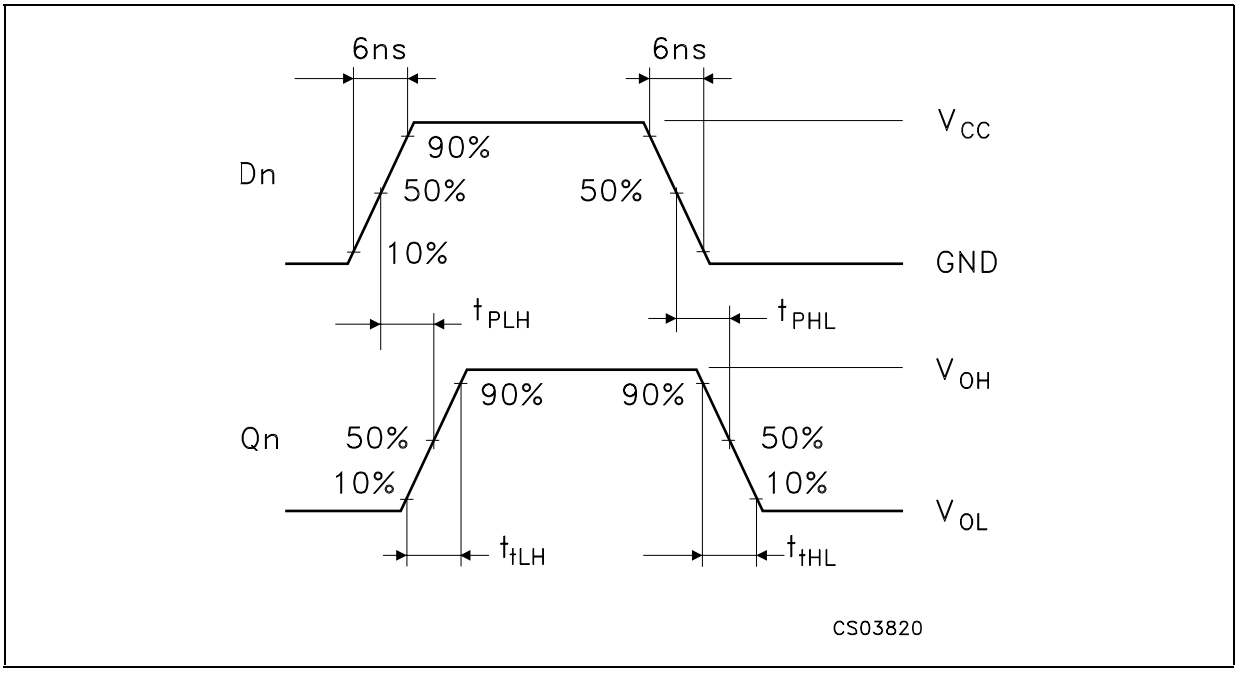
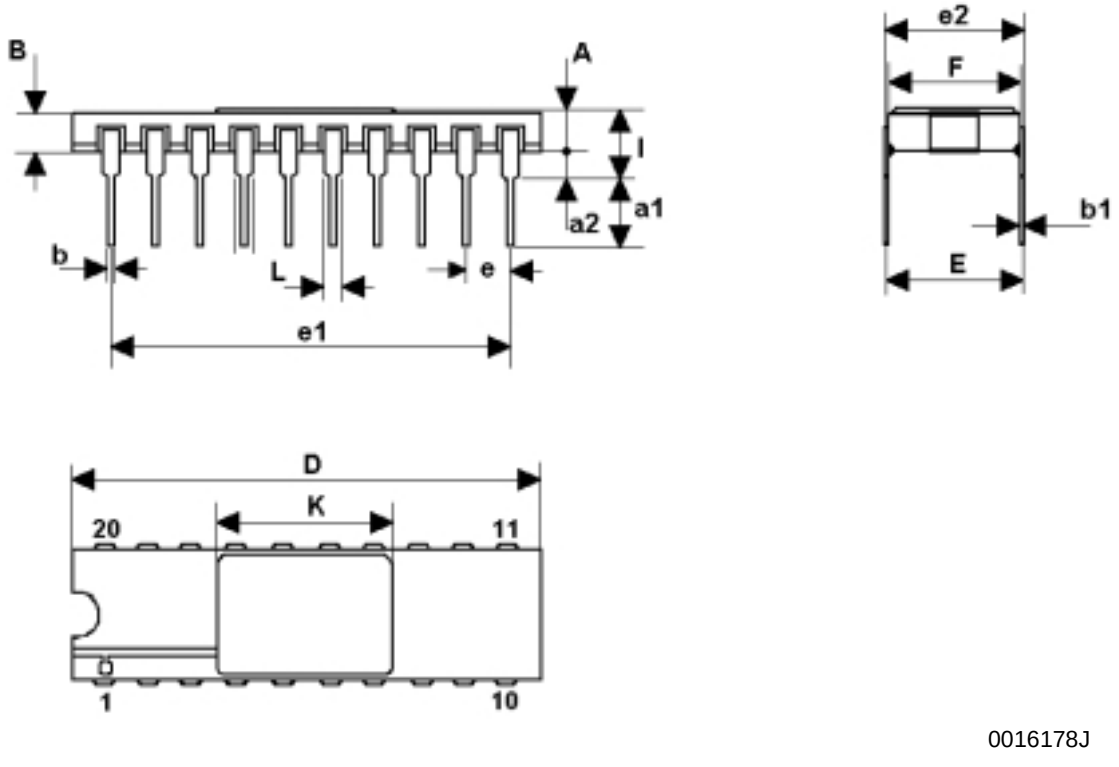


Figure 7: Waveform - Propagation Delay Times (f=1MHz; 50% duty cycle)



DILC-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.1		2.71	0.083		0.107
a1	3.00		3.70	0.118		0.146
a2	0.63	0.88	1.14	0.025	0.035	0.045
B	1.93	2.03	2.23	0.076	0.080	0.088
b	0.40	0.45	0.50	0.016	0.018	0.020
b1	0.20	0.254	0.30	0.008	0.010	0.012
D	25.14	25.40	25.65	0.990	1.000	1.010
E	7.36	7.62	7.87	0.290	0.300	0.310
e		2.54			0.100	
e1	22.73	22.86	22.99	0.895	0.900	0.905
e2	7.62	7.87	8.12	0.300	0.310	0.320
F	7.29	7.49	7.70	0.287	0.295	0.303
I			3.86			0.152
K	11.30		11.56	0.445		0.455
L	1.14	1.27	1.40	0.045	0.050	0.055



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FPC-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	9.98	10.16	10.34	0.393	0.400	0.407
B	9.98	10.16	10.34	0.393	0.400	0.407
C	1.45	1.61	1.78	0.57	0.63	0.070
D	0.10	0.127	0.18	0.004	0.005	0.007
E	11.30	11.43	11.56	0.445	0.450	0.455
F		1.27			0.050	
G	0.38	0.43	0.48	0.015	0.017	0.019
H	7.24		8.16	0.285		0.320
L	24.46		26.67	0.960		1.050
M	0.45	0.50	0.55	0.018	0.020	0.022
N		7.87			0.310	
O	1.14	1.27	1.40	0.045	0.050	0.055
P	0.10	0.18	0.25	0.004	0.007	0.010

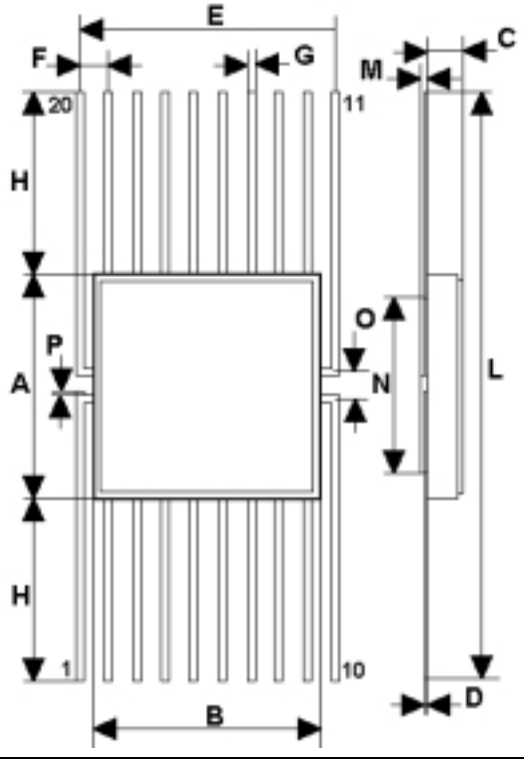

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Table 8: Revision History

Date	Revision	Description of Changes
14-May-2004	1	First Release