Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note: Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp. Customer Support Dept. April 1, 2003



PLL-SPLIT VIF/SIF

DESCRIPTION

M52769FP is a semiconductor integrated circuit consisting of VIF/SIF signal processing for CTVs and VCRs. M52769FP corresponds to FM radio and provide low cost and high performance system with the coil-less AFT.

FEATURES

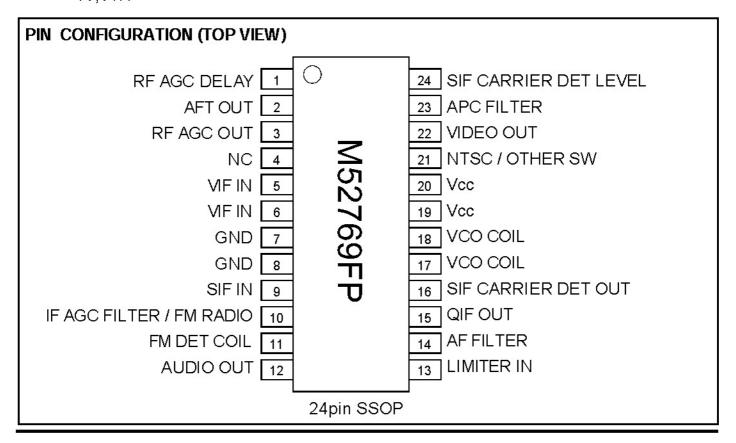
- FM radio receiving is a vailable without FM radio IC and external filter
- Built-in FM radio carrier indicator
- Coil-less AFT.
- The PLL-SPLIT system provides good sound sensitivity and reduces buzz.
- Video output is 2.0Vp-p through EQ AMP.
- Built-in QIF AGC.
- ■Improve over modulation characteristics and Vcc ripple rejection.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range (Vcc) • • • • • • 4.75 to 5.25 V Rated Supply Voltage (Vcc) • • • • • 5.0 V

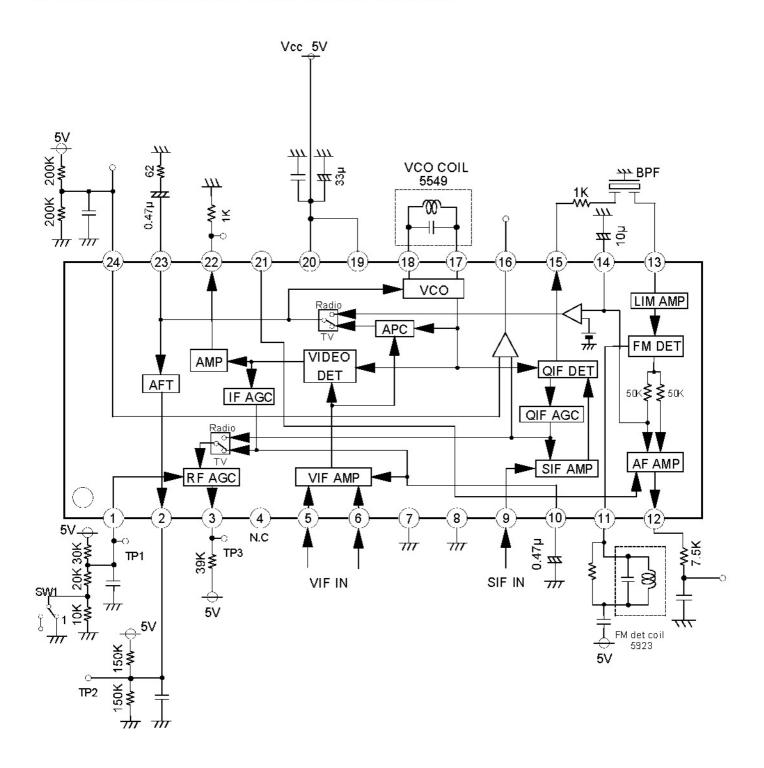
APPLICATION

TV,VTR





BLOCK DIAGRAM and PERIPHERAL CIRCUIT

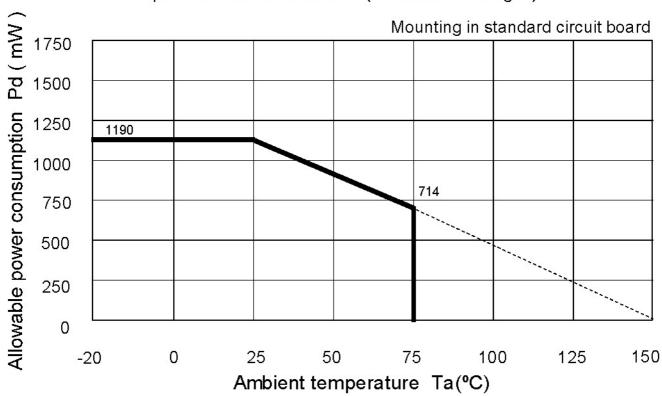


ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C, unless otherwise noted)

Parameter	Symbol	Ratings	Unit	Note
Supply Voltage 1	Vcc	6.0	>	
Power Consumption	Pd	1190	mW	
Operating Temperature	Topr	-20 to +75	°C	
Storage Temperature	Tstg	-40 to +150	°C	

Temperature Characteristics (maximum ratings)



PLL-SPLIT VIF/SIF

ELECTRICAL CHARACTERISTICS (Vcc=5V,Ta=25°C unless otherwise noted) TV Mode

<u> </u>	<u>Mode</u>		W	50. 10.		25	929			2.			12	
			Test	Test	Input	Input		a sure	ement condition	Limits				
NO	Parameter	Symbol		Point	Input Point	Input SG	V10	ver	switches set to position 1 unless otherwise noted	MIN	TYP	MAX	Unit	Note
1	Circuit Current 1 Vcc=5V	ICC1	1	Α	VIF IN	SG1	_	_	VCC=5V SW19=2	30	43	56	mΑ	
2	Video Output DC Voltage 1	V22	1	TP22A	_	_	0	_	SW10=2	3.2	3.5	3.8	٧	
3	Video Output Voltage 1	Vo det	1	TP22A	VIF IN	SG1	9 3	_		1.8	2.1	2.4	Vp-p	
4	Video S/N	Video S/N	1	TP22B	VIF IN	SG2	3 3		SW22=2	51	56	l,	dB	1
5	Video Band Width	BW	1	TP22A	VIF IN	SG3	Vari- able	_	SW10=2	6.0	7.0	-	MHz	2
6	Input Sensitiv ity	VIN MIN	1	TP22A	VIF IN	SG4		_			48	52	dΒμ	3
7	Maximum Allowable Input	VIN MAX	1	TP22A	VIF IN	SG5	2	_		101	105	-	dΒμ	4
8	AGC Control Range Input	GR	1	_	_	_	-	_		50	57	-	dB	5
9	IF AGC Voltage	V10	1	TP10	VIF IN	SG6		_		2.9	3.2	3.5	٧	
10	Maximum IF AGC Voltage	V10H	1	TP10	_	_	(s):	_		4.0	4.4	-	٧	
11	Minimum IF AGC Voltage	V10L	1	TP10	VIF IN	SG7	: — :	_		2.2	2.4	2.6	٧	
12	Maximum RF AGC Voltage	V3H	1	TP3	VIF IN	SG6	a—.	_		4.2	4.7	_	٧	
13	Minimum RF AGC Voltage	V3L	1	TP3	VIF IN	SG7		_		_	0.1	0.5	٧	
14	RF AGC Delay Point	V3	1	TP3	VIF IN	SG8	s s	_	SW1=1	89	92	95	dΒμ	6
15	Capture Range U	CL-U	1	TP22A	VIF IN	SG9	_	_		1.0	1.7	_	MHz	7
16	Capture Range L	CL-L	1	TP22A	VIF IN	SG9		_		1.8	2.4	_	MHz	8
17	Capture Range T	CL-T	_	_	_	_		_		3.1	4.1	_	MHz	9
18	AFT Sensitivity	μ	1	TP2	VIF IN	SG10	32. 31	_		23	35	70	mV kHz	10
19	AFT Maximum Voltage	V2H	1	TP2	VIF IN	SG10	:	_		3.85	4.15	-	٧	10
20	AFT Minimum Voltage	V2L	1	TP2	VIF IN	SG10	1-	_		_	0.7	1.2	٧	10



PLL-SPLIT VIF/SIF

				_			2000000		95 3355599					_
NO Devementar		Cambal	Test	Test	Input	Input	External		rement condition	L	imits		l In it	Note
NO	Parameter	Symbol	Circuit	Point	Point	SG		V14	1 unless otherwise noted	MIN	TYP	MAX	OIIIL	More
21	Inter Modulation	IM	1	TP22A	VIF IN	SG11	Vari- able	1	SW10=2	35	40	_	dB	11
22	Differential Gain	DG	1	TP22A	VIF IN	SG12	_	I		_	2	5	%	
23	Differential Phase	DP	1	TP22A	VIF IN	SG12	_	l		-	2	5	deg	
24	Sync. tip lev el	V22 SYNC	1	TP22A	VIF IN	SG2	_	l		0.85	1.15	1.45	>	
25	VIF Input Resistor	RINV	2	TP5	_	_		_			1.2		kΩ	
26	VIF Input capacitance	CINV	2	TP5	_	g -	_				5		pF	



PLL-SPLIT VIF/SIF

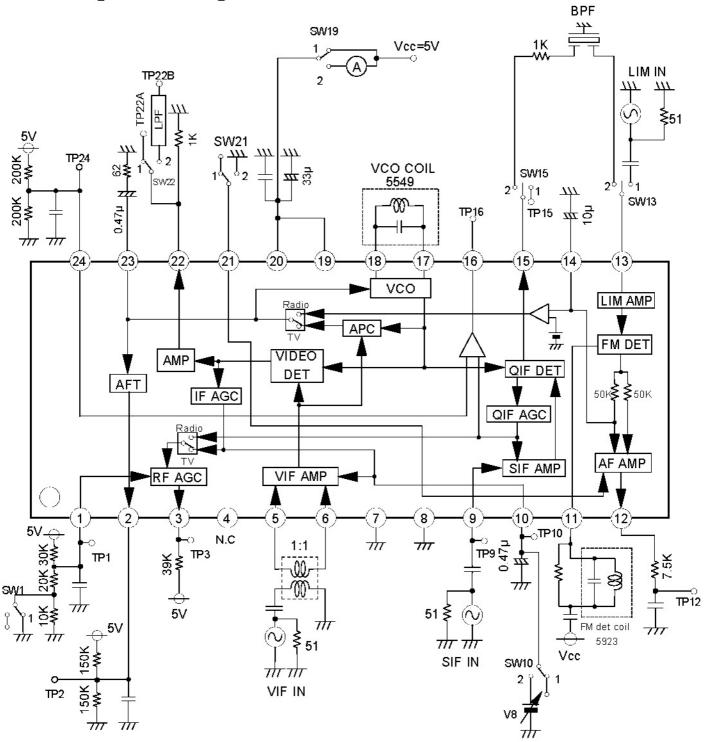
			Test	Test	Input	Input	Exte	rnal	rement condition	Limits				
NO	Parameter	Symbol	Circuit	Point	Point	SG	v10		position 1 unless otherwise noted	MIN	TYP	MAX	Unit	Note
27	QIF Output Voltage 1	QIF1	1	TP15	VIF IN SIF IN	SG2 SG13	_	_		90	96	102	dΒμ	
28	QIF Output Voltage 2	QIF2	1	TP15	VIF IN SIF IN	SG2 SG14	_	_		90	96	102	dΒμ	
29	AF Output (4.5MHz)	VoAF1	1	TP12	LIM IN	SG15				300	430	615	mVrms	
30	AFOutput Distortion (4.5MHz)	THD AF1	1	TP12	LIM IN	SG15	_	_		_	0.2	1.0	%	
31	Limiting Sensitivity (4.5MHz)	LIM1	1	TP12	LIM IN	SG16	-	_		_	55	60	dΒμ	12
32	AM Rejection (4.5MHz)	AMR 1	1	TP12	LIM IN	SG17	_	_		40	46	_	dB	13
33	AF S/N (4.5MHz)	AF S/N1	1	TP12	LIM IN	SG19	_	_		46	53	-	dB	14
34	SIF Input Resistor	RINS	2	TP9	_	_	_	_		—	1.5	_	kΩ	
35	SIF Input capacitance	CINS	2	TP9	_	_	<u>-</u>	_		1-0	4	_	pF	

FM Radio Mode

1 171	Madio Mode													
NO	O Parameter Symbol Test To		Test	Test Input		Measur External power		switches set to	Limits			Linit	Note	
NO	Farameter	Cyrriba	Circuit	Point	Point	SG	V10	V14	position 1 unless otherwise noted	MIN	TYP	MAX		1010
32	SIF detection out High Voltage	V16H	1	TP16	_	_	0	_	SW10=2	4.0	4.8	_	٧	
33	SIF detection out Low Voltage	V16L	1	TP16	SIF IN	SG20	0		SW10=2	1	0.2	1.0	V	
34	SIF detection Threshold Point	TSIF	1	TP16	SIF IN	SG21	0	ı	SW10=2	85	90	95	dΒμ	15
35	RF AGC Delay Point	V3F	1	TP3	SIF IN	SG21	0	l,	SW1=2 SW10=2	85	90	95	dΒμ	16
36	AF Output	VoF	1	TP12	LIM IN	SG22	0	ı	SW10=2	400	560	800	mVrms	
37	AF Output Distortion	THD F	1	TP12	LIM IN	SG22	0		SW10=2	_	0.2	1.0	%	
38	AF S/N	S/N F	1	TP12	LIM IN	SG19	0	_	SW10=2	55	62	_	dB	17

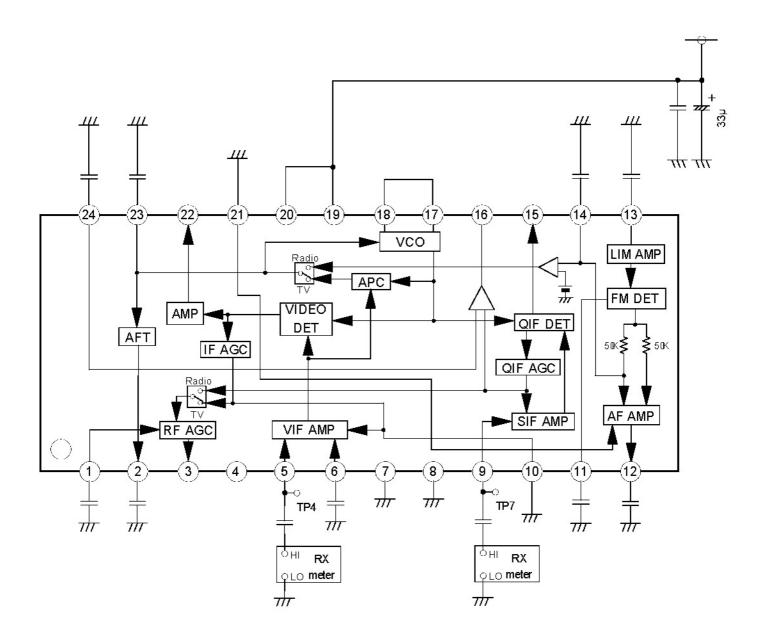


Measuring Circuit Diagram1



- * All capacitor is 0.01µF, unless otherwise noted.
- * The Measuring Circuit 1 is Mitsubishi standard evaluation fixture.

Measuring Circuit Diagram2



* All capacitor is 0.01 µF, unless otherwise noted.

PLL-SPLIT VIF/SIF

INPUT SIGNAL

SG	50ohm Termination
1	fo=58.75MHz AM 20 KHz 77.8 % 90 dBµ
2	fo=58.75MHz 90 dBµ Cw
3	f1=58.75MHz 90 dBµ Cw f2=Frequency Variable 70 dBµ Cw } Mixed Signal
4	fo=58.75MHz AM 20 KHz 77.8% Level Variable
5	fo=58.75MHz AM 20 KHz 14.0% Level Variable
6	fo=58.75 MHz 80 dBµ Cw
7	fo=58.75 MHz 110 dBµ Cw
8	fo=58.75 MHz Level Variable Cw
9	fo=Frequency Variable AM 20 KHz 77.8 % 90 dBµ
10	fo=FrequencyVariable 90 dBµ Cw
11	f1=58.75MHz 90 dBµ Cw f2=55.17MHz 80 dBµ Cw f3=54.25MHz 80 dBµ Cw
12	fo=58.75MHz 87.5 % TV modulation Ten-step waveform Sync Tip Level 90 dBµ
13	fo=54.25MHz 95 dBµ Cw
14	fo=54.25MHz 75 dBµ Cw
15	fo=4.5 MHz 90 dBµ FM 400 Hz ±25 KHz dev
16	fo=4.5 MHz Level Variable FM 400Hz ±25KHz dev
17	fo=4.5 MHz 100 dBµ AM 400 Hz 30 %
18	fo=4.5 MHz Level Variable Cw
19	fo=4.5 MHz 90 dBµ Cw
20	fo=54.25 MHz 90 dBµ Cw
21	fo=54.25 MHz Level Variable Cw
22	fo=4.5 MHz 90 dBµ FM 400 Hz ±75 KHz dev



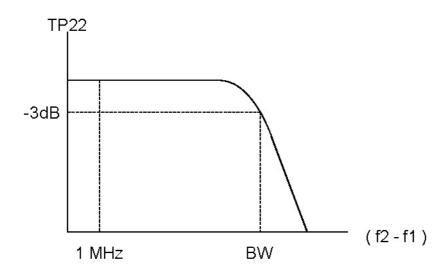
Notes

1. Video S/N

Input SG2 into VIF IN and measure the video out(Pin 22) noise in r.m.s at TP22-B through a 5MHz (-3dB) L.P.F.

$$S/N=20 \log \left(\frac{0.7 \times Vo \det}{NOISE} \right)$$
 (dB)

- 2. Video Band width: BW
 - Measure the 1MHz component level of Video output TP22A with a spectrum analyzer when SG3(f2=57.75MHz) is input into VF IN. At that time, measure the voltage at TP10 with SW10, set to position 2, and then fix V10 at that voltage.
 - 2. Reduce f2 and measure the value of (f2-f1) when the (f2-f1) component level reaches -3dB from the 1MHz component level as shown below.



3. Input Sensitivity: VIN MIN

Input SG4 (Vi=90dBµ) into VF IN, and then gradually reduce Vi and measure the input level when the 20KHz component of Video output TP22A reaches -3dB from Vo det level.

- 4. Maximum Allowable Input: VIN MAX
 - 1. Input SG5 (Vi=90dBµ) into VIF IN , and measure the level of the 20KHz component of Video output.
 - 2. Gradually increase the Vi of SG and measure the input level when the output reaches -3dB.



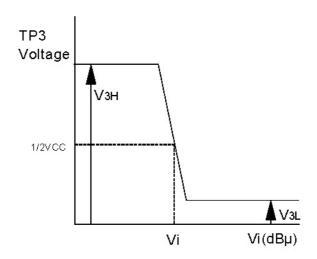
PLL-SPLIT VIF/SIF

5. AGC Control Range: GR

GR = VIN MAX - VIN M IN (dB)

6. RF AGC Operating Voltage: V3

Input SG8 into VIF IN and gradually reduce Vi and then measure the input level when RF AGC output TP3 reaches 1/2 VCC, as shown below.



- 7. Capture range: CL U
 - 1. Increase the frequency of SG9 until the VCO is out of locked-oscillation.
 - 2. Decrease the frequency of SG9 and measure the frequency fU when the VCO locks.

$$CL - U = fU - 58.75$$
 (MHz)

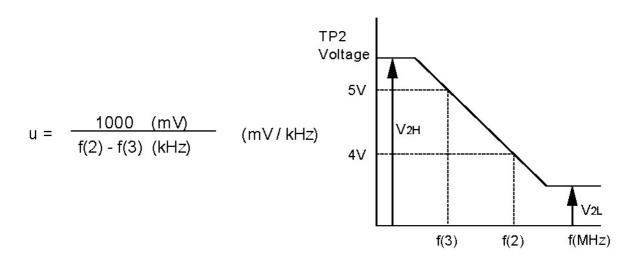
- 8. Capture range: CL L
 - 1. Decrease the frequency of SG9 until the VCO is out of locked-oscillation.
 - 2. Increase the frequency of SG9 and measure the frequency fL when the VCO locks.

$$CL - L = 58.75 - fL$$
 (MHz)

9. Capture range: CL - T

$$CL - T = CL - U + CL - L$$
 (MHz)

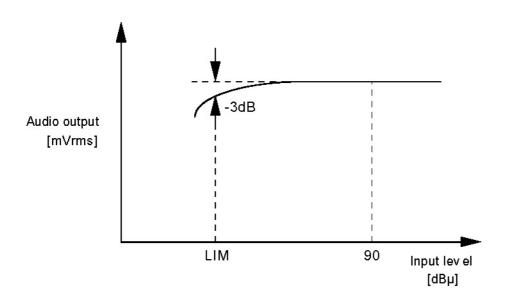
- 10. AFT sensitivity u, Maximum AFT voltage V2H, Minimum AFT voltage V2L
 - 1. Input SG10 into VIF IN, and set the frequency of SG10 so that the voltage of AFT output TP2 is 3V. This frequency is named f(3).
 - 2. Set the frequency of SG10 so that the AFT output voltage is 2V. This frequency is named f(2)
 - 3. IN the graph, maximum and minimum DC voltage is V2H and V2L, respectively.



- 11. Inter modulation: IM
 - 1. Input SG11 into VIF IN, and measure EQ output TP22A with an oscilloscope.
 - 2. Adjust AGC filter voltage V10 so that the minimum DC level of the output waveform is 1.0V.
 - 3. At this time, measure TP22A with a spectrum analyzer. The intermodulation is defined as a difference between 0.92MHz and 3.58 MHz frequency components.



- 12. Limiting Sensitivity: LIM
 - 1. Input SG16 (Vi=90dBµ) into SIF IN, and measure the 400Hz component level of AF output TP12.
 - 2. Lower the input level of SG16, and measure the level of SG16 when the VoAF level reaches -3dB.



- 13. AM Rejection: AMR
 - 1. Input SG17 into SIF IN, and measure the output level of AF OUT (TP12). This level is named VAM.

2. AMR is;

$$AMR = 20log \left(\frac{VoAF (mVr.m.s)}{VAM (mVr.m.s)} \right)$$
(dB)

- 14. AF S/N: AF S/N
 - Input SG19 into SIF IN, and measure the output noise level of AF OUT (TP12).

This level is named VN.

2. S/N is; $S/N = 20 \log \left(\frac{VoAF (mVr.m.s)}{VN (mVr.m.s)} \right)$ (dB)

15. SIF detection threshold level TSIF

SG21 is applied to SIF IN and the input amplitude is swept. Then, the level of SG21, TSIF, is measured at the time when the DC voltage of SIF CARRIER DET OUT (TP16) has just begun to vary.

16. RF AGC voltage V3F

SG21 is applied to SIF IN and the input amplitude is swept. Then, the level of SG21, V3F, is measured at the time when the DC voltage of RF AGC OUT (TP3) has just reached 1/2Vcc.

17. AF S/ N (S/N F)

- 1. SG19 is applied to SIF IN and the output noise of AUDIO OUT (TP12) is measured. The measured noise is named VNF.
- 2. S/N F is,

S/N F =
$$20\log\left(\frac{\text{VoF [mVr.m.s]}}{\text{VNF [mVr.m.s]}}\right)$$
 [dB]



VCO coil adjustment methods

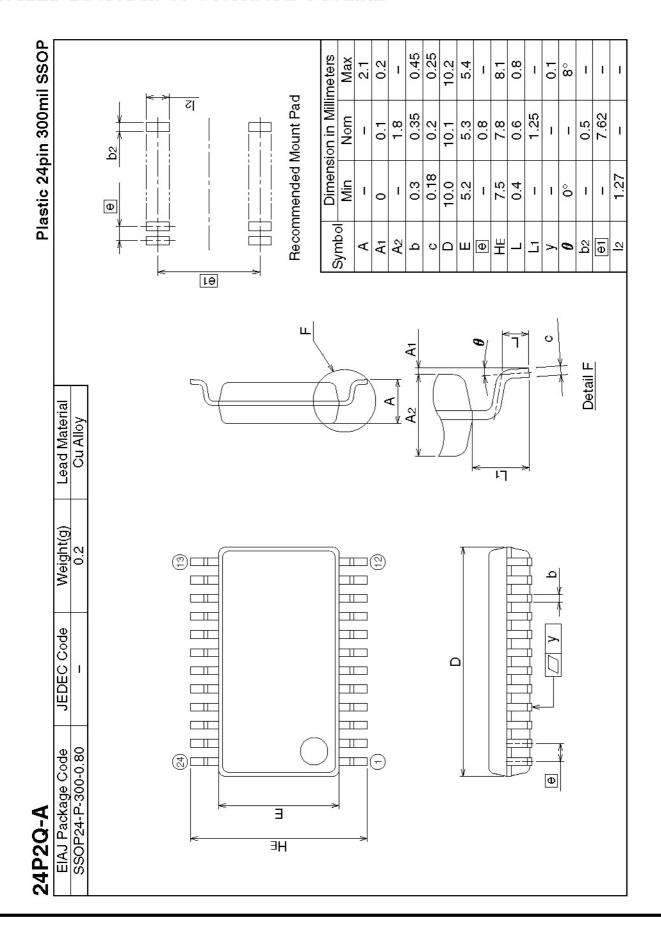
- 1. Input SG2 (fo=58.75MHz, 90dBµ CW) into VIF IN.
- 2. And adjust the coil until the voltage of AFT output reaches about Vcc/2=2.5V.

FM DET coil adjustment methods

- 1. The first thing, adjust the VCO coil.
- 2. Input SG13 (fo=54.25MHz, 95dBµ CW) into SIF IN.
- 3. Change the switch of SW13 and SW15 to 2 position.
- 4. Change to FM RADIO mode (V10=0V).
- 5. Adjust the DC voltage of AFT OUT to Vcc/2 and SIF det OUT to Low (under 1V).



DETAILED DIAGRAM OF PACKAGE OUTLINE



PLL-SPLIT VIF/SIF

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