To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M52766FP

PLL SPLIT VIF / SIF

DESCRIPTION

The M52766FP is a semiconducttor IC with PLL system of VIF/ SIF.

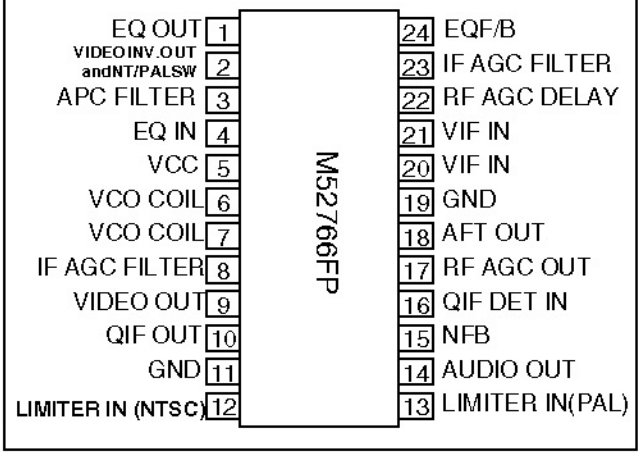
The circuit includes video UF amplifier,PLL video detector,IFAGC,RFAGC,VCO,AFT,LOCK DET,EQ,REG,QIFamplifier,QIF detector,QIF AGC,LIM,FM detector function.

The circuit realize no abjustment SIF,nothing coil AFT.

FEATURES

- Dynamic AGC realizes high speed AGC with double filtre.
- The M52766FP can correspond to 2tipe sound career,from change on standard board,with sound LIM input have 2pins (12,13pin).
- Sound FM detection can correspond to wide SIF signal,with PLL system and no abjustment.
- The N52766FP correspond to PLL split system and intercareer system.
- AFT coil is necessary.
- AFT mute is not used.
- The M52766FP optimum for VTR and color TV,with video output-pin,because this IC has a built in EQ amplifier.
- VCC correspond to 5V,be main strem of tuner in future.
- Flat package is 24-pin SSOP of mini flat (0.8mm pich), suitable for space saving.

PIN CONFIGURATION (TOP VIEW)



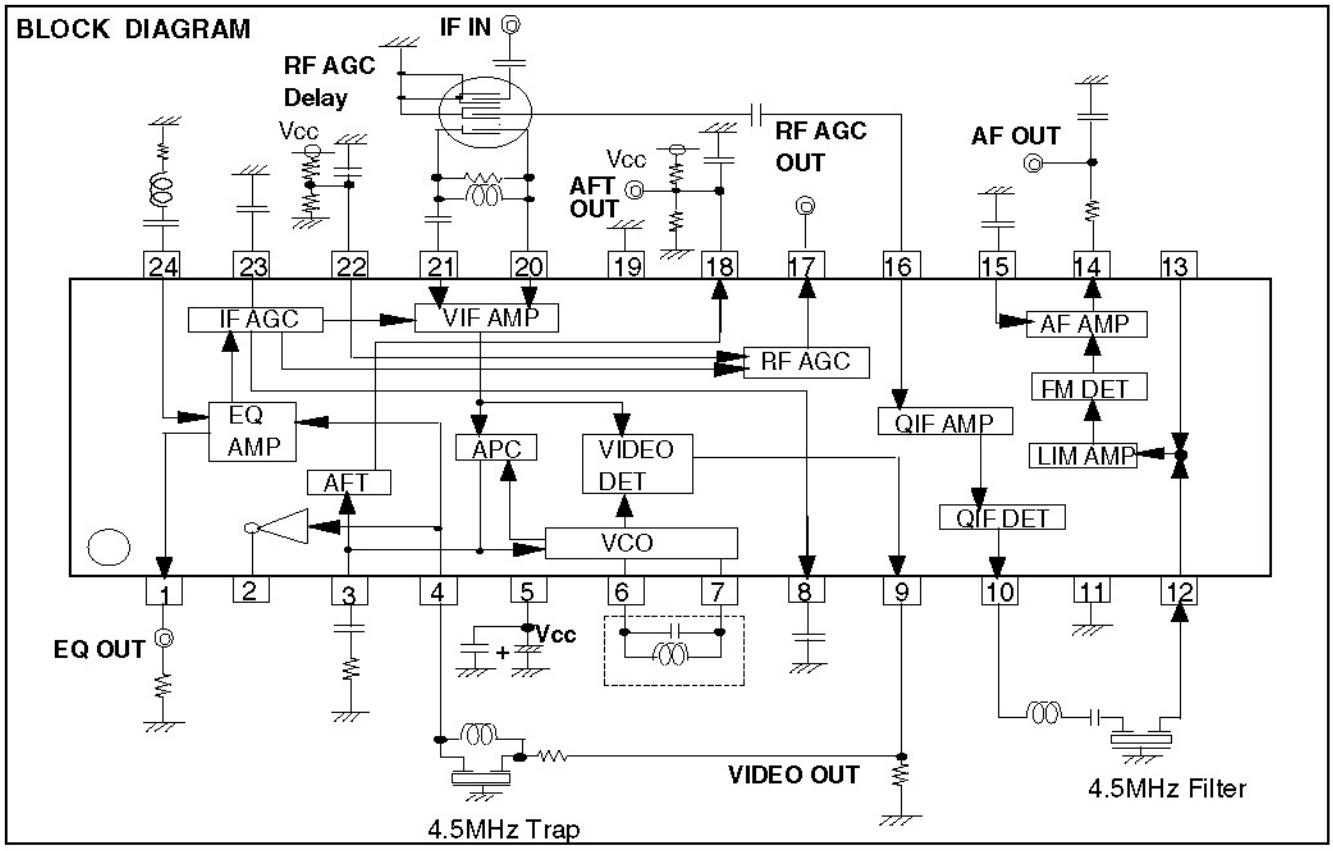
APPLICATION

TV sets, VTR tuners.

RECOMMEND OPERATING CONDITION

Supply voltage range • • • • 5.0 ± 0.25V
Recommended supply voltage • • • 5.0V

BLOCK DIAGRAM

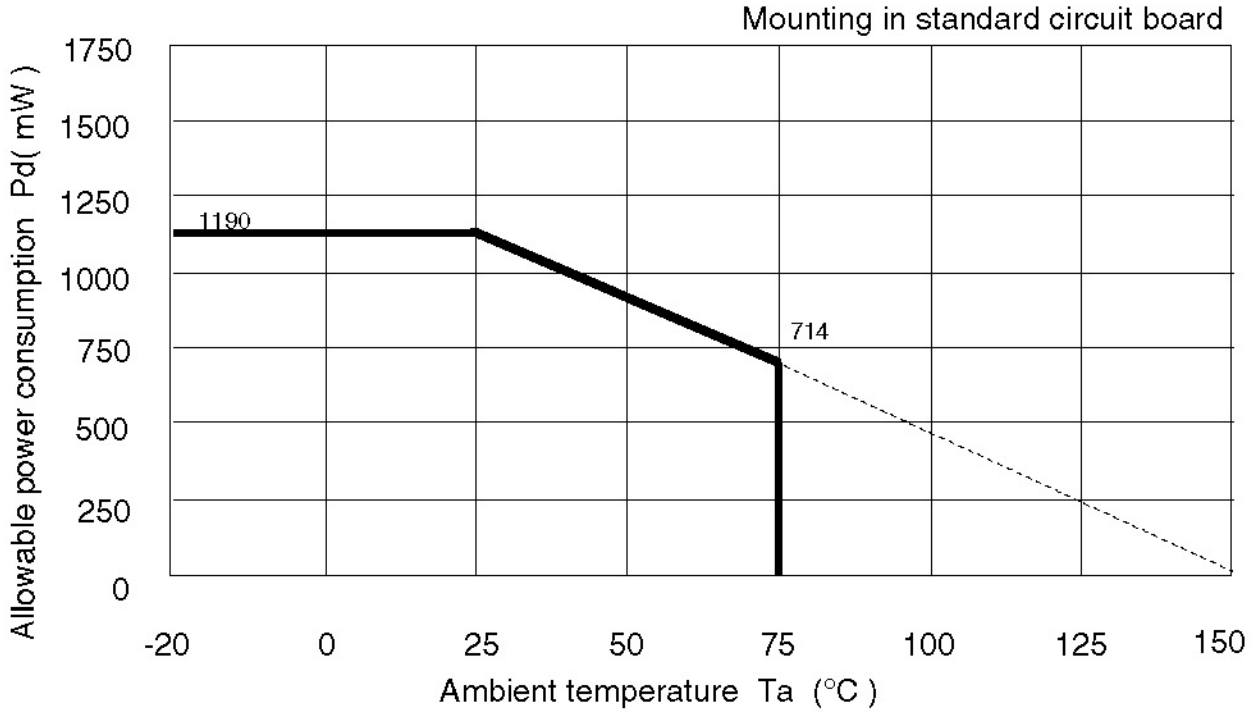


Absolute maximum ratings (Ta = 25°C, unless otherwise noted)

Parameter	Symbol	Ratings	Unit	Note
Supply Voltage 1	Vcc	6.0	V	
Power Consumption	Pd	1524	mW	
Operating Temperature	Topr	-20 to +75	°C	
Storage Temperature	Tstg	-40 to +150	°C	
Surge voltage resistance	Surge	±200	V	surge protection capacitance 200pF resistance 0Ω

★ There is not all pins problem about surge, but the case of use pay attention about latch up because the ninth pin is weak a few.

Temperature Characteristics (maximum ratings)



Recommended Operating Condition (Ta = 25°C, unless otherwise noted)

Supply Voltage Range (Vcc) ••••• 4.75 to 5.25 V

Rated Supply Voltage (Vcc) •••••• 5.0 V

Electrical Characteristics (Vcc=5V, Ta=25°C unless otherwise noted)

VIF Section

No.	Parameter	Symbol	Test Circuit	Test Point	Input Point	Input SG	Measurement switches set to position 1 unless otherwise noted	Limits MIN	Limits TYP	Limits MAX	Unit	Note
1	Circuit Current 1 Vcc=5V	Icc1	1	A	–	–	SW5=2	40	56	72	mA	
2	Video Output DC Voltage 1	V1	1	TP1A	–	–	SW23=2 V23=0V	3.1	3.5	3.9	V	
3	Video Output Voltage 9	Vo det9	1	TP9	VIF IN	SG1		0.85	1.1	1.35	Vp-p	
4	Video Output Voltage 1	Vo det	1	TP1A	VIF IN	SG1		1.77	2.1	2.43	Vp-p	
5	Video S/N	Video S/N	1	TP1B	VIF IN	SG2	SW1=2	51	56	–	dB	1
6	Video Band Width	BW	1	TP1A	VIF IN	SG3	SW23=2 V23=Variable	5.0	7.0	–	MHz	2
7	Input Sensitivity	VIN MIN	1	TP1A	VIF IN	SG4		–	48	52	dBμ	3
8	Maximum Allowable Input	VIN MAX	1	TP1A	VIF IN	SG5		101	105	–	dBμ	4
9	AGC Control Range Input	GR	–	–	–	–		50	57	–	dB	5
10	IF AGC Voltage 1	V23	1	TP23	VIF IN	SG6		2.47	2.75	3.03	V	
11	Maximum IF AGC Voltage 1	V23H	1	TP23	–	–		4.35	4.75	–	V	
12	Minimum IF AGC Voltage 1	V23L	1	TP23	VIF IN	SG7		2.06	2.25	2.45	V	
13	Maximum RF AGC Voltage	V17H	1	TP17	VIF IN	SG6		4.13	4.75	–	V	
14	Minimum RF AGC Voltage	V17L	1	TP17	VIF IN	SG7		–	0.1	0.5	V	
15	RF AGC Delay Point	V17	1	TP17	VIF IN	SG8		80	83	86	dBμ	6
16	Capture Range U	CL-U	1	TP1A	VIF IN	SG9		0.9	1.5	–	MHz	7
17	Capture Range L	CL-L	1	TP1A	VIF IN	SG9		1.3	1.8	–	MHz	8
18	Capture Range T	CL-T	1	–	–	–		2.5	3.3	–	MHz	9

No.	Parameter	Symbol	Test Circuit	Test Point	Input Point	Input SG	Measurement switches set to position 1 unless otherwise noted	Limits MIN	Limits TYP	Limits MAX	Unit	Note
19	AFT Sensitivity	μ	1	TP18	VIF IN	SG10		20	30	70	mV/kHz	10
20	AFT Maximum Voltage	V18H	1	TP18	VIF IN	SG10		3.85	4.15	–	V	10
21	AFT Minimum Voltage	V18L	1	TP18	VIF IN	SG10		–	0.7	1.2	V	10
22	AFT defeat	AFT def 1	1	TP18	VIF IN	–		2.2	2.5	2.8	V	
23	Inter Modulation	IM	1	TP1A	VIF IN	SG11	SW23=2 V23=Variable	33	40	–	dB	11
24	Differential Gain	DG	1	TP1A	VIF IN	SG12		–	2	5	%	
25	Differential Phase	DP	1	TP1A	VIF IN	SG12		–	2	5	deg	
26	Sync. tip level	V9 SYNC	1	TP1A	VIF IN	SG2		0.95	1.35	1.75	V	
27	VIF Input Resistor	RINV	2	TP20				–	1.2	–	kΩ	
28	VIF Input capacitance	CINV	2	TP20				–	5	–	pF	
29	IF AGC Voltage 2	V8	1	TP8	VIF IN	SG6		2.40	2.75	3.11	V	
30	Maximum IF AGC Voltage 2	V8	1	TP8	VIF IN	–		3.80	4.25	–	V	
31	Minimum IF AGC Voltage 2	V8	1	TP8	VIF IN	SG7		1.95	2.25	2.55	V	
32	Video Inversion Output Voltage	Vo det INV	1	TP2	VIF IN	SG1		0.25	0.5	0.75	Vp-p	

Control Section

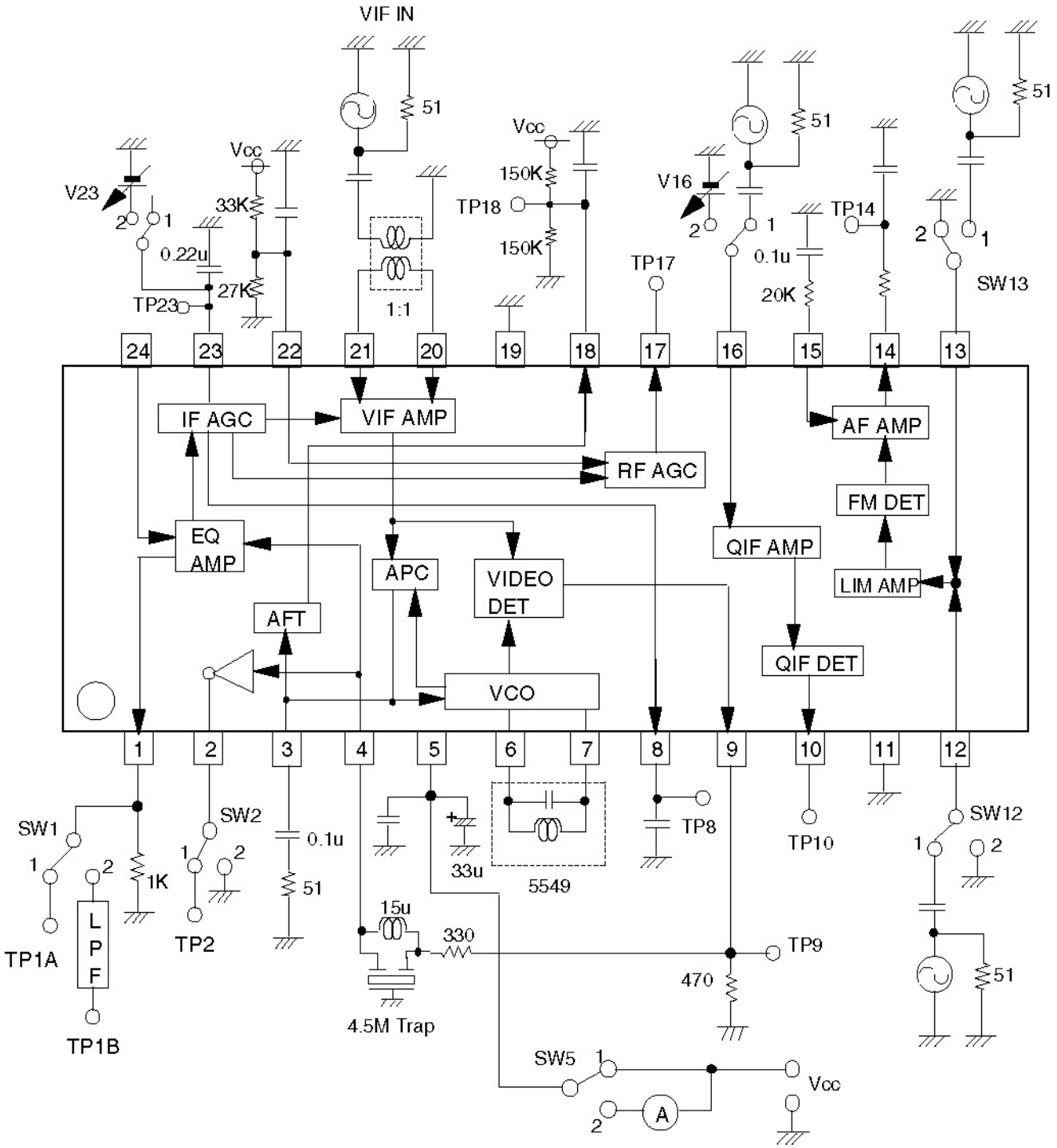
No.	Parameter	Symbol	Test Circuit	Test Point	Input Point	Input SG	Measurement switches set to position 1 unless otherwise noted	Limits MIN	Limits TYP	Limits MAX	Unit	Note
33	QIF Control	C_{QIF}	1	TP16	–	–	SW16=2	–	0.7	1.0	V	15

Electrical Characteristics (Vcc=5V,Ta=25°C unless otherwise noted)

SIF Section

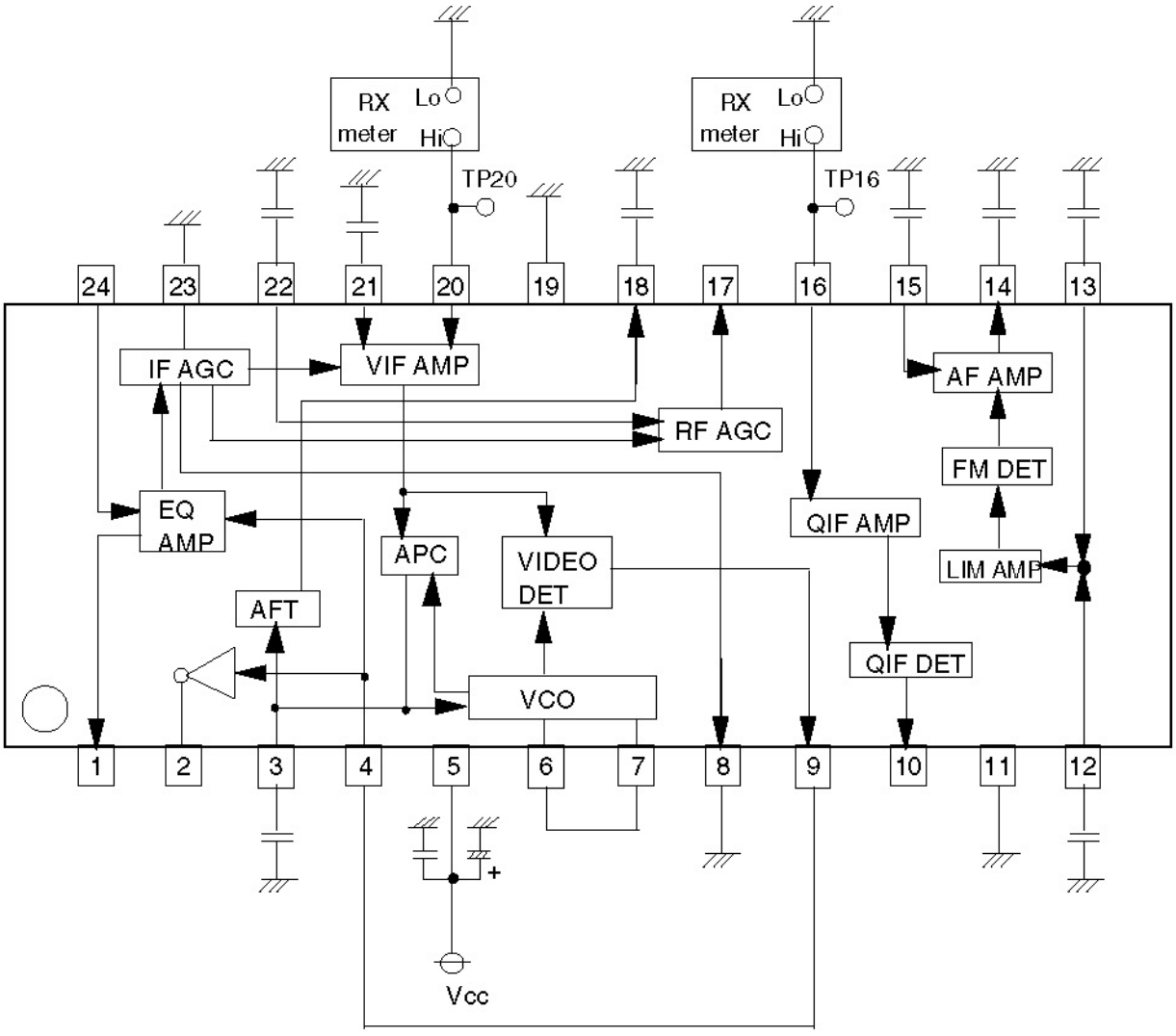
No.	Parameter	Symbol	Test Circuit	Test Point	Input Point	Input SG	Measurement switches set to position 1 unless otherwise noted	Limits MIN	Limits TYP	Limits MAX	Unit	Note
34	QIF Output Voltage 1	QIF1	1	TP10	VIF IN QIF IN	SG2 SG13		104	110	116	dBµ	
35	QIF Output Voltage 2	QIF2	1	TP10	VIF IN QIF IN	SG2 SG14		94	100	106	dBµ	
36	SIF Detection Output	Vos	1	TP10	VIF IN	SG15	SW16=2 V16=0V	94	100	106	dBµ	
37	AF Output DC Voltage	V1	1	TP14	SIF IN	SG19		1.5	2.1	2.7	V	
38	AF Output (4.5MHz)	VoAF 1	1	TP14	SIF IN	SG16	SW13=2	571	800	1142	mVrms	
39	AF Output (5.5MHz)	VoAF 2	1	TP14	SIF IN	SG21	SW2=2 SW12=2	521	730	1043	mVrms	
40	AFOutput Distortion (4.5MHz)	THD AF 1	1	TP14	SIF IN	SG16	SW13=2	–	0.8	1.2	%	
41	AFOutput Distortion (5.5MHz)	THD AF 2	1	TP14	SIF IN	SG21	SW2=2 SW12=2	–	0.6	1.0	%	
42	Limiting Sensitivity (4.5MHz)	LIM 1	1	TP14	SIF IN	SG17	SW13=2	–	42	55	dBµ	12
43	Limiting Sensitivity (5.5MHz)	LIM 2	1	TP14	SIF IN	SG22	SW2=2 SW12=2	–	42	55	dBµ	12
44	AM Rejection (4.5MHz)	AMR 1	1	TP14	SIF IN	SG18	SW13=2	53	62	–	dB	13
45	AM Rejection (5.5MHz)	AMR 2	1	TP14	SIF IN	SG23	SW2=2 SW12=2	54	64	–	dB	13
46	AF S/N (4.5MHz)	AF S/N 1	1	TP14	SIF IN	SG19	SW13=2	53	62	–	dB	14
47	AF S/N (5.5MHz)	AF S/N 2	1	TP14	SIF IN	SG24	SW2=2 SW12=2	54	64	–	dB	14
48	SIF Input Resistor	RINS	2	TP16				–	0.7	–	kΩ	
49	SIF Input Capacitance	CINS	2	TP16				–	4	–	pF	

Measuring Circuit Diagram 1



* All capacitor is 0.01µF, unless otherwise noted.
* The Measuring Circuit 1 is Mitsubishi standard evaluation fixture.

Measuring Circuit Diagram 2



* All capacitor is 0.01µF, unless otherwise noted.

INPUT SIGNAL

SG	50 Ω Termination
1	f0 = 58.75 MHz AM 20 KHz 77.8 % 90 dBμ
2	f0 = 58.75 MHz 90 dBμ Cw
3	f1 = 58.75 MHz 90 dBμ Cw f2 = Frequency Variable 70 dB Cw } Mixed Signal
4	f0 = 58.75 MHz AM 20 KHz 77.8% Level Variable
5	f0 = 58.75 MHz AM 20 KHz 14.0% Level Variable
6	f0= 58.75 MHz 80 dBμ Cw
7	f0 = 58.75 MHz 110 dBμ Cw
8	f0 = 58.75 MHz Cw Level Variable
9	f0 = Frequency Variable AM 20 KHz 77.8 % 90 dBμ
10	f0 = Frequency Variable 90 dBμ Cw
11	f1 = 58.75 MHz 90 dBμ Cw f2 = 55.17 MHz 80 dBμ Cw f3 = 54.25 MHz 80 dBμ Cw } Mixed Signal
12	f0 = 58.75 MHz 87.5 % TV modulation Ten-step waveform Sync Tip Level 90 dBμ
13	f1 = 54.25 MHz 95 dBμ Cw
14	f1 = 54.25 MHz 75 dBμ Cw
15	f1 = 58.75 MHz 90 dBμ Cw f2 = 54.25 MHz 70 dBμ Cw } Mixed Signal
16	f0 = 4.5 MHz 90 dBμ FM 400 Hz ±25 KHzdev
17	f0 = 4.5 MHz Level Variable FM 400Hz ±25KHzdev
18	f0 = 4.5 MHz 90 dBμ AM 400 Hz 30 %
19	f0 = 4.5 MHz 90 dBμ Cw
20	f0 = 4.5 MHz Level Variable Cw
21	f0 = 5.5 MHz 90 dBμ FM 400 Hz ±50 KHzdev
22	f0 = 5.5 MHz Level Variable FM 400Hz ±50KHzdev
23	f0 = 5.5 MHz 90 dBμ AM 400 Hz 30 %
24	f0 = 5.5 MHz 90 dBμ Cw
25	f0 = 5.5 MHz Level Variable Cw

Notes

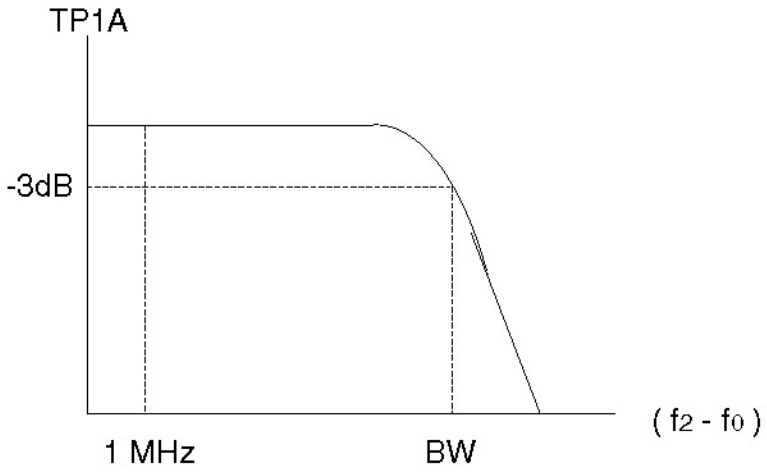
1. Video S/N

Input SG2 into VIF IN and measure the video out(Pin 1) noise in r.m.s at TP1B through a 5MHz (-3dB) L.P.F.

$$S/N=20 \log \left(\frac{0.7 \times Vo\ det}{NOISE} \right) \quad [dB]$$

2. Video Band Width: BW

1. Measure the 1MHz component level of Video output TP1A with a spectrum analyzer when SG3(f_2=57.75MHz) is input into VIF IN. At that time, measure the voltage at TP23 with SW23, set to position 2, and then fix V23 at that voltage.
2. Reduce f_2 and measure the value of (f_2-f_0) when the (f_2-f_0) component level reaches -3dB from the 1MHz component level as shown below.



3. Input Sensitivity: VIN MIN

Input SG4 (Vi=90dBμ) into VIF IN , and then gradually reduce Vi and measure the input level when the 20KHz component of Video output TP1A reaches -3dB from Vo det level.

4. Maximum Allowable Input: VIN MAX

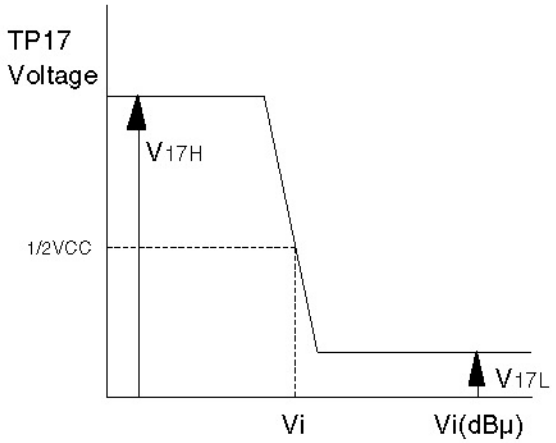
1. Input SG5 (Vi=90dBμ) into VIF IN , and measure the level of the 20KHz component of Video output.
2. Gradually increase the Vi of SG and measure the input level when the output reaches -3dB.

5. AGC Control Range: GR

GR = VIN MAX - VIN MIN [dB]

6. RF AGC Operating Voltage: V17

Input SG8 into VIF IN and gradually reduce Vi and then measure the input level when RF AGC output TP17 reaches 1/2 VCC, as shown below.



7. Capture range: CL - U

1. Increase the frequency of SG9 until the VCO is out of locked-oscillation.
2. Decrease the frequency of SG9 and measure the frequency fU when the VCO locks.

CL - U = fU - 58.75 [MHz]

8. Capture range: CL - L

1. Decrease the frequency of SG9 until the VCO is out of locked-oscillation.
2. Increase the frequency of SG9 and measure the frequency fL when the VCO locks.

CL - L = 58.75 - fL [MHz]

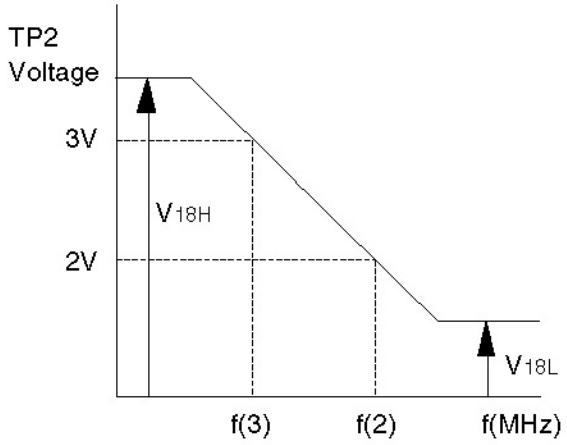
9. Capture range: CL - T

CL - T = CL - U + CL - L [MHz]

10. AFT sensitivity μ, Maximum AFT voltage V_{18H} , Minimum AFT voltage V_{18L}

1. Input SG10 into VIF IN , and set the frequency of SG10 so that the voltage of AFT output TP18 is 3[V] . This frequency is named f(3).
2. Set the frequency of SG10 so that the AFT output voltage is 2[V]. This frequency is named f(2)
3. IN the graph, maximum and minimum DC voltage are V_{18H} and V_{18L}, respectively.

$$\mu = \frac{1000 \quad [mV]}{f(2) - f(3) \quad [kHz]} \quad [mV/kHz]$$

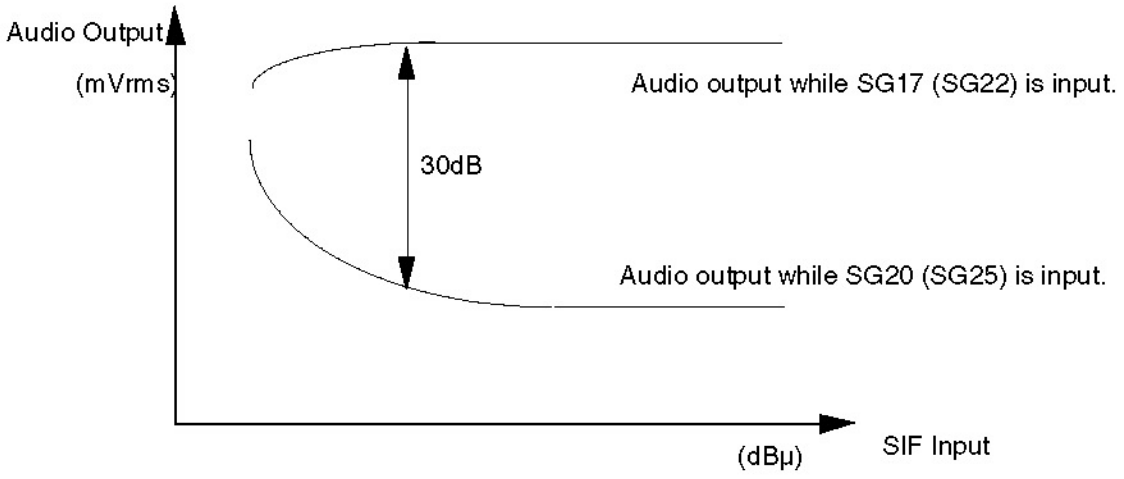


11. Inter modulation: IM

1. Input SG11 into VIF IN, and measure video output TP9 with an oscilloscope.
2. Adjust AGC filter voltage V23 so that the minimum DC level of the output waveform is 1.0V.
3. At this time, measure TP9 with a spectrum analyzer . The inter modulation is defined as a difference between 0.92MHz and 3.58 MHz frequency components.

12. Limiting Sensitivity: LIM

1. Input SG17 (SG22) into SIF input, and measure the 400Hz component level of AF output TP14.
2. Input SG20 (SG25) into SIF input, and measure the 400Hz component level of AF output TP14 .
3. The input limiting sensitivity is defined as the input level when a difference between each 400Hz components of audio output (TP14) is 30dB, as shown below.



13. AM Rejection: AMR

1. Input SG18 (SG23) into SIF IN ,and measure the output level of Audio output (TP12). This level is named VAM.
2. AMR is;

$$AMR = 20\log\left(\frac{VoAF\ (mVr.m.s)}{VAM\ (mVr.m.s)}\right) \quad [dB]$$

14. AF S/N: AF S/N

1. Input SG19 (SG24) into SIF input ,and measure the output noise level of Audio output (TP14). This level is named VN.
2. S/N is;

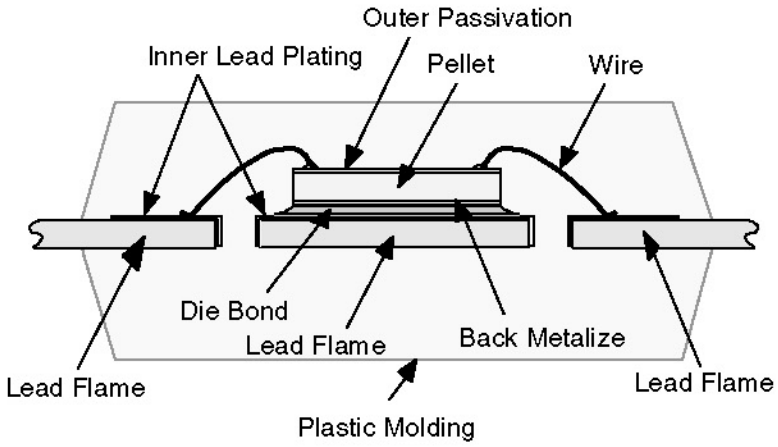
$$S/N = 20\log\left(\frac{VoAF\ (mVr.m.s)}{VN\ (mVr.m.s)}\right) \quad [dB]$$

15. QIF Control : C_{QIF}

Lower the voltage of V16 ,and measure the voltage of V16 when DC voltage of TP10 begins to change.

Structure of package (Cross section)

Structure



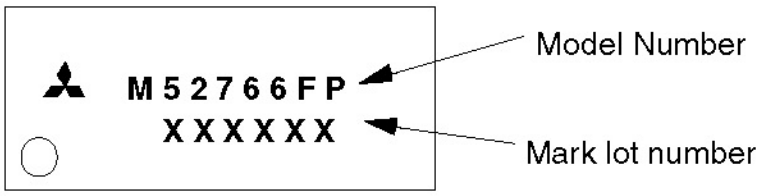
Matrrial

Mold resin	: Epoxy resin
Internal lead	: Au wire(ϕ 25µm)
External lead plating	: Solder plating
Lead frame	: Copper alloy
Passivation	: Nitride coat

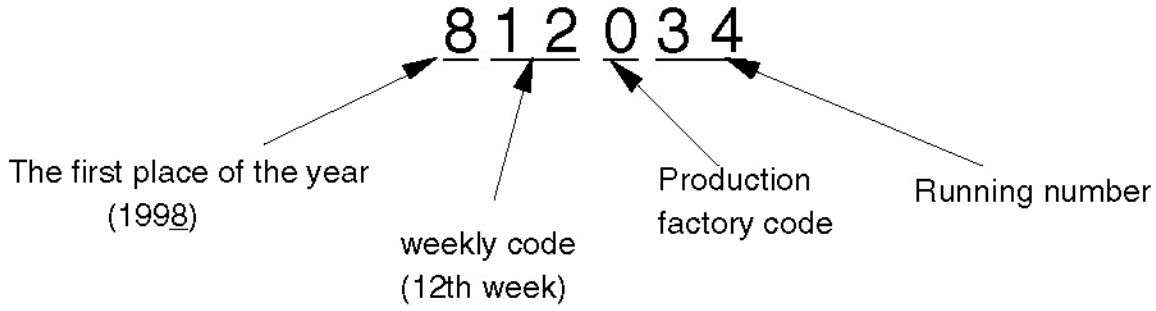
Manufacturing place (Wafer process,assembly,final inspection)

Mitsubishi Electric Corporation Fukuoka Semiconductor Factory

Indications



Lot number constitution



Package specification

IC package : 24P2Q

In case of tube shipping

Tube : 50 pieces / tube
Interior box : 5000 pieces / interior box
(100 tubes / interior box)
Exterior box : 20000 pieces / exterior box
(4 interior boxes / exterior box)

In case of emboss tape shipping
(The direction of T1)

Reel : 2000 pieces / reel
Interior box : 1 reel / interior
Exterior box : 10000 pieces / exterior box
(5 interior boxes / exterior box)

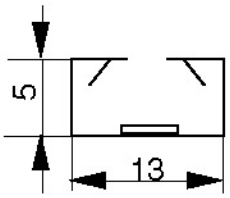
The packing method in case of tube shipping

1. Container tube

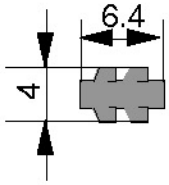
1.1 Container tube size

(1) IC tube MP016PC

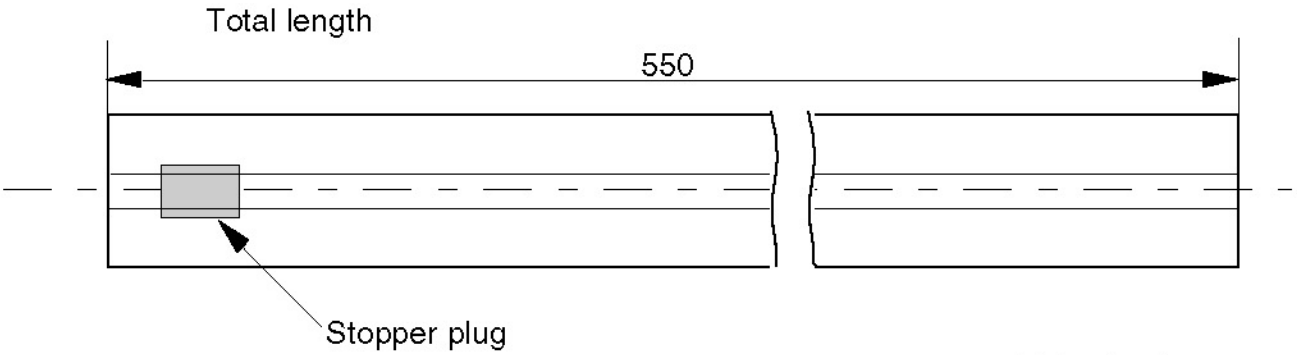
A cross section



(2) Stopper plug



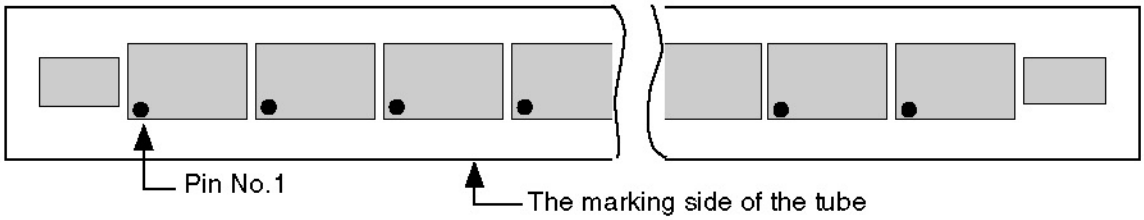
Width : 5.5
Color : Gray



Unit : (mm)

1.2 Packing method

(1) The packing direction of the device.
(Facing the Pin No.1 with the marking side as shown below.)



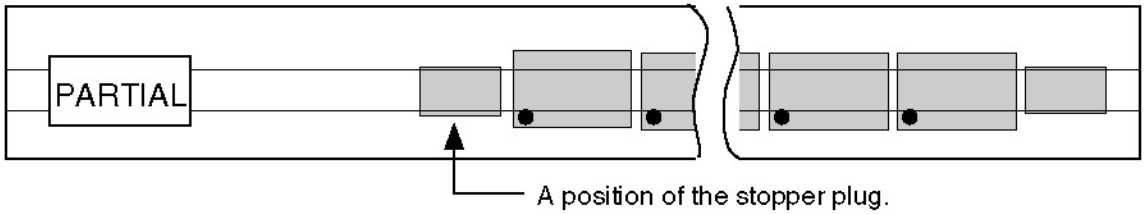
(2) The prevention of the vibration damage.

The stopper plug is pushed into the tube so that devices should not move and are kept plain condition.
Take care they do not warp.

(3) In case of a fraction

* In case IC number does not fill the typical accommodations, the stopper plug is used to fix devices.

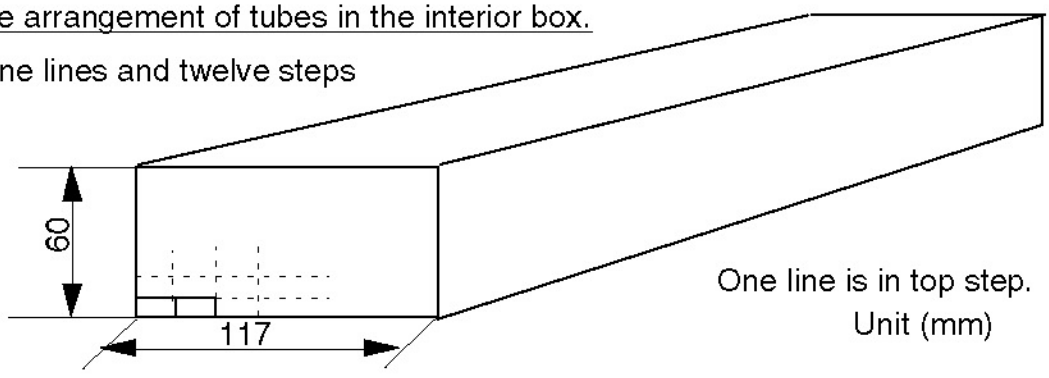
* "PARTIAL"label is stuck on the fraction tube as shown below.



2. Interior box and exterior box

2.1 The arrangement of tubes in the interior box.

Nine lines and twelve steps



2.2 Damp proof packing

Use the specified PE bag and put a silica gel in it.

* Put the sealed interior box in a PE bag.
* Put the silica gel on the top step in the box.