Document Title

2.4GHz FSK Transceiver

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	August 2, 2002	Preliminary
0.1	Modify current consumption, Tx output power, sensitivity, RSSI range, frequency deviation, data rate, SPI interface, and pin description.	October 16, 2002	Preliminary
0.2	Modify X'TAL Settling Time, Tx output power (Hi power) Application Circuit, and delete X'TAL accuracy	June 9, 2003	Preliminary
0.3	Modify Tx output power (Hi power)	Dec. 30 2003	Preliminary
0.4	Modify data rate and calibration mode	March 10, 2004	Preliminary

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Typical Applications

- Wireless Mouse and Keyboard
- 2.4GHz ISM Band Communication System
- Two way wireless Transceiver
- Wireless toy
- Wireless Modem

General Description

The A7101 is a monolithic CMOS integrated circuit intended for use as a low cost FSK transceiver in wireless applications. The device is provided in 48-lead plastic QFN7X7 packaging and is designed to function as a complete FSK transceiver. It is intended for wireless applications in the 2.4GHz to 2.5GHz ISM band. This chip features a fully programmable frequency synthesizer with integrated VCO circuitry.

Pin Configurations

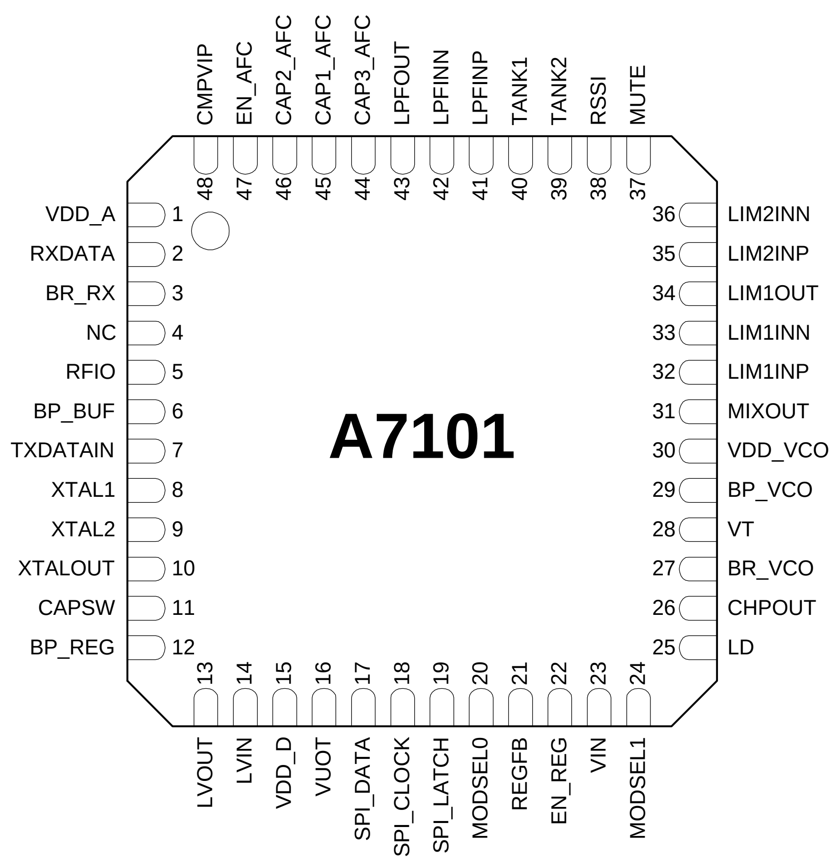


Figure 1. QFN Package Top View

Block Diagram

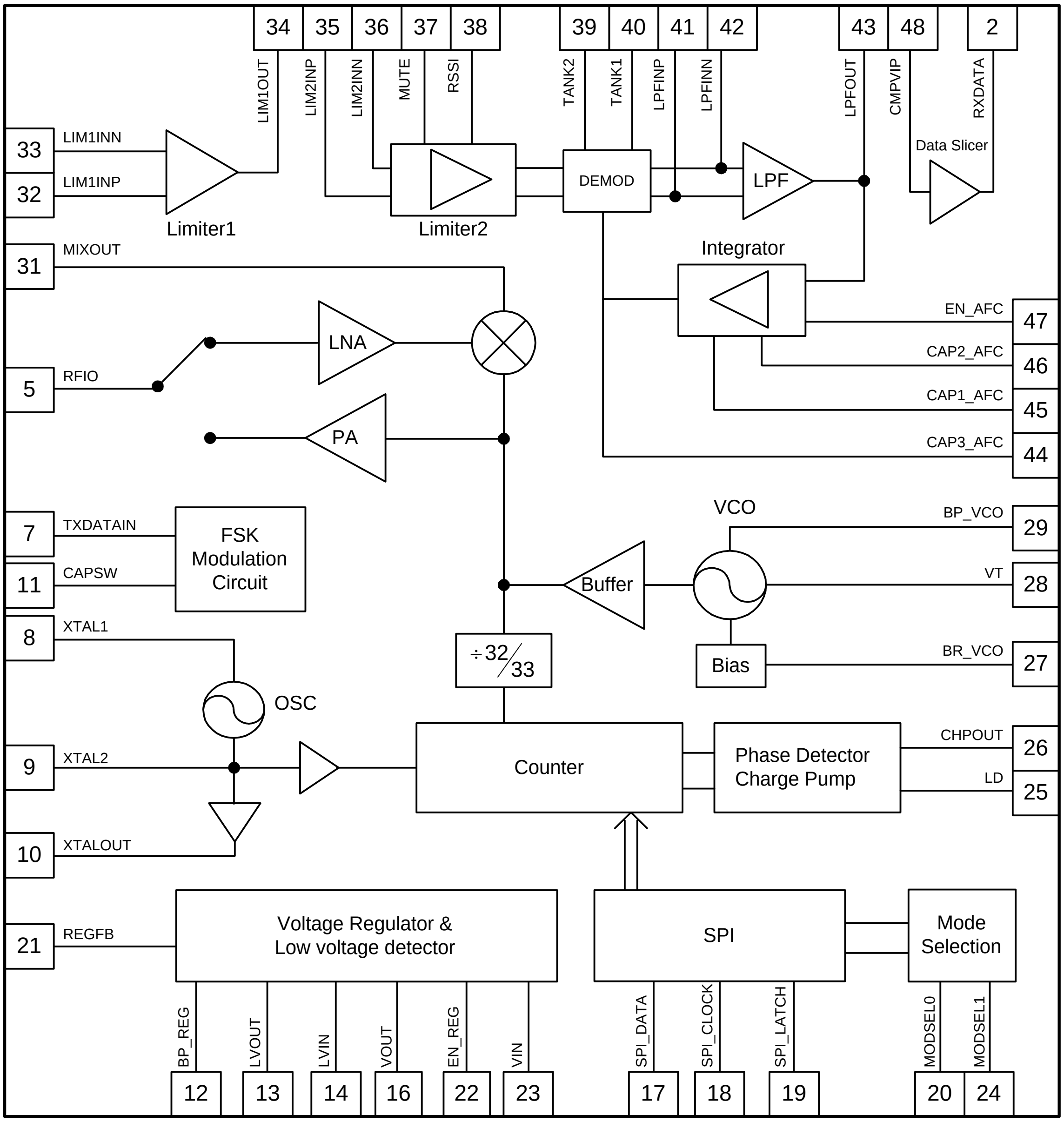


Figure 2. System Block Diagram

Specification

Parameter	Description	Min.	Typ.	Max.	Unit
General					
Storage Temperature		-20		70	°C
Operating Temperature		0		50	°C
Supply Voltage		2.2	2.5	5	V
Current Consumption Transceiver Circuit	Active (RX Mode)		30		mA
	Active (TX Mode @high power)		17		mA
	Active (TX Mode @low power)		14		mA
	Stand By Mode		1.5		mA
	Sleep Mode		5		μA
Current Consumption Embedded Regulator	Active @VIN = 3.3V		150		μA
	Stand By		5		μA
Phase Locked Loop					
Reference Frequency		4,6,8,10,12,14,16			MHz
X'TAL Settling Time	@12MHz, cap. Load = 20pF		5		ms
Operation Frequency			2416~2478		MHz
Number of Channels	@ 2MHz spacing		32		
PLL Settling Time	@Loop bandwidth = 100KHz		150		μs
RF Front End (TX mode)					
TX Power	High Power		-6		dBm
	Low Power		-16		dBm
RF Output Impedance	@2.45GHz		50		Ohm
RF Front End (RX mode)					
RF Input Impedance	@2.45GHz		50		Ohm
Sensitivity	@BER=0.001		-80		dBm
Cascaded IIP3 TBM			-30		dBm
IF Section					
Intermediate Frequency			10.7		MHz
RSSI Range	@RF input	-90		-50	dBm
Modulation / Demodulation					
Scheme	FSK				
Data rate	@ Crystal modulation			64	Kbps
	@ VCO modulation	100			Kbps
Frequency Deviation	@ Crystal modulation		50		KHz
	@ VCO modulation		150		KHz
Regulator					
Supply voltage				5	V
Output voltage			2.5		V
Drop out voltage			0.2		V
Load current				50	mA
Battery-Low indicator reference			1.2		V

Table 1.

RF - Baseband Interface

Pin Number	Pin Name	Description	Note
23	VIN	Supply voltage.	
	GND	Ground.	Please see Pin Descriptions section for detail.
7	TXDATAIN	Transmitter data input.	
2	RXDATA	Receiver data output.	
17	SPI_DATA	Data for SPI interface.	
18	SPI_CLOCK	Clock for SPI interface.	
19	SPI_LATCH	Latch for SPI interface.	
20	MODSEL0	Chip operation mode selection (LSB).	Option.
24	MODSEL1	Chip operation mode selection (MSB).	Option.
25	LD	PLL locked detect Indicator output.	Option.
22	EN_REG	Voltage regulator enable pin.	Option.
13	LVOUT	Battery-low indicator output.	Option.
37	MUTE	Receiver mute control output pin.	Option.
47	EN_AFC	AFC circuit control pin.	Option.

Table 2.

Pin Descriptions (I: input O: output OD: open drain output)

Pin No.	Symbol	I/O	Function Description
1	VDD_A	I	Analog supply voltage input.
2	RXDATA	OD	Recovered data output. This pin is an open drain output.
3	BR_RX	O	Receiver band gap bias output. Connect to external resistor to set bias current.
4	NC		This pin must be open.
5	RFIO	I/O	RF input/output port.
6	BP_BUF	O	Noise bypass. Connect to external noise rejection capacitor.
7	TXDATAIN	I	Transmitter data input.
8	XTAL1	I	Colpitts crystal oscillator node 1. Connect to external feedback capacitor.
9	XTAL2	I	Colpitts crystal oscillator node 2. Connect to external feedback capacitor.
10	XTALOUT	O	Buffered crystal oscillator output.
11	CAPSW	I	Modulation switch input.
12	BP_REG	O	Regulator band gap bypass output. Connect to external noise rejection capacitor. Typical output voltage is 1.2V.
13	LVOUT	O	Battery-Low voltage indicator output. This pin is active low when LVIN is below BP_REG voltage level.
14	LVIN	I	Input for battery-low voltage indicator. The indicator compares LVIN with the threshold voltage, BP_REG.
15	VDD_D	I	Digital supply voltage input.
16	VOUT	O	Regulator output voltage. Nominal voltage output is 2.5V.
17	SPI_DATA	I/OD	Data for SPI interface. This pin operates as an Input pin when SPI is in Write mode. This pin operates as an open drain output when SPI is in Read mode.
18	SPI_CLOCK	I	Clock input for SPI interface.
19	SPI_LATCH	I	Latch input for SPI interface.
20 24	MODSEL0 MODSEL1	I	Transceiver (embedded regulator is not included) operation mode selection inputs. MODSEL[1:0] = 00: Sleep mode. Transceiver circuit is turned off. MODSEL[1:0] = 01: Stand-by mode. X'TAL oscillator is turned on. MODSEL[1:0] = 10: Transmit mode. MODSEL[1:0] = 11: Receive mode.
21	REGFB	O	Output from regulator feedback network. VOUT is set to nominal voltage when this pin is opened. If other voltage is required, connect it to external resistor to adjust VOUT.
22	EN_REG	I	Voltage regulator enable pin. Signal is active high.
23	VIN	I	Supply voltage for the internal voltage regulator.
25	LD	OD	Output from PLL lock detector. This pin is active high (Open drain) when PLL is locked.
26	CHPOUT	O	Charge-pump output. This pin charges external capacitor to adjust VCO frequency.
27	BR_VCO	O	VCO band gap bias output. Connect to external resistor to set bias current.
28	VT	I	VCO tuning voltage input. The VCO frequency increases as VT increases.
29	BP_VCO	O	Noise bypass. Connect to external noise rejection capacitor.
30	VDD_VCO	I	VCO supply voltage input.

Pin Descriptions (I: input O: output OD: open drain output)(continued)

Pin No.	Symbol	I/O	Function Description
31	MIXOUT	O	Single-ended Mixer output.
32	LIM1INP	I	First Limiter differential positive input.
33	LIM1INN	I	First Limiter differential negative input.
34	LIM1OUT	O	First Limiter single-ended output.
35	LIM2INP	I	Second Limiter differential positive input.
36	LIM2INN	I	Second Limiter differential negative input.
37	MUTE	OD	Receiver mute control output. Open drain output. This pin is active low when received RF signal is under threshold level.
38	RSSI	O	Received Signal Strength Indicator output. RSSI output voltage is inversely proportional to the received RF signal power level.
39	TANK2	I	Demodulator Tank 2 input.
40	TANK1	I	Demodulator Tank 1 input.
41	LPFINP	I	Low pass filter differential positive input.
42	LPFINN	I	Low pass filter differential negative input.
43	LPFOUT	O	Low pass filter single-ended output.
44	CAP3_AFC	O	Auto frequency control circuit output bypass pin3. Connect to external capacitor.
45	CAP1_AFC	O	Auto frequency control circuit output bypass pin 1. Connect to external capacitor.
46	CAP2_AFC	O	Auto frequency control circuit output bypass pin 2. Connect to external capacitor.
47	EN_AFC	I	AFC circuit control input. Signal is active high.
48	CMPVIP	I	Positive input for data slicer.

Table 3.

Absolute Maximum Rating*

Parameter	With respect to	Rating	Unit
Supply voltage range (VDD)	GND	-0.3 to 5.5	Vdc
Other I/O pins range	GND	-0.3 to VDD+0.3	Vdc
Maximum input RF level		0	dBm
Storage temperature range		-20 ~ +70	°C

Table 4.

*Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Circuit Description

1. Low Noise Amplifier

The first stage of the receiver is a low noise amplifier. The main function of the LNA is to provide enough gain to overcome noise generated by subsequent stages. In order to make the circuit less sensitive to parasitic parameters, and more tolerant to common mode disturbances, differential pair is used. The LNA operates at very low power consumption with modest 20dB voltage gain. It is internally matched to 50ohm. No other external components are required.

2. RF Mixer

The RF mixer is designed to translate incoming RF signal to intermediate frequency (IF). The mixer is a conventional double balanced Gilbert cell mixer. Its output impedance is matched to 330ohm. A conventional 330ohm ceramic filter should be connected between the mixer and the first limiter to filter out all un-wanted noise.

3. IF Limiter

The IF limiter consists of two stages:

The first IF limiter stage consists of 3 differential amplifiers and a single-ended output buffer. The output impedance of the single-ended buffer is matched internally to 330 ohm, permitting direct connection to a 330ohm ceramic filter. A second filter can be connected between the first limiter and the second limiter to increase the receiver selectivity. Minimum input level of approximately 100mV_{RMS} is required at the first limiter to generate a limited signal at the output of the second IF limiter. The first IF limiter provides a gain of approximately 34dB. A by-pass capacitor of 10nF should be used to connect LIM1INN to ground.

The second IF limiter consists of 4 differential amplifiers and a differential output buffer. The second IF limiter provides an overall gain of approximately 40 dB. A by-pass capacitor of 10nF should be used to connect LIM2INN to ground. The limiter output is fed directly to the FSK demodulator.

4. Demodulator

The demodulator demodulates the FSK signal. It consists of a quadrature multiplier, external LC tank circuit and a tuning circuit to adjust the tank resonant frequency.

5. Low Pass Filter (LPF)

An internal operational amplifier connected with external RC components makes up the LPF. The bandwidth of LPF can be determined by external RC values.

6. Data Slicer

The data slicer compares the output of low pass filter with internal reference voltage threshold, V_{REF} and provides binary logic signals. The data slicer output is open drain type and will be pull high when data is muted.

7. RESET

When SPI_CLOCK and SPI _LATCH are both held high simultaneously, bit 4 through bit 9 of the Mode Select Register will be reset to “Low” state.

8. Serial to Parallel Interface (SPI)

The SPI bus consists of three signals: SPI_DATA, SPI_CLOCK, and SPI_LATCH. This interface is used for external base-band controller to communicate with transmitter's internal data and control registers. The contents of the registers are shown in the following register description sections.

After setting SPI_LATCH signal to "Low" state, data on SPI_DATA is shifted into the internal shift register on the rising edge of SPI_CLOCK with MSB going in first. SPI_LATCH should be asserted at the end to latch the data packet into the register according to the address bits, bit 0 through bit 3, for each of the registers. All registers can only be written into except the Status Register which can only be read.

When the content of the Status Register need to be fetched by external controller, external baseband controller need to make sure that the address bits are pointing to address location 0x0 for proper read operation. After the address bits are shifted into the SPI interface and latched by asserting SPI_LATCH, the SPI interface will be in Read Mode and the content of the Status Register will be shifted out on SPI_DATA pin. When all 12 status bits have been shifted out, the SPI bus will be put back to Write Mode automatically.

A. Register Description

Note: Convention used:

1: Logic level "ONE".
0: Logic level "ZERO".
X: Don't care.

Synthesizer Configuration Register I (Write only / Address 0xf)

Bit 15	Bit 14	Bit 13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit 1	Bit 0
MB6	MB5	MB4	MB3	MB2	MB1	MB0	MA4	MA3	MA2	MA1	MA0	1	1	1	1

Synthesizer Configuration Register II (Write only / Address 0x7)

Bit 15	Bit 14	Bit 13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit 1	Bit 0
X	MB9	MB8	MB7	R7	R6	R5	R4	R3	R2	R1	R0	0	1	1	1

Synthesizer Configuration Register I and Synthesizer Configuration Register II control synthesizer frequency settings where

MA[4:0]: A counter[4:0],
MB[9:0]: B counter[9:0],
R[7:0]: R counter[7:0]. Valid range is from 2 to 255.

The content of A, B and R registers are in unsigned binary format (i.e., $11111_2 = 31_{10}$).

The equation for setting the synthesizer frequency is:

$f_{vco} = f_{crystal} * (32*B + A) / R$ (B must be greater than A).

$f_{ref} = f_{crystal} / R$

Crystal Control Register (Write only / Address 0xb)

Bit 15	Bit 14	Bit 13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit 1	Bit 0
0	DP	TXH2	TXH1	TXH0	TXL2	TXL1	TXL0	FX3	FX2	FX1	FX0	1	0	1	1

DP: Data Polarity. This control bit sets data output polarity.
0: Data is inverted.
1: Normal.

TXH[2:0]: Reserved. Must be set to 0x0 for proper operation.
TXL[2:0]: Reserved. Must be set to 0x0 for proper operation.
FX[3:0]: Reserved. Must be set to 0x0 for proper operation.

VCO Control Register (Write only / Address 0x3)

Bit 15	Bit 14	Bit 13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit 1	Bit 0
VTH2	VTH1	VTH0	T1	T0	HP0	CP2	CP1	CP0	VC2	VC1	VC0	0	0	1	1

VTH[2:0]: Set VCO tuning voltage range. Valid range is from 0x7 to 0x0. The setting of VTH varies inversely with the tuning voltage range such that when VTH = 0x0 tuning voltage range is from 0.3V to VDD-0.3V and when VTH = 0x7 tuning voltage range is from 1V to VDD-1V.

T[1:0]: Reserved. Must be set to 0x0 for proper operation.

HP0: RF output power level control.
0: Low power output (-16 dBm).
1: High power output (-6 dBm).

CP[2]: Reserved. Must be set to 0x0 for proper operation.

CP[1:0]: Charge pump output current control. Valid range is from 0x3 to 0x0. The setting of CP varies linearly with the output current level such that when CP = 0x0 output current = 100uA and when CP = 0x3 output current = 700uA.

VC[2:0]: VCO band selection.

RX Control Register (Write only / Address 0xd)

Bit 15	Bit 14	Bit 13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit 1	Bit 0
T2	T1	T0	MT2	MT1	MT0	MTC	DM4	DM3	DM2	DMI	DM0	1	1	0	1

T[2:0]: Reserved. Must be set to 0x3 for proper operation.

MT[2:0]: Internal voltage threshold level for mute output (pin 37). Valid range is from 0x7 to 0x0. The setting of MT varies linearly with the voltage reference level such that when MT = 0x0 voltage reference = 1.44V and when MT = 0x7 voltage reference = 0.32V.

MTC: RXDATA mute function enable.
0: Disable mute function.
1: Enable mute function. When RSSI output voltage level is higher than the threshold set by MT[2:0], RXDATA becomes inactive and pull high.

DM[4:0]: Reference voltage level for demodulator tank center frequency tuning.
Valid range is from 0x1f to 0x6. The setting of DM varies with the voltage reference level such that when DM = 0x6 voltage reference = 0.9V and when DM = 0x1f voltage reference = 2.4V.

Note: When AFC function is used, set DM[4:0] to 0x0.

Mode Select Register (Write only / Address 0x5)

Bit 15	Bit 14	Bit 13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit 1	Bit 0
X	X	X	X	X	SC1	SC0	XOE	CM	EXTB	MD1	MD0	0	1	0	1

SC[1:0]: Status Register bit 6 control. Depends on the setting of SC[1:0], bit 6 of the Status Register can represent system error flag, Battery-low detect or PLL lock detect.

[1:0] = 10: System Error.
[1:0] = 11: Battery-low detect.
[1:0] = 0X: PLL lock detect.

XOE: Crystal oscillator buffer output enable.
0: Output enable.
1: Output disable. The output will be forced to low level at this setting.

CM: Calibration mode setting for VCO band selection.
0: manual calibration mode. Please see application note for detail description.
1: auto calibration mode.

EXTB: Operating mode selection.
0: external mode. Operation mode is determined by external pin MODSEL0 and MODSEL1.
1: internal mode. Operation mode is determined by setting of MD[1:0].

MD[1:0]: Internal mode selection.
[1:0] = 00: Sleep mode. Transceiver circuit is turned off.
[1:0] = 01: Stand-by mode. X'TAL oscillator is turned on.
[1:0] = 10: Transmit mode.
[1:0] = 11: Receive mode.

Status Register (Read only / Address 0x0)

SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
X	X	X	X	X	X	X	X	X	S/B/P	X	X	0	0	0	0

S/B/P: Depends on the setting of SC[1:0] in Mode Select Register, this bit can be used to reflect the status of System Error, Battery-low detect or PLL lock detect.
System Error: 0: Normal; 1: Error.
Battery-low detect: 0: Battery supply voltage below threshold. 1: Normal.
PLL lock detect: 0: Unlock. 1: Lock.

SR[3:0] address bits.

B. SPI Timing Diagram

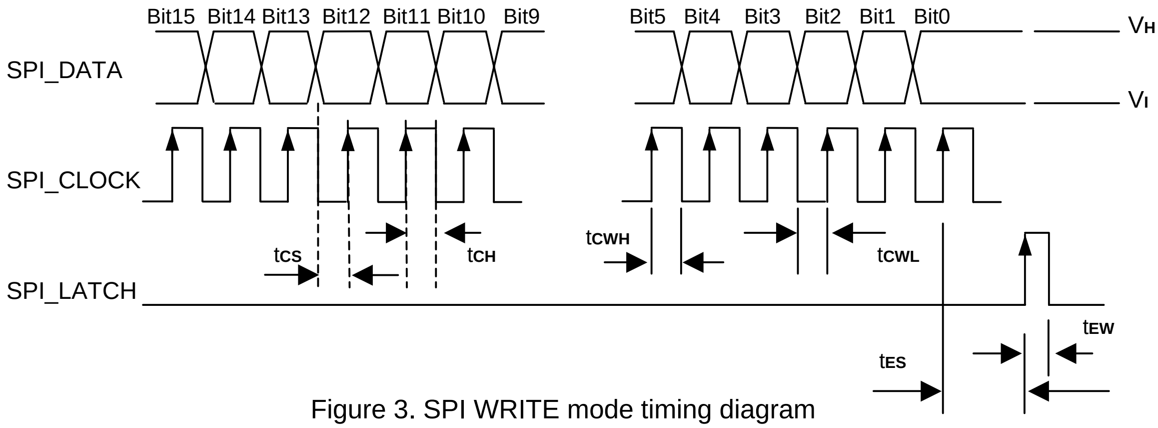


Figure 3. SPI WRITE mode timing diagram

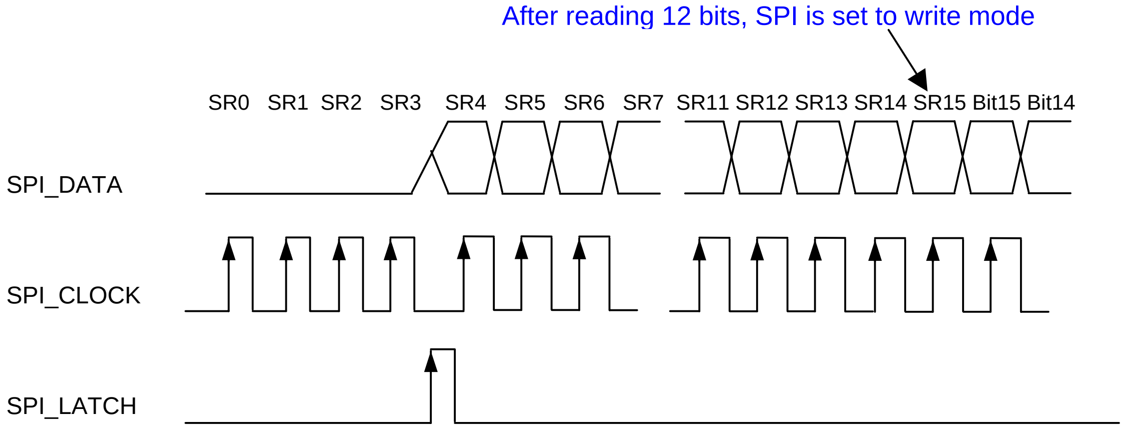


Figure 4. SPI READ mode timing diagram

C. SPI Timing Specification

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
V_H	The High level of voltage	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram	VCC-0.4			V
V_l	The low level of voltage	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram			0.4	V
t_{CE}	SPI_DATA to SPI_CLOCK setup time	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram	50			ns
t_{CH}	SPI_CLOCK to SPI_DATA hold time	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram	10			ns
t_{CWH}	SPI_CLOCK pulse width high	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram	50			ns
t_{CWL}	SPI_CLOCK pulse width low	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram	50			ns
t_{ES}	SPI_CLOCK to SPI_LATCH setup time	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram	50			ns
t_{EW}	SPI_LATCH pulse width	Three wire SPI_CLOCK, SPI_DATA, SPI_LATCH timing diagram	50			ns

Table 5.

9. PLL Section

The sub-block diagram of PLL is shown in the following:

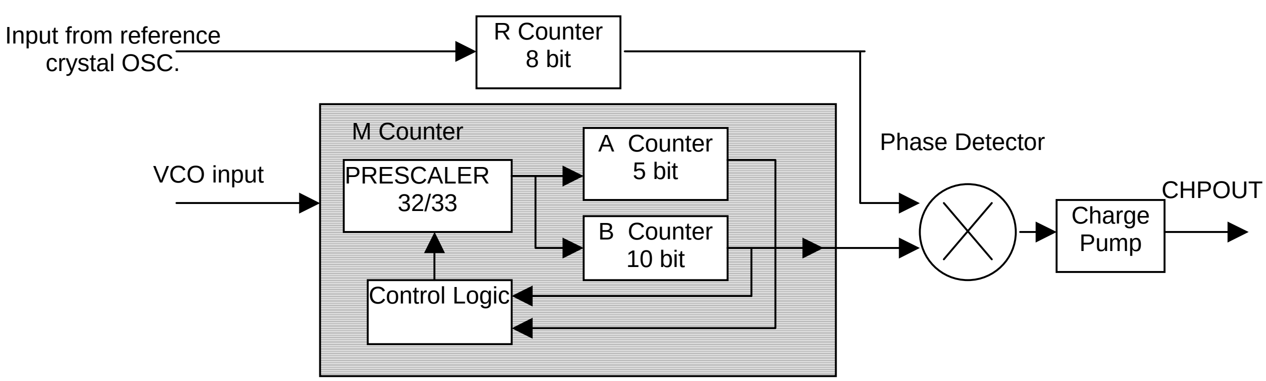


Figure 5. Phase Lock Loop Block Diagram

A. M Counter

The M counter consists of a 32/33 pre-scalar, a 5-bit A counter and a 10-bit B counter (where M = B*32+A).

B. A and B counters

A and B counters can be programmed through the Synthesizer Configuration Register I and II. The corresponding relations between the division ratio counters and Synthesizer Configuration Register are shown in the following table:

M counter	B counter	A counter	B counter (binary)										A counter (binary)				
(DEC)	(DEC)	(DEC)	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0	MA4	MA3	MA2	MA1	MA0
24000	750	0	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0
24001	750	1	1	0	1	1	1	0	1	1	1	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
24031	750	31	1	0	1	1	1	0	1	1	1	0	1	1	1	1	1
24032	751	0	1	0	1	1	1	0	1	1	1	1	0	0	0	0	0
24033	751	1	1	0	1	1	1	0	1	1	1	1	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
24063	751	31	1	0	1	1	1	0	1	1	1	1	1	1	1	1	1
24064	752	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
24992	781	0	1	1	0	0	0	0	1	1	0	1	0	0	0	0	0
24993	781	1	1	1	0	0	0	0	1	1	0	1	0	0	0	0	1
24994	781	2	1	1	0	0	0	0	1	1	0	1	0	0	0	1	0
24995	781	3	1	1	0	0	0	0	1	1	0	1	0	0	0	1	1
24996	781	4	1	1	0	0	0	0	1	1	0	1	0	0	1	0	0
24997	781	5	1	1	0	0	0	0	1	1	0	1	0	0	1	0	1
24998	781	6	1	1	0	0	0	0	1	1	0	1	0	0	1	1	0
24999	781	7	1	1	0	0	0	0	1	1	0	1	0	0	1	1	1
25000	781	8	1	1	0	0	0	0	1	1	0	1	0	1	0	0	0

Table 6.

C. R counter

R counter division R	R counter							
(DEC)	R7	R6	R5	R4	R3	R2	R1	R0
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
100	0	1	1	0	0	1	0	0
101	0	1	1	0	0	1	0	1
102	0	1	1	0	0	1	1	0
.	.	.	.	.	.	.	.	.
120	0	1	1	1	1	0	1	1
.	.	.	.	.	.	.	.	.
255	1	1	1	1	1	1	1	1

Note: Valid range of R counter is from 2 to 255.

Table 7.

The equation for setting the synthesizer frequency is:

$f_{vco} = f_{crystal}$ X (32 X B + A) / R (B must be greater than A).

D. Phase Frequency Detector (PFD) and Charge Pump

Phase Frequency Detector takes inputs from R counter and M counter, and produces an output proportional to the phase and frequency difference. The following shows a simplified schematic:

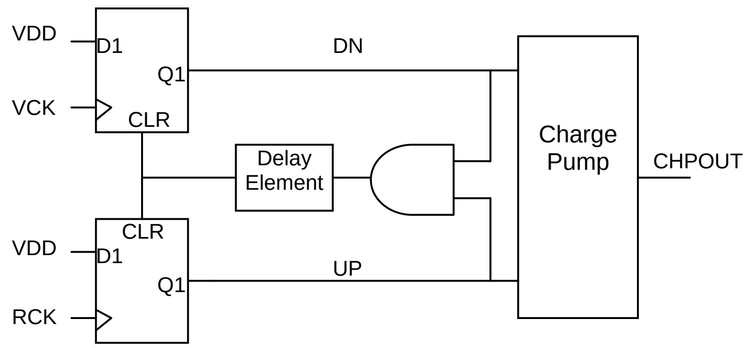


Figure 6. Phase Detector Block Diagram

The PFD output waveform is shown below.

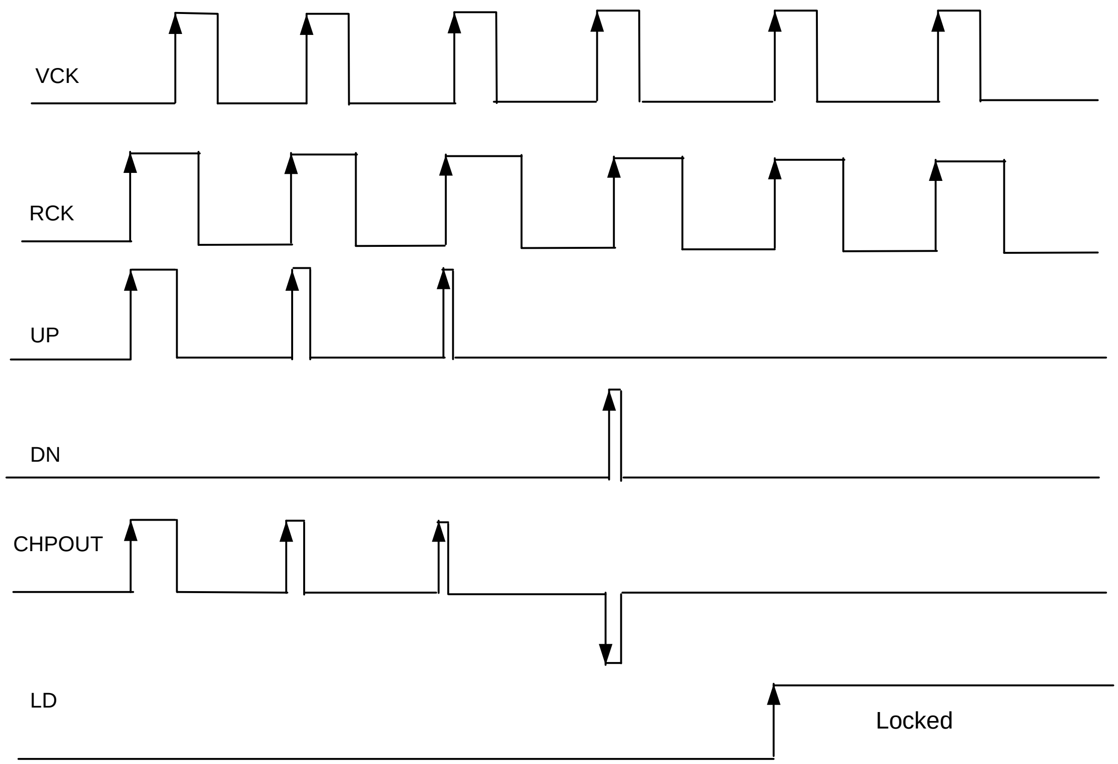


Figure 7. The PFD output waveform

10. Crystal Oscillator and FSK modulation Section

As shown in the following figure, it is a Colpitts type Crystal oscillator(XOSC). The FSK modulation is achieved by switching the external capacitor C_X in the XOSC circuit.

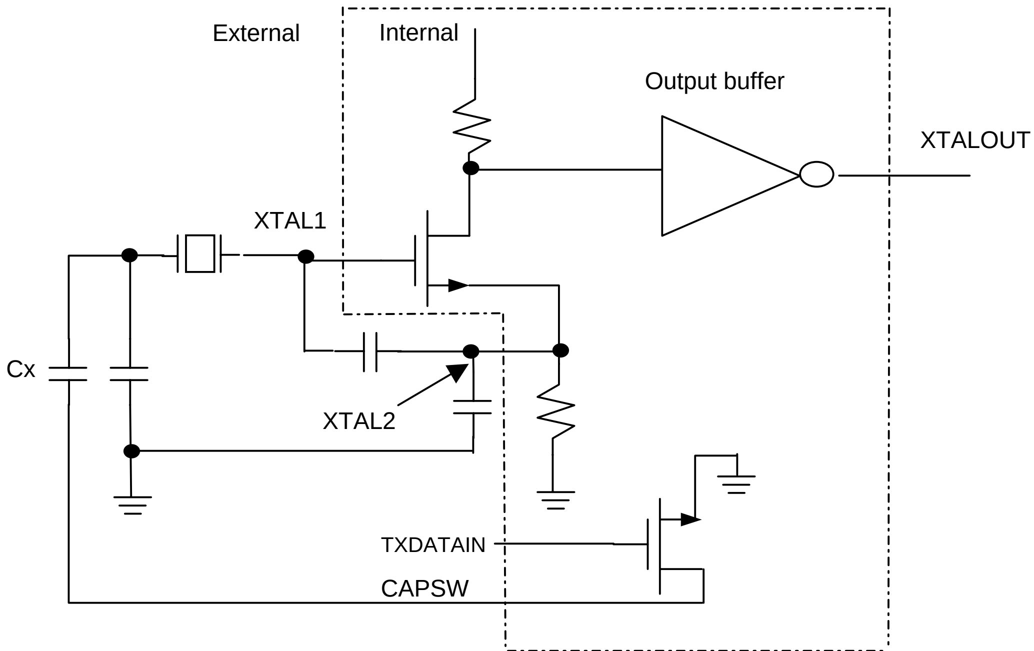


Figure 8. Crystal Oscillator and FSK modulation Circuit

12.Chip setup procedure:

(1) Auto calibration:

For Transmitter Operation

Step 1: Supply DC voltage to Pin 23, VIN.

Step 2: Set Pin 20, MODSEL0 and Pin 24, MODSEL1 to logic **0** (ground) to ensure the IC is operating in external sleep mode after reset.

Step 3: Reset IC by setting Pin 18, SPI_CLOCK and Pin 19, SPI _LATCH to logic high simultaneously for more than **1 us**.

Step 4: Setup IC's internal control registers by configuring the followings: Synthesizer Configuration Register I, Synthesizer Configuration Register II, Crystal Control Register, and VCO Control Register. All registers should be written to in the order specified above.

a. Synthesizer Configuration Register I and II: Set VCO center frequency.
b. Crystal Control Register: Set TXDATA polarity.
c. VCO Control Register: Set VCO tuning range and charge pump output current.

Step 5: Set IC to TX mode.

For internal mode operation, set Mode Select Register to **0x05E5**.

For external mode operation, set Pin 24, MODSEL1 to "logic **1**", Pin 20, MODSEL0 to "logic **0**" and set Mode Select Register to **0x05A5**.

Whenever frequency is to be changed, or system error has been detected (by reading from the Status Register) the IC must be reset by repeating step **2, 3, 4-a,** and **5**.

For Receiver Operation

Step 1: Supply DC voltage to Pin 23, VIN.

Step 2: Set Pin 20, MODSEL0 and Pin 24, MODSEL1 to logic **0** (ground) to ensure the IC is operating in external sleep mode after
reset.

Step 3: Reset IC by setting Pin 18, SPI_CLOCK and Pin 19, SPI _LATCH to logic high simultaneously for more than **1 us**.

Step 4: Setup IC's internal control registers by configuring the followings: Synthesizer Configuration Register I, Synthesizer Configuration Register II, VCO Control Register, RX Control Register, and the Mode Select Register. All registers should be written to in the order specified above.

a. Synthesizer Configuration Register I and II: Set VCO center frequency.
b. VCO Control Register: Set VCO tuning range and charge pump output current.
c. RX Control Register: Set mute threshold level, RXDATA mute function and reference voltage for demodulator tank center frequency tuning. When **AFC** function is used, DM[4:0] must be set to **0x0** for proper operation.

Step 5: Set IC to RX mode.

For internal mode operation, set Mode Select Register to **0x05F5**.

For external mode operation, set Pin 24, MODSEL1 to "logic **1**", Pin 20, MODSEL0 to "logic **1**" and set Mode Select Register to **0x05B5**.

Whenever frequency is to be changed, or system error has been detected (by reading from the Status Register) the IC must be reset by repeating step **2, 3, 4-a,** and **5**.

(2) Manual calibration:

Please see application note (AN_CAL_A7101) for detail description.

Application Circuit

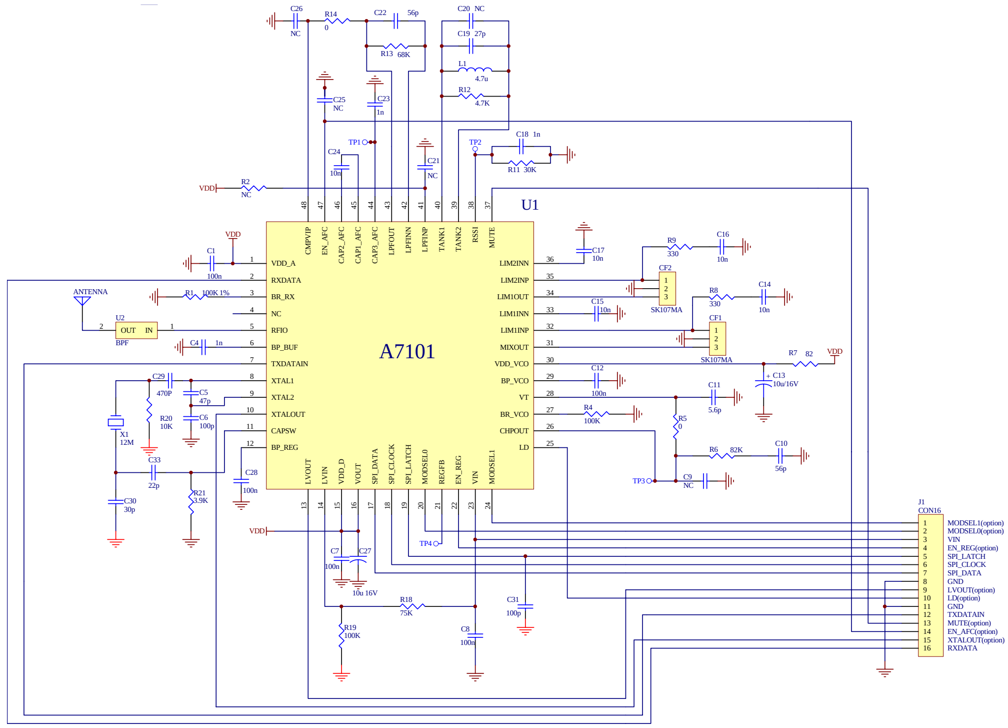


Figure 10. Application Circuit for Transceiver (Data rate = 64Kbps)

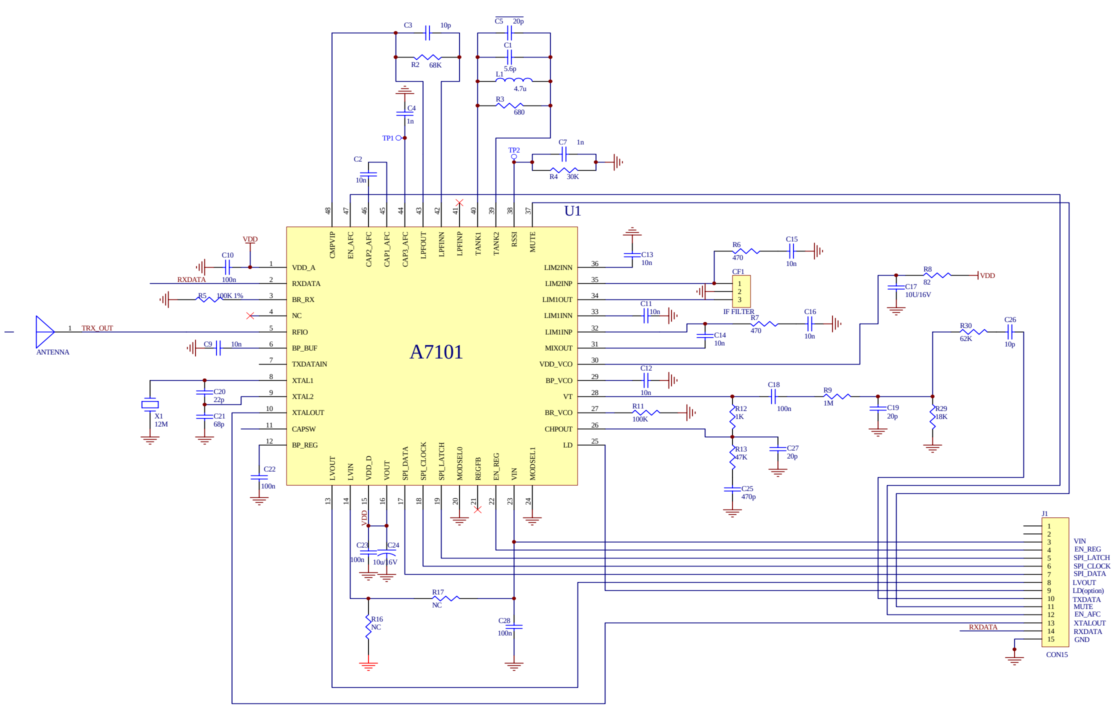


Figure 11. Application Circuit for Transceiver (Data rate = 250Kbps)

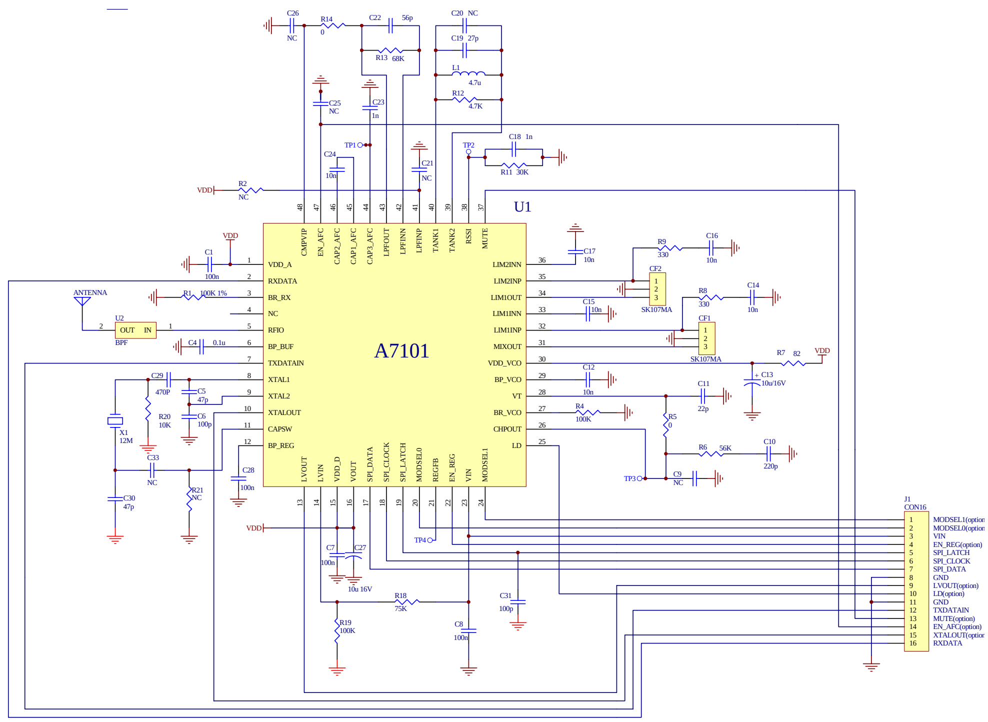


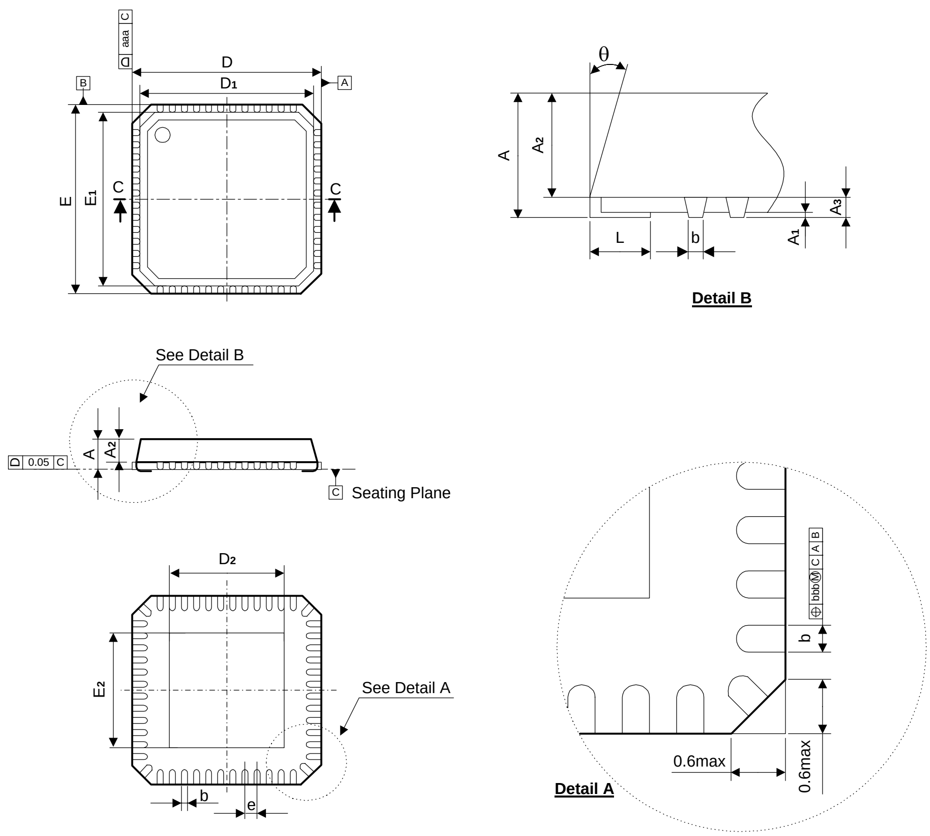
Figure 12. Application Circuit for Receiver

Ordering Information

Part No.	Package
A71P024P01Q	QFN 48L

Package Information

QFN 48L (7 x 7mm) Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.031	0.033	0.039	0.80	0.85	1.00
A_1	0.000	0.001	0.002	0.00	0.02	0.05
A_2	-	0.026	0.039	-	0.65	1.00
A_3	-	0.008	-	-	0.20	-
b	0.007	0.009	0.012	0.18	0.23	0.30
D	0.276 BSC			7.00 BSC		
D_1	0.266 BSC			6.75 BSC		
D_2	0.089	0.185	0.207	2.25	4.70	5.25
E	0.276 BSC			7.00 BSC		
E_1	0.266 BSC			6.75 BSC		
E_2	0.089	0.185	0.207	2.25	4.70	5.25
e	0.020 BSC			0.5 BSC		
L	0.012	0.016	0.020	0.30	0.40	0.50
θ	0°	-	12°	0°	-	12°
aaa	-	-	0.010	-	-	0.25
bbb	-	-	0.004	-	-	0.10