

To all our customers

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## **Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.**

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The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

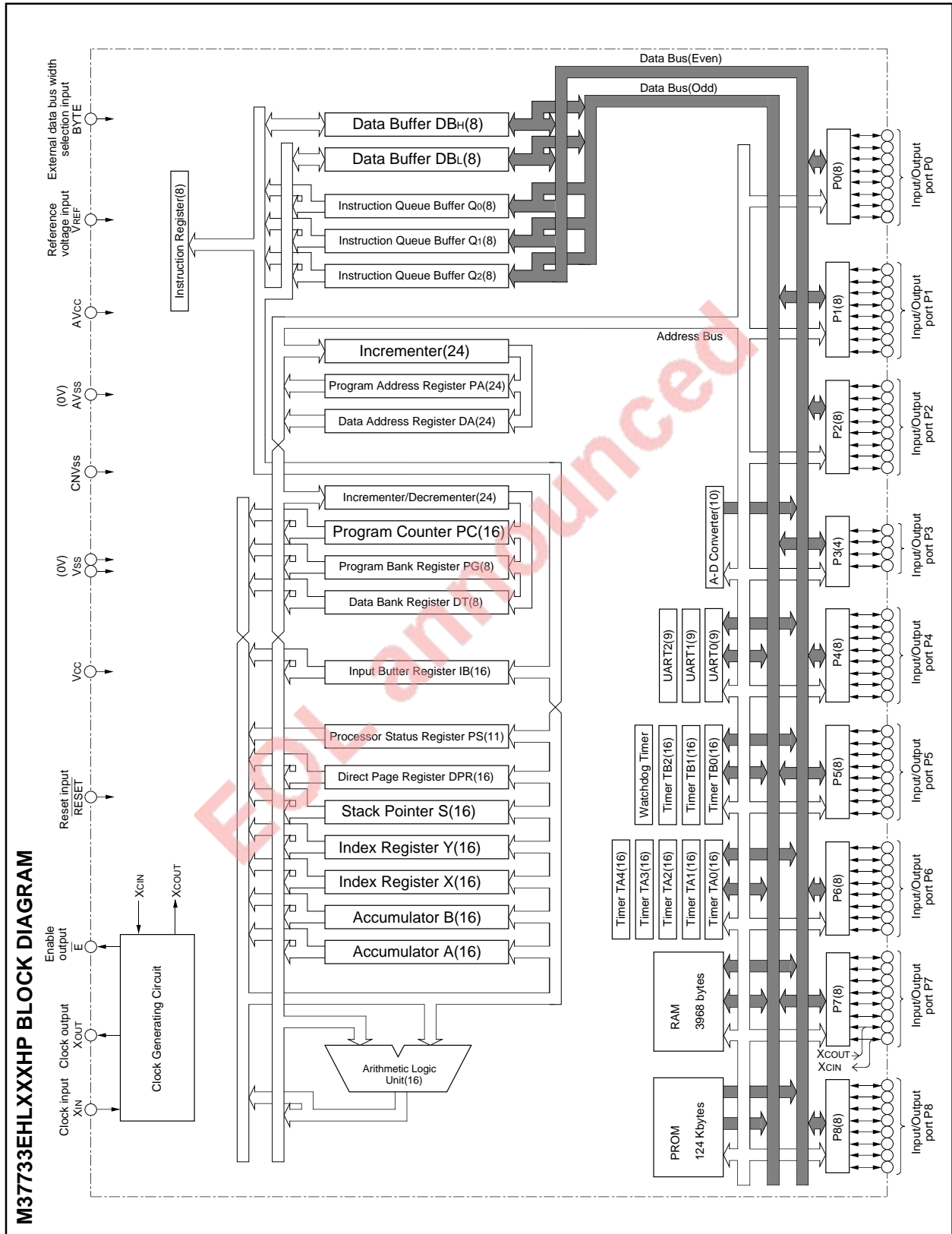
Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003



**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

**MITSUBISHI MICROCOMPUTERS**  
**M37733EHLXXXHP**

PROM VERSION OF M37733MHLXXXHP



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**MITSUBISHI MICROCOMPUTERS**  
**M37733EHLXXXHP**

PROM VERSION OF M37733MHLXXXHP

**FUNCTIONS OF M37733EHLXXXHP**

Parameter		Functions
Number of basic instructions		103
Instruction execution time		333 ns (the fastest instruction at external clock 12 MHz frequency)
Memory size	PROM	124 Kbytes
	RAM	3968 bytes
Input/Output ports	P0 – P2, P4 – P8	8-bit X 8
	P3	4-bit X 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bit X 5
	TB0, TB1, TB2	16-bit X 3
Serial I/O		(UART or clock synchronous serial I/O) X 3
A-D converter		10-bit X 1 (8 channels)
Watchdog timer		12-bit X 1
Interrupts		3 external types, 16 internal types Each interrupt can be set to the priority level (0 – 7.)
Clock generating circuit		2 circuits built-in (externally connected to a ceramic resonator or a quartz-crystal oscillator)
Supply voltage		2.7 – 5.5 V
Power dissipation		9 mW (at 3 V supply voltage, external clock 12 MHz frequency) 22.5 mW (at 5 V supply voltage, external clock 12 MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		Maximum 16 Mbytes
Operating temperature range		–40 to 85 °C
Device structure		CMOS high-performance silicon gate process
Package		80-pin plastic molded fine-pitch QFP (80P6D-A;0.5 mm lead pitch)

EOL announcement

**PIN DESCRIPTION**

Pin	Name	Input/Output	Functions
Vcc, Vss	Power source		Apply 2.7 – 5.5 V to Vcc and 0 V to Vss.
CNVss	CNVss input	Input	This pin controls the processor mode. Connect to Vss for the single-chip mode and the memory expansion mode, and to Vcc for the microprocessor mode.
RESET	Reset input	Input	When "L" level is applied to this pin, the microcomputer enters the reset state.
XIN	Clock input	Input	These are pins of main-clock generating circuit. Connect a ceramic resonator or a quartz-crystal oscillator between XIN and XOUT. When an external clock is used, the clock source should be connected to the XIN pin, and the XOUT pin should be left open.
XOUT	Clock output	Output	
E	Enable output	Output	This pin functions as the enable signal output pin which indicates the access status in the internal bus. When output level of E signal is "L", data/instruction read or data write is performed.
BYTE	External data bus width selection input	Input	In the memory expansion mode or the microprocessor mode, this pin determines whether the external data bus has an 8-bit width or a 16-bit width. The data bus has a 16-bit width when "L" signal is input and an 8-bit width when "H" signal is input.
AVcc, AVss	Analog power source input		Power source input pin for the A-D converter. Externally connect AVcc to Vcc and AVss to Vss.
VREF	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
P00 – P07	I/O port P0	I/O	In the single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in the input mode when reset. In the memory expansion mode or the microprocessor mode, these pins output address (A0 – A7).
P10 – P17	I/O port P1	I/O	In the single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in the memory expansion mode or the microprocessor mode and external data bus has a 16-bit width, high-order data (D8 – D15) is input/output or an address (A8 – A15) is output. When the BYTE pin is "H" and an external data bus has an 8-bit width, only address (A8 – A15) is output.
P20 – P27	I/O port P2	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, low-order data (D0 – D7) is input/output or an address (A16 – A23) is output.
P30 – P33	I/O port P3	I/O	In the single-chip mode, these pins have the same function as port P0. In the memory expansion mode or the microprocessor mode, R/W, BHE, ALE, and HLDA signals are output.
P40 – P47	I/O port P4	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, P40, P41, and P42 become HOLD and RDY input pins, and a clock $\phi_1$ output pin, respectively. Functions of the other pins are the same as in the single-chip mode. However, in the memory expansion mode, P42 can be selected as an I/O port.
P50 – P57	I/O port P5	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timers A0 to A3 and input pins for key input interrupt input (KI0 – KI3).
P60 – P67	I/O port P6	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timer A4, input pins for external interrupt input (INT0 – INT2) and input pins for timers B0 to B2. P67 also functions as sub-clock $\phi_{SUB}$ output pin.
P70 – P77	I/O port P7	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins function as input pins for A-D converter. P72 to P75 also function as I/O pins for UART2. Additionally, P76 and P77 have the function as the output pin (XCOUT) and the input pin (XCIN) of the sub-clock (32 kHz) oscillation circuit, respectively. When P76 and P77 are used as the XCOUT and XCIN pins, connect a resonator or an oscillator between the both.
P80 – P87	I/O port P8	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for UART 0 and UART 1.

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**MITSUBISHI MICROCOMPUTERS**  
**M37733EHLXXXHP**

PROM VERSION OF M37733MHLXXXHP

**PIN DESCRIPTION (EPROM MODE)**

Pin	Name	Input/Output	Functions
VCC, VSS	Power supply		Supply 5V±10% to Vcc and 0V to Vss.
CNVSS	VPP input	Input	Connect to VPP when programming or verifying.
BYTE	VPP input	Input	Connect to VPP when programming or verifying.
RESET	Reset input	Input	Connect to Vss.
XIN	Clock input	Input	Connect a ceramic resonator between XIN and XOUT.
XOUT	Clock output	Output	
E	Enable output	Output	Keep open.
AVCC, AVSS	Analog supply input		Connect AVcc to Vcc and AVss to Vss.
VREF	Reference voltage input	Input	Connect to Vss.
P00 – P07	Address input (A0 – A7)	Input	Port P0 functions as the lower 8 bits address input (A0 – A7).
P10 – P17	Address input (A8 – A15)	Input	Port P1 functions as the higher 8 bits address input (A8 – A15).
P20 – P27	Data I/O (D0 – D7)	I/O	Port P2 functions as the 8 bits data bus (D0 – D7).
P30	Address input (A16)	Input	P30 functions as the most significant bit address input (A16).
P31 – P33	Input port P3	Input	Connect to Vss.
P40 – P47	Input port P4	Input	Connect to Vss.
P50 – P57	Control signal input	Input	P50, P51 and P52 function as PGM, OE and CE input pins respectively. Connect P53, P54, P55 and P56 to Vcc. Connect P57 to Vss.
P60 – P67	Input port P6	Input	Connect to Vss.
P70 – P77	Input port P7	Input	Connect to Vss.
P80 – P87	Input port P8	Input	Connect to Vss.

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**BASIC FUNCTION BLOCKS**

The M37733EHLXXXHP has the same functions as the M37733MHBXXXFP except for the following :

- (1) The built-in ROM is PROM.
- (2) The package is different.
- (3) The reset circuit is different.
- (4) The status of bit 3 of the oscillation circuit control register 1 (address 6F16) at a reset is different.
- (5) The usage condition of bit 3 of the oscillation circuit control register 1 is different.

Accordingly, refer to the basic function blocks description in the M37733MHBXXXFP except for Figure 1 (bit configuration of the oscillation circuit control register 1) , Figure 3 and Figure 4 (reset circuit).

In the M37733EHLXXXHP, bit 3 of the oscillation circuit control register 1 must be "1". (Refer to Figure 1.) The status of this bit at a reset is "1".

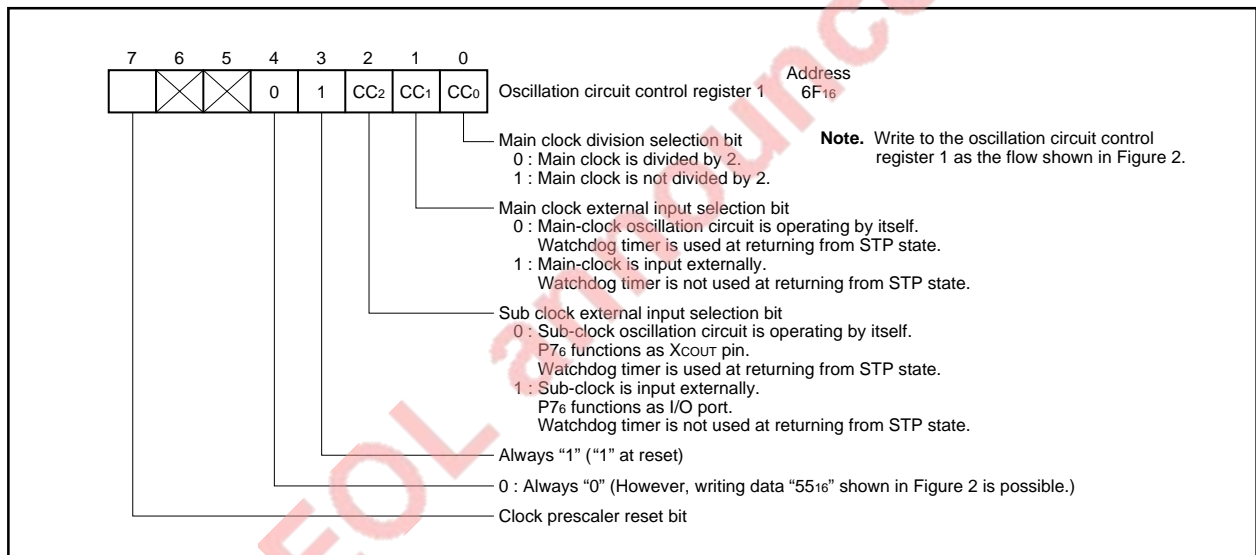


Fig. 1 Bit configuration of oscillation circuit control register 1 (corresponding to Figure 63 in data sheet "M37733MHBXXXFP")

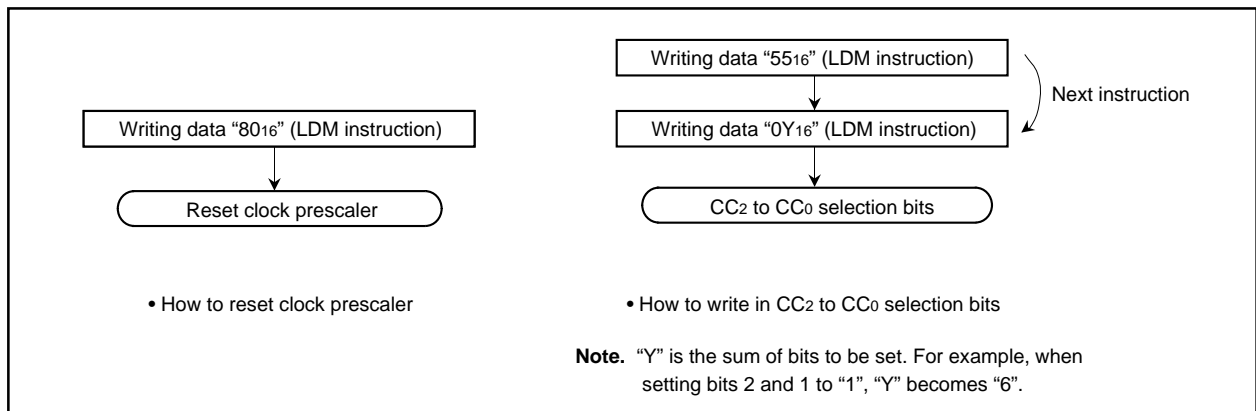


Fig. 2 How to write data in oscillation circuit control register 1 (identical with Figure 64 in data sheet "M37733MHBXXXFP")

## RESET CIRCUIT

The microcomputer is released from the reset state when the  $\overline{\text{RESET}}$  pin is returned to "H" level after holding it at "L" level with the power source voltage at 2.7 – 5.5 V. Program execution starts at the address formed by setting address  $A_{23} - A_{16}$  to 0016,  $A_{15} - A_8$  to the contents of address FFFF<sub>16</sub>, and  $A_7 - A_0$  to the contents of address FFFE<sub>16</sub>. Figure 3 shows the microcomputer internal status during reset. Figure 4 shows an example of a reset circuit. When the stabilized clock is input from the external to the main-clock oscillation circuit, the reset input voltage must be 0.55 V or less when the power source voltage reaches 2.7 V. When a resonator/oscillator is connected to the main-clock oscillation circuit, change the reset input voltage from "L" to "H" after the main-clock oscillation is fully stabilized.

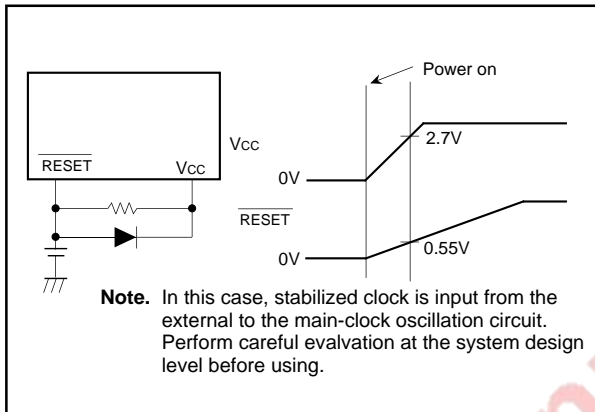


Fig. 4 Example of a reset circuit



	Address		Address		
Port P0 direction register	(04 <sub>16</sub> ) <sup>***</sup>	00 <sub>16</sub>	Watchdog timer frequency selection flag	(61 <sub>16</sub> ) <sup>***</sup>	XXXXXXXXXX0
Port P1 direction register	(05 <sub>16</sub> ) <sup>***</sup>	00 <sub>16</sub>	Memory allocation control register	(63 <sub>16</sub> ) <sup>***</sup>	XXXXXXXX00000
Port P2 direction register	(08 <sub>16</sub> ) <sup>***</sup>	00 <sub>16</sub>	UART2 transmit/receive mode register	(64 <sub>16</sub> ) <sup>***</sup>	X0000000
Port P3 direction register	(09 <sub>16</sub> ) <sup>***</sup>	XXXXXX0000	UART2 transmit/receive control register 0	(68 <sub>16</sub> ) <sup>***</sup>	XXXXXXXX1000
Port P4 direction register	(0C <sub>16</sub> ) <sup>***</sup>	00 <sub>16</sub>	UART2 transmit/receive control register 1	(69 <sub>16</sub> ) <sup>***</sup>	000000010
Port P5 direction register	(0D <sub>16</sub> ) <sup>***</sup>	00 <sub>16</sub>	Oscillation circuit control register 0	(6C <sub>16</sub> ) <sup>***</sup>	X00000X1
Port P6 direction register	(10 <sub>16</sub> ) <sup>***</sup>	00 <sub>16</sub>	Port function control register	(6D <sub>16</sub> ) <sup>***</sup>	00 <sub>16</sub>
Port P7 direction register	(11 <sub>16</sub> ) <sup>***</sup>	00 <sub>16</sub>	Serial transmit control register	(6E <sub>16</sub> ) <sup>***</sup>	XXXX00XXXX
Port P8 direction register	(14 <sub>16</sub> ) <sup>***</sup>	00 <sub>16</sub>	Oscillation circuit control register 1	(6F <sub>16</sub> ) <sup>***</sup>	0XXXX01000
A-D control register 0	(1E <sub>16</sub> ) <sup>***</sup>	00000???	A-D/UART2 trans./rece. interrupt control register	(70 <sub>16</sub> ) <sup>***</sup>	XXXXXXXX0000
A-D control register 1	(1F <sub>16</sub> ) <sup>***</sup>	XXXX000X11	UART 0 transmission interrupt control register	(71 <sub>16</sub> ) <sup>***</sup>	XXXXXXXX0000
UART 0 transmit/receive mode register	(30 <sub>16</sub> ) <sup>***</sup>	00 <sub>16</sub>	UART 0 receive interrupt control register	(72 <sub>16</sub> ) <sup>***</sup>	XXXXXXXX0000
UART 1 transmit/receive mode register	(38 <sub>16</sub> ) <sup>***</sup>	00 <sub>16</sub>	UART 1 transmission interrupt control register	(73 <sub>16</sub> ) <sup>***</sup>	XXXXXXXX0000
UART 0 transmit/receive control register 0	(34 <sub>16</sub> ) <sup>***</sup>	00001000	UART 1 receive interrupt control register	(74 <sub>16</sub> ) <sup>***</sup>	XXXXXXXX0000
UART 1 transmit/receive control register 0	(3C <sub>16</sub> ) <sup>***</sup>	00001000	Timer A0 interrupt control register	(75 <sub>16</sub> ) <sup>***</sup>	XXXXXXXX0000
UART 0 transmit/receive control register 1	(35 <sub>16</sub> ) <sup>***</sup>	00000010	Timer A1 interrupt control register	(76 <sub>16</sub> ) <sup>***</sup>	XXXXXXXX0000
UART 1 transmit/receive control register 1	(3D <sub>16</sub> ) <sup>***</sup>	00000010	Timer A2 interrupt control register	(77 <sub>16</sub> ) <sup>***</sup>	XXXXXXXX0000
Count start flag	(40 <sub>16</sub> ) <sup>***</sup>	00 <sub>16</sub>	Timer A3 interrupt control register	(78 <sub>16</sub> ) <sup>***</sup>	XXXXXXXX0000
One-shot start flag	(42 <sub>16</sub> ) <sup>***</sup>	XXXX0000	Timer A4 interrupt control register	(79 <sub>16</sub> ) <sup>***</sup>	XXXXXXXX0000
Up-down flag	(44 <sub>16</sub> ) <sup>***</sup>	00 <sub>16</sub>	Timer B0 interrupt control register	(7A <sub>16</sub> ) <sup>***</sup>	XXXXXXXX0000
Timer A0 mode register	(56 <sub>16</sub> ) <sup>***</sup>	00 <sub>16</sub>	Timer B1 interrupt control register	(7B <sub>16</sub> ) <sup>***</sup>	XXXXXXXX0000
Timer A1 mode register	(57 <sub>16</sub> ) <sup>***</sup>	00 <sub>16</sub>	Timer B2 interrupt control register	(7C <sub>16</sub> ) <sup>***</sup>	XXXXXXXX0000
Timer A2 mode register	(58 <sub>16</sub> ) <sup>***</sup>	00 <sub>16</sub>	INT <sub>0</sub> interrupt control register	(7D <sub>16</sub> ) <sup>***</sup>	XXXX000000
Timer A3 mode register	(59 <sub>16</sub> ) <sup>***</sup>	00 <sub>16</sub>	INT <sub>1</sub> interrupt control register	(7E <sub>16</sub> ) <sup>***</sup>	XXXX000000
Timer A4 mode register	(5A <sub>16</sub> ) <sup>***</sup>	00 <sub>16</sub>	INT <sub>2</sub> /Key input interrupt control register	(7F <sub>16</sub> ) <sup>***</sup>	XXXX000000
Timer B0 mode register	(5B <sub>16</sub> ) <sup>***</sup>	00100000	Processor status register (PS)		000??0001??
Timer B1 mode register	(5C <sub>16</sub> ) <sup>***</sup>	001XXXX000	Program bank register (PG)		00 <sub>16</sub>
Timer B2 mode register	(5D <sub>16</sub> ) <sup>***</sup>	001XXXX000	Program counter (PC <sub>H</sub> )		Content of FFFF <sub>16</sub>
Processor mode register 0	(5E <sub>16</sub> ) <sup>***</sup>	00 <sub>16</sub>	Program counter (PC <sub>L</sub> )		Content of FFFE <sub>16</sub>
Processor mode register 1	(5F <sub>16</sub> ) <sup>***</sup>	XXXXXXXXXX0	Direct page register (DPR)		0000 <sub>16</sub>
Watchdog timer register	(60 <sub>16</sub> ) <sup>***</sup>	FFF <sub>16</sub>	Data bank register (DT)		00 <sub>16</sub>

Contents of other registers and RAM are undefined during reset. Initialize them by software.

Fig. 3 Microcomputer internal status during reset

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**MITSUBISHI MICROCOMPUTERS**  
**M37733EHLXXXHP**

PROM VERSION OF M37733MHLXXXHP

**EPROM MODE**

The M37733EHLXXXHP features an EPROM mode in addition to its normal modes. When the RESET signal level is "L", the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 5 shows the pin connections in the EPROM mode.

The EPROM mode is the 1M mode for the EPROM that is equivalent to the M5M27C101K.

When in the EPROM mode, ports P0, P1, P2, P30, P50, P51, P52, CNVss and BYTE are used for the EPROM (equivalent to the

M5M27C101K). When in this mode, the built-in PROM can be programmed or read from using these pins in the same way as with the M5M27C101K.

This chip does not have Device Identifier Mode, so that set the corresponding program algorithm. The program area should specify address 0100016 – 1FFFF16.

Connect the clock which is either ceramic resonator or external clock to XIN pin and XOUT pin.

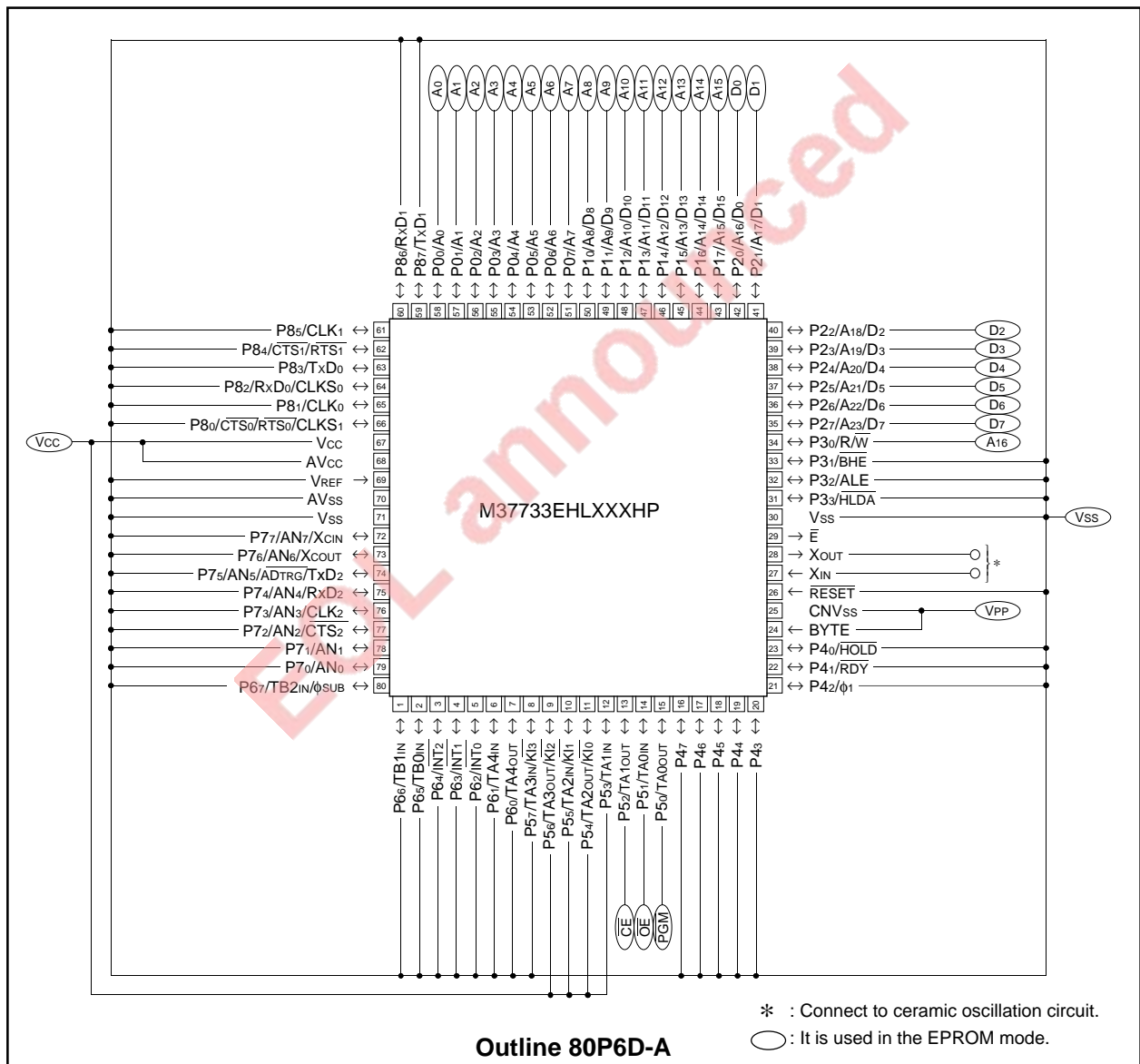


Fig. 5 Pin connection in EPROM mode

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**M37733EHLXXXHP**

PROM VERSION OF M37733MHLXXXHP

Table 1 Pin function in EPROM mode

	M37733EHLXXXHP	M5M27C101K
V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>
V <sub>PP</sub>	CNV <sub>SS</sub> , BYTE	V <sub>PP</sub>
V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>
Address input	Ports P0, P1, P30	A0 – A16
Data I/O	Port P2	D0 – D7
$\overline{\text{CE}}$	P52	$\overline{\text{CE}}$
$\overline{\text{OE}}$	P51	$\overline{\text{OE}}$
PGM	P50	PGM

**EOL announced**

**FUNCTION IN EPROM MODE**  
**1M mode (equivalent to the M5M27C101K)**

**Reading**

To read the EPROM, set the  $\overline{CE}$  and  $\overline{OE}$  pins to a "L" level. Input the address of the data (A0 – A16) to be read, and the data will be output to the I/O pins D0 – D7. The data I/O pins will be floating when either the  $\overline{CE}$  or  $\overline{OE}$  pins are in the "H" state.

**Programming**

Programming must be performed in 8 bits by a byte program. To program to the EPROM, set the  $\overline{CE}$  pin to a "L" level and the  $\overline{OE}$  pin to a "H" level. The CPU will enter the programming mode when 12.5 V is applied to the VPP pin. The address to be programmed to is selected with pins A0 – A16, and the data to be programmed is input to pins D0 – D7. Set the  $\overline{PGM}$  pin to a "L" level to being programming.

**Programming operation**

To program the M37733EHLXXXHP, first set VCC = 6 V, VPP = 12.5 V, and set the address to 0100016. Apply a 0.2 ms programming pulse, check that the data can be read, and if it cannot be read OK, repeat the procedure, applying a 0.2 ms programming pulse and checking that the data can be read until it can be read OK. Record the accumulated number of pulse applied (X) before the data can be read OK, and then write the data again, applying a further once this number of pulses (0.2 X X ms).

When this series of programming operations is complete, increment the address, and continue to repeat the procedure above until the last address has been reached.

Finally, when all addresses have been programmed, read with VCC = VPP = 5 V (or VCC = VPP = 5.5 V).

Table 2. I/O signal in each mode

Mode	Pin					
	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	VPP	VCC	Data I/O
Read-out	VIL	VIL	X	5 V	5 V	Output
Output	VIL	VIH	X	5 V	5 V	Floating
Disable	VIH	X	X	5 V	5 V	Floating
Programming	VIL	VIH	VIL	12.5 V	6 V	Input
Programming Verify	VIL	VIL	VIH	12.5 V	6 V	Output
Program Disable	VIH	VIH	VIH	12.5 V	6 V	Floating

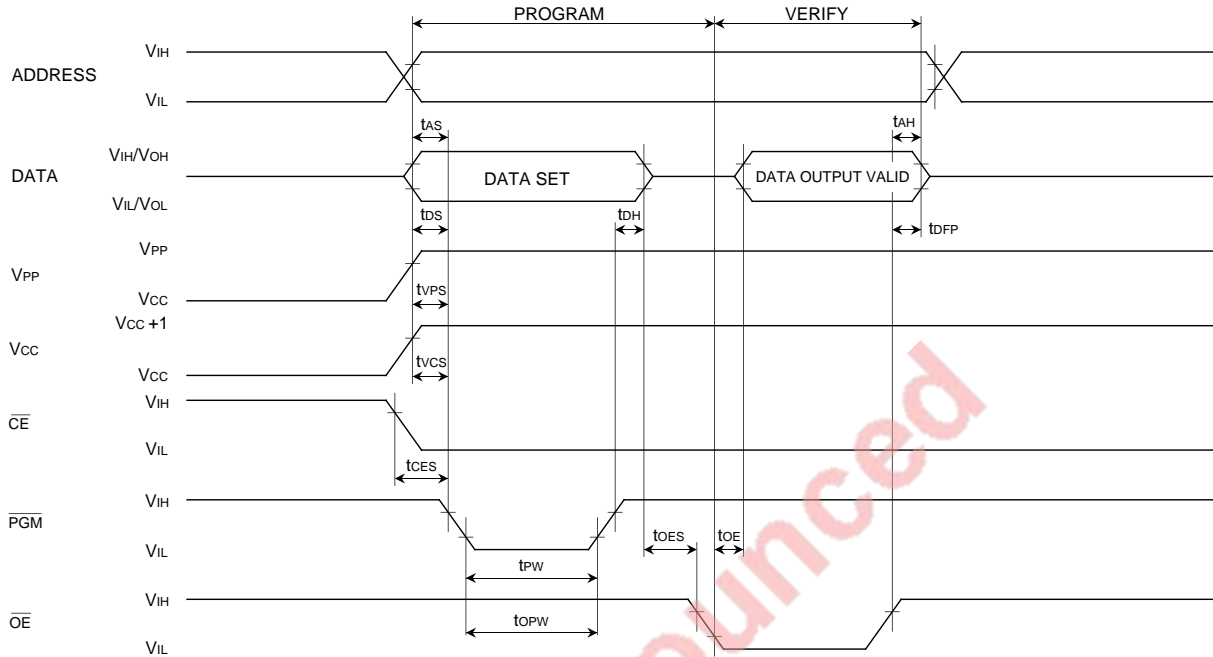
**Note 1** : An X indicates either VIL or VIH.

**Programming operation (equivalent to the M5M27C101K)**

AC ELECTRICAL CHARACTERISTICS (Ta = 25 ± 5 °C, VCC = 6 V ± 0.25 V, VPP = 12.5 ± 0.3 V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
tAS	Address setup time		2			μs
tOES	$\overline{OE}$ setup time		2			μs
tDS	Data setup time		2			μs
tAH	Address hold time		0			μs
tDH	Data hold time		2			μs
tDFP	Output enable to output float delay		0		130	ns
tVCS	VCC setup time		2			μs
tVPS	VPP setup time		2			μs
tPW	$\overline{PGM}$ pulse width		0.19	0.2	0.21	ms
tOPW	$\overline{PGM}$ over program pulse width		0.19		5.25	ms
tCES	$\overline{CE}$ setup time		2			μs
tOE	Data valid from $\overline{OE}$				150	ns

**AC waveforms**



Test conditions for A.C. characteristics

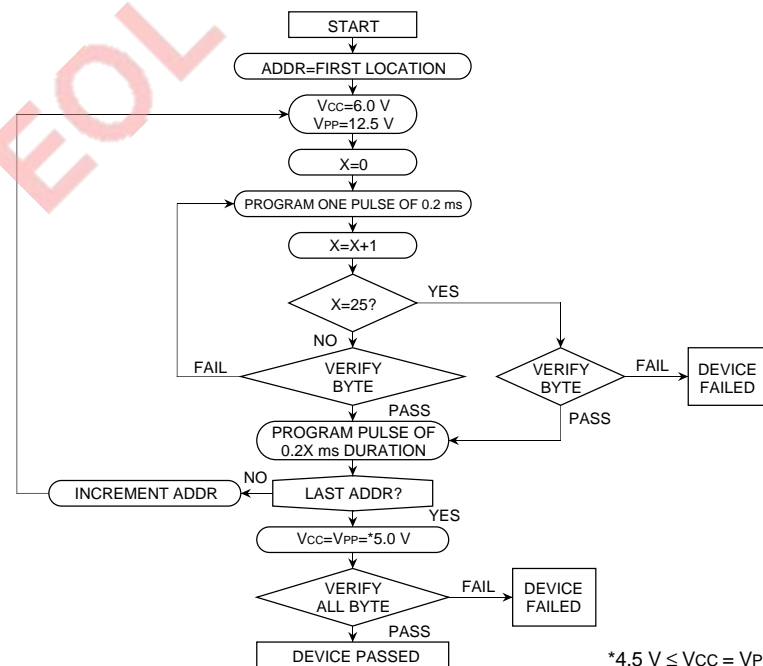
Input voltage :  $V_{IL} = 0.45 \text{ V}$ ,  $V_{IH} = 2.4 \text{ V}$

Input rise and fall times (10% – 90%) :  $\leq 20 \text{ ns}$

Reference voltage at timing measurement : Input, Output

"L" = 0.8 V, "H" = 2 V

**Programming algorithm flow chart**

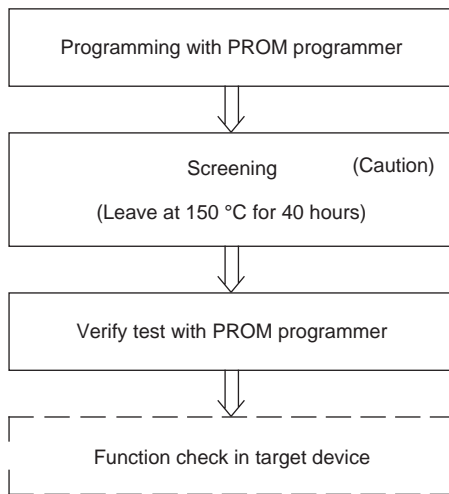


\*4.5 V ≤ VCC = VPP ≤ 5.5 V

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### SAFETY INSTRUCTIONS

- (1) A high voltage is used for programming. Take care that over-voltage is not applied. Take care especially at power on.
- (2) The programmable M37733EHLHP that is shipped in blank is also provided. For the M37733EHLHP, Mitsubishi Electric corp. does not perform PROM programming test and screening following the assembly processes. To improve reliability after programming, performing programming and test according to the flow below before use is recommended.



Caution : Never expose to 150 °C exceeding 100 hours.

### ADDRESSING MODES

The M37733EHLXXXHP has 28 powerful addressing modes. Refer to the "7700 Family Software Manual" for the details.

### MACHINE INSTRUCTION LIST

The M37733EHLXXXHP has 103 machine instructions. Refer to the "7700 Family Software Manual" for the details.

### DATA REQUIRED FOR PROM ORDERING

Please send the following data for writing to PROM.

- (1) M37733EHLXXXHP writing to PROM order confirmation form
- (2) 80P6D, 80P6Q mark specification form
- (3) ROM data (EPROM 3 sets)

**EOL announced**

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>cc</sub>	Power source voltage		-0.3 to +7	V
AV <sub>cc</sub>	Analog power source voltage		-0.3 to +7	V
V <sub>i</sub>	Input voltage RESET, CNV <sub>ss</sub> , BYTE		-0.3 to +12 (Note)	V
V <sub>i</sub>	Input voltage P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, V <sub>REF</sub> , X <sub>IN</sub>		-0.3 to V <sub>cc</sub> + 0.3	V
V <sub>o</sub>	Output voltage P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, X <sub>OUT</sub> , $\bar{E}$		-0.3 to V <sub>cc</sub> + 0.3	V
P <sub>d</sub>	Power dissipation	T <sub>a</sub> = 25 °C	200	mW
T <sub>opr</sub>	Operating temperature		-40 to +85	°C
T <sub>stg</sub>	Storage temperature		-65 to +150	°C

**Note.** When the EPROM is programmed, input voltage of pins CNV<sub>ss</sub> and BYTE is 13 V respectively.

**RECOMMENDED OPERATING CONDITIONS** (V<sub>cc</sub> = 2.7 – 5.5 V, T<sub>a</sub> = -40 to +85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V <sub>cc</sub>	Power source voltage	f(X <sub>IN</sub> ) : Operating	2.7	5.5	V
		f(X <sub>IN</sub> ) : Stopped, f(X <sub>CIN</sub> ) = 32.768 kHz	2.7	5.5	
AV <sub>cc</sub>	Analog power source voltage		V <sub>cc</sub>		V
V <sub>ss</sub>	Power source voltage		0		V
AV <sub>ss</sub>	Analog power source voltage		0		V
V <sub>IH</sub>	High-level input voltage P00 – P07, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, X <sub>IN</sub> , RESET, CNV <sub>ss</sub> , BYTE, X <sub>CIN</sub> (Note 3)	0.8 V <sub>cc</sub>		V <sub>cc</sub>	V
V <sub>IH</sub>	High-level input voltage P10 – P17, P20 – P27 (in single-chip mode)	0.8 V <sub>cc</sub>		V <sub>cc</sub>	V
V <sub>IH</sub>	High-level input voltage P10 – P17, P20 – P27 (in memory expansion mode and microprocessor mode)	0.5 V <sub>cc</sub>		V <sub>cc</sub>	V
V <sub>IL</sub>	Low-level input voltage P00 – P07, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, X <sub>IN</sub> , RESET, CNV <sub>ss</sub> , BYTE, X <sub>CIN</sub> (Note 3)	0		0.2V <sub>cc</sub>	V
V <sub>IL</sub>	Low-level input voltage P10 – P17, P20 – P27 (in single-chip mode)	0		0.2V <sub>cc</sub>	V
V <sub>IL</sub>	Low-level input voltage P10 – P17, P20 – P27 (in memory expansion mode and microprocessor mode)	0		0.16V <sub>cc</sub>	V
I <sub>OH(peak)</sub>	High-level peak output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87			-10	mA
I <sub>OH(avg)</sub>	High-level average output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87			-5	mA
I <sub>OL(peak)</sub>	Low-level peak output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P43, P54 – P57, P60 – P67, P70 – P77, P80 – P87			10	mA
I <sub>OL(peak)</sub>	Low-level peak output current P44 – P47, P50 – P53			16	mA
I <sub>OL(avg)</sub>	Low-level average output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P43, P54 – P57, P60 – P67, P70 – P77, P80 – P87			5	mA
I <sub>OL(avg)</sub>	Low-level average output current P44 – P47, P50 – P53			12	mA
f(X <sub>IN</sub> )	Main-clock oscillation frequency (Note 4)			12	MHz
f(X <sub>CIN</sub> )	Sub-clock oscillation frequency		32.768	50	kHz

- Notes**
1. Average output current is the average value of a 100 ms interval.
  2. The sum of I<sub>OL(peak)</sub> for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I<sub>OH(peak)</sub> for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I<sub>OL(peak)</sub> for ports P4, P5, P6, and P7 must be 100 mA or less, and the sum of I<sub>OH(peak)</sub> for ports P4, P5, P6, and P7 must be 80 mA or less.
  3. Limits V<sub>IH</sub> and V<sub>IL</sub> for X<sub>CIN</sub> are applied when the sub clock external input selection bit = "1".
  4. The maximum value of f(X<sub>IN</sub>) = 6 MHz when the main clock division selection bit = "1".

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -40$  to  $+85\text{ }^\circ\text{C}$ ,  $f(X_{IN}) = 12\text{ MHz}$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
VOH	High-level output voltage P00 – P07, P10 – P17, P20 – P27, P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87	VCC = 5 V, IOH = –10 mA	3			V	
		VCC = 3 V, IOH = –1 mA	2.5				
VOH	High-level output voltage P00 – P07, P10 – P17, P20 – P27, P33	VCC = 5 V, IOH = –400 $\mu\text{A}$	4.7			V	
VOH	High-level output voltage P30 – P32	VCC = 5 V, IOH = –10 mA	3.1			V	
		VCC = 5 V, IOH = –400 $\mu\text{A}$	4.8				
		VCC = 3 V, IOH = –1 mA	2.6				
VOH	High-level output voltage $\bar{E}$	VCC = 5 V, IOH = –10 mA	3.4			V	
		VCC = 5 V, IOH = –400 $\mu\text{A}$	4.8				
		VCC = 3 V, IOH = –1 mA	2.6				
VOL	Low-level output voltage P00 – P07, P10 – P17, P20 – P27, P33, P40 – P43, P54 – P57, P60 – P67, P70 – P77, P80 – P87	VCC = 5 V, IOL = 10 mA			2	V	
		VCC = 3 V, IOL = 1 mA			0.5		
VOL	Low-level output voltage P44 – P47, P50 – P53	VCC = 5 V, IOL = 16 mA			1.8	V	
		VCC = 3 V, IOL = 10 mA			1.5		
VOL	Low-level output voltage P00 – P07, P10 – P17, P20 – P27, P33	VCC = 5 V, IOL = 2 mA			0.45	V	
VOL	Low-level output voltage P30 – P32	VCC = 5 V, IOL = 10 mA			1.9	V	
		VCC = 5 V, IOL = 2 mA			0.43		
		VCC = 3 V, IOL = 1 mA			0.4		
VOL	Low-level output voltage $\bar{E}$	VCC = 5 V, IOL = 10 mA			1.6	V	
		VCC = 5 V, IOL = 2 mA			0.4		
		VCC = 3 V, IOL = 1 mA			0.4		
VT+ – VT–	Hysteresis HOLD, RDY, TA0IN – TA4IN, TB0IN – TB2IN, INT0 – INT2, ADTRG, CTS0, CTS1, CTS2, CLK0, CLK1, CLK2, KI0 – KI3	VCC = 5 V	0.4		1	V	
		VCC = 3 V	0.1		0.7		
VT+ – VT–	Hysteresis $\bar{\text{RESET}}$	VCC = 5 V	0.2		0.5	V	
		VCC = 3 V	0.1		0.4		
VT+ – VT–	Hysteresis XIN	VCC = 5 V	0.1		0.4	V	
		VCC = 3 V	0.06		0.26		
VT+ – VT–	Hysteresis XCIN (When external clock is input)	VCC = 5 V	0.1		0.4	V	
		VCC = 3 V	0.06		0.26		
IIH	High-level input current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, XIN, RESET, CNVss, BYTE	VCC = 5 V, VI = 5 V			5	$\mu\text{A}$	
		VCC = 3 V, VI = 3 V			4		
IIL	Low-level input current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P53, P60, P61, P65 – P67, P70 – P77, P80 – P87, XIN, RESET, CNVss, BYTE	VCC = 5 V, VI = 0 V			–5	$\mu\text{A}$	
		VCC = 3 V, VI = 0 V			–4		
IIL	Low-level input current P54 – P57, P62 – P64	VI = 0 V, without a pull-up transistor	VCC = 5 V			–5	$\mu\text{A}$
			VCC = 3 V			–4	
		VI = 0 V, with a pull-up transistor	VCC = 5 V	–0.25	–0.5	–1.0	mA
			VCC = 3 V	–0.08	–0.18	–0.35	
VRAM	RAM hold voltage	When clock is stopped.	2			V	



**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ to }+85\text{ }^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
I <sub>CC</sub>	Power source current	When single-chip mode, output pins are open, and other pins are V <sub>SS</sub> .	V <sub>CC</sub> = 5 V, f(X <sub>IN</sub> ) = 12 MHz (square waveform), f(f <sub>2</sub> ) = 6 MHz, f(X <sub>CIN</sub> ) = 32.768 kHz, in operating (Note 1)		4.5	9	mA
			V <sub>CC</sub> = 3 V, f(X <sub>IN</sub> ) = 12 MHz (square waveform), f(f <sub>2</sub> ) = 6 MHz, f(X <sub>CIN</sub> ) = 32.768 kHz, in operating (Note 1)		3	6	mA
			V <sub>CC</sub> = 3 V, f(X <sub>IN</sub> ) = 12 MHz (square waveform), f(f <sub>2</sub> ) = 0.75 MHz, f(X <sub>CIN</sub> ) : Stopped, in operating		0.4	0.8	mA
			V <sub>CC</sub> = 3 V, f(X <sub>IN</sub> ) = 12 MHz (square waveform), f(X <sub>CIN</sub> ) = 32.768 kHz, when a WIT instruction is executed (Note 2)		6	12	μA
			V <sub>CC</sub> = 3 V, f(X <sub>IN</sub> ) : Stopped, f(X <sub>CIN</sub> ) = 32.768 kHz, in operating (Note 3)		30	60	μA
			V <sub>CC</sub> = 3 V, f(X <sub>IN</sub> ) : Stopped, f(X <sub>CIN</sub> ) = 32.768 kHz, when a WIT instruction is executed (Note 4)		3	6	μA
			T <sub>a</sub> = 25 °C, when clock is stopped			1	μA
			T <sub>a</sub> = 85 °C, when clock is stopped			20	μA

- Notes 1.** This applies when the main clock external input selection bit = "1", the main clock division selection bit = "0", and the signal output stop bit = "1".
- 2.** This applies when the main clock external input selection bit = "1" and the system clock stop bit at wait state = "1".
- 3.** This applies when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.
- 4.** This applies when the X<sub>COUT</sub> drivability selection bit = "0" and the system clock stop bit at wait state = "1".

**A-D CONVERTER CHARACTERISTICS**

(V<sub>CC</sub> = AV<sub>CC</sub> = 5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V, T<sub>a</sub> = -40 to +85 °C, f(X<sub>IN</sub>) = 12 MHz, unless otherwise noted (Note))

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	V <sub>REF</sub> = V <sub>CC</sub>			10	Bits
—	Absolute accuracy	V <sub>REF</sub> = V <sub>CC</sub>			± 3	LSB
RLADDER	Ladder resistance	V <sub>REF</sub> = V <sub>CC</sub>	10		25	kΩ
t <sub>CONV</sub>	Conversion time		19.6			μs
V <sub>REF</sub>	Reference voltage		2.7		V <sub>CC</sub>	V
V <sub>IA</sub>	Analog input voltage		0		V <sub>REF</sub>	V

**Note.** This applies when the main clock division selection bit = "0" and f(f<sub>2</sub>) = 6 MHz.

**TIMING REQUIREMENTS** ( $V_{CC} = 2.7 - 5.5 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ,  $T_a = -40 \text{ to } +85 \text{ }^\circ\text{C}$ ,  $f(X_{IN}) = 12 \text{ MHz}$ , unless otherwise noted (Note 1))

**Notes 1.** This applies when the main clock division selection bit = "0" and  $f(f_2) = 6 \text{ MHz}$ .

**2.** Input signal's rise/fall time must be 100 ns or less, unless otherwise noted.

**External clock input**

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_c$	External clock input cycle time (Note 1)	83		ns
$t_{w(H)}$	External clock input high-level pulse width (Note 2)	33		ns
$t_{w(L)}$	External clock input low-level pulse width (Note 2)	33		ns
$t_r$	External clock rise time		15	ns
$t_f$	External clock fall time		15	ns

**Notes 1.** When the main clock division selection bit = "1", the minimum value of  $t_c = 166 \text{ ns}$ .

**2.** When the main clock division selection bit = "1", values of  $t_{w(H)} / t_c$  and  $t_{w(L)} / t_c$  must be set to values from 0.45 through 0.55.

**Single-chip mode**

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su}(P0D-E)$	Port P0 input setup time	200		ns
$t_{su}(P1D-E)$	Port P1 input setup time	200		ns
$t_{su}(P2D-E)$	Port P2 input setup time	200		ns
$t_{su}(P3D-E)$	Port P3 input setup time	200		ns
$t_{su}(P4D-E)$	Port P4 input setup time	200		ns
$t_{su}(P5D-E)$	Port P5 input setup time	200		ns
$t_{su}(P6D-E)$	Port P6 input setup time	200		ns
$t_{su}(P7D-E)$	Port P7 input setup time	200		ns
$t_{su}(P8D-E)$	Port P8 input setup time	200		ns
$t_h(E-P0D)$	Port P0 input hold time	0		ns
$t_h(E-P1D)$	Port P1 input hold time	0		ns
$t_h(E-P2D)$	Port P2 input hold time	0		ns
$t_h(E-P3D)$	Port P3 input hold time	0		ns
$t_h(E-P4D)$	Port P4 input hold time	0		ns
$t_h(E-P5D)$	Port P5 input hold time	0		ns
$t_h(E-P6D)$	Port P6 input hold time	0		ns
$t_h(E-P7D)$	Port P7 input hold time	0		ns
$t_h(E-P8D)$	Port P8 input hold time	0		ns

**Memory expansion mode and microprocessor mode**

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su}(D-E)$	Data input setup time	50		ns
$t_{su}(RDY- 1)$	RDY input setup time	80		ns
$t_{su}(HOLD- 1)$	HOLD input setup time	80		ns
$t_h(E-D)$	Data input hold time	0		ns
$t_h( 1-RDY)$	RDY input hold time	0		ns
$t_h( 1-HOLD)$	HOLD input hold time	0		ns

**Timer A input** (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t <sub>c</sub> (TA)	TAiIN input cycle time	250		ns
t <sub>w</sub> (TAH)	TAiIN input high-level pulse width	125		ns
t <sub>w</sub> (TAL)	TAiIN input low-level pulse width	125		ns

**Timer A input** (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t <sub>c</sub> (TA)	TAiIN input cycle time (Note)	666		ns
t <sub>w</sub> (TAH)	TAiIN input high-level pulse width (Note)	333		ns
t <sub>w</sub> (TAL)	TAiIN input low-level pulse width (Note)	333		ns

**Note.** Limits change depending on f(X<sub>IN</sub>). Refer to "DATA FORMULAS" on page 20.

**Timer A input** (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t <sub>c</sub> (TA)	TAiIN input cycle time (Note)	666		ns
t <sub>w</sub> (TAH)	TAiIN input high-level pulse width	166		ns
t <sub>w</sub> (TAL)	TAiIN input low-level pulse width	166		ns

**Note.** Limits change depending on f(X<sub>IN</sub>). Refer to "DATA FORMULAS" on page 20.

**Timer A input** (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t <sub>w</sub> (TAH)	TAiIN input high-level pulse width	166		ns
t <sub>w</sub> (TAL)	TAiIN input low-level pulse width	166		ns

**Timer A input** (Up-down input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t <sub>c</sub> (UP)	TAiOUT input cycle time	3333		ns
t <sub>w</sub> (UPH)	TAiOUT input high-level pulse width	1666		ns
t <sub>w</sub> (UPL)	TAiOUT input low-level pulse width	1666		ns
t <sub>su</sub> (UP-T <sub>IN</sub> )	TAiOUT input setup time	666		ns
t <sub>h</sub> (T <sub>IN</sub> -UP)	TAiOUT input hold time	666		ns

**Timer A input** (Two-phase pulse input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t <sub>c</sub> (TA)	TAjIN input cycle time	2000		ns
t <sub>su</sub> (TAjIN-TAjOUT)	TAjIN input setup time	500		ns
t <sub>su</sub> (TAjOUT-TAjIN)	TAjOUT input setup time	500		ns

**Timer B input** (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t <sub>c</sub> (TB)	TBiIn input cycle time (one edge count)	250		ns
t <sub>w</sub> (TBH)	TBiIn input high-level pulse width (one edge count)	125		ns
t <sub>w</sub> (TBL)	TBiIn input low-level pulse width (one edge count)	125		ns
t <sub>c</sub> (TB)	TBiIn input cycle time (both edges count)	500		ns
t <sub>w</sub> (TBH)	TBiIn input high-level pulse width (both edges count)	250		ns
t <sub>w</sub> (TBL)	TBiIn input low-level pulse width (both edges count)	250		ns

**Timer B input** (Pulse period measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t <sub>c</sub> (TB)	TBiIn input cycle time (Note)	666		ns
t <sub>w</sub> (TBH)	TBiIn input high-level pulse width (Note)	333		ns
t <sub>w</sub> (TBL)	TBiIn input low-level pulse width (Note)	333		ns

**Note.** Limits change depending on f(X<sub>IN</sub>). Refer to "DATA FORMULAS" on page 20.

**Timer B input** (Pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t <sub>c</sub> (TB)	TBiIn input cycle time (Note)	666		ns
t <sub>w</sub> (TBH)	TBiIn input high-level pulse width (Note)	333		ns
t <sub>w</sub> (TBL)	TBiIn input low-level pulse width (Note)	333		ns

**Note.** Limits change depending on f(X<sub>IN</sub>). Refer to "DATA FORMULAS" on page 20.

**A-D trigger input**

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t <sub>c</sub> (AD)	AD <sub>TRG</sub> input cycle time (minimum allowable trigger)	1333		ns
t <sub>w</sub> (ADL)	AD <sub>TRG</sub> input low-level pulse width	166		ns

**Serial I/O**

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t <sub>c</sub> (CK)	CLK <sub>i</sub> input cycle time	333		ns
t <sub>w</sub> (CKH)	CLK <sub>i</sub> input high-level pulse width	166		ns
t <sub>w</sub> (CKL)	CLK <sub>i</sub> input low-level pulse width	166		ns
t <sub>d</sub> (C-Q)	TxD <sub>i</sub> output delay time		100	ns
t <sub>h</sub> (C-Q)	TxD <sub>i</sub> hold time	0		ns
t <sub>su</sub> (D-C)	RxD <sub>i</sub> input setup time	65		ns
t <sub>h</sub> (C-D)	RxD <sub>i</sub> input hold time	75		ns

**External interrupt INT<sub>i</sub> input, key input interrupt KLi input**

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t <sub>w</sub> (INH)	INT <sub>i</sub> input high-level pulse width	250		ns
t <sub>w</sub> (INL)	INT <sub>i</sub> input low-level pulse width	250		ns
t <sub>w</sub> (KIL)	KLi input low-level pulse width	250		ns

**DATA FORMULAS**

**Timer A input** (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIn input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAH)}$	TAiIn input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAL)}$	TAiIn input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

**Timer A input** (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIn input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns

**Timer B input** (In pulse period measurement mode or pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIn input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBH)}$	TBiIn input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBL)}$	TBiIn input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

**Note.**  $f(f_2)$  represents the clock  $f_2$  frequency.

For the relation to the main clock and sub clock, refer to Table 9 in data sheet "M37733MHBXXXFP".

**SWITCHING CHARACTERISTICS**

(V<sub>CC</sub> = 2.7 – 5.5 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = –40 to +85°C, f(X<sub>IN</sub>) = 12 MHz, unless otherwise noted (Note))

**Single-chip mode**

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
td(E–P0Q)	Port P0 data output delay time	Fig. 6		300	ns
td(E–P1Q)	Port P1 data output delay time			300	ns
td(E–P2Q)	Port P2 data output delay time			300	ns
td(E–P3Q)	Port P3 data output delay time			300	ns
td(E–P4Q)	Port P4 data output delay time			300	ns
td(E–P5Q)	Port P5 data output delay time			300	ns
td(E–P6Q)	Port P6 data output delay time			300	ns
td(E–P7Q)	Port P7 data output delay time			300	ns
td(E–P8Q)	Port P8 data output delay time			300	ns

**Note.** This applies when the main clock division selection bit = “0” and f(f<sub>2</sub>) = 6 MHz.

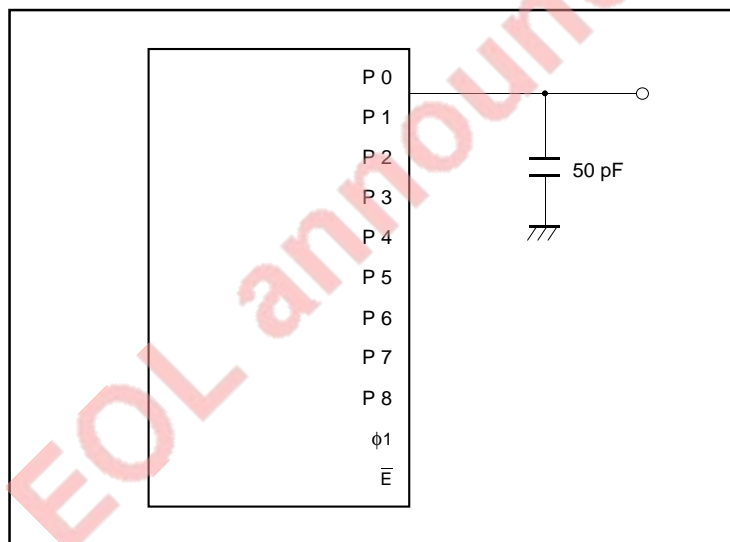


Fig. 6 Measuring circuit for ports P0 – P8 and φ<sub>1</sub>

**Memory expansion mode and microprocessor mode**

(V<sub>CC</sub> = 2.7 – 5.5 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = –40 to +85°C, f(X<sub>IN</sub>) = 12 MHz (Note 1), unless otherwise noted)

Symbol	Parameter	(Note 2) Wait mode	Test conditions	Limits		Unit
				Min.	Max.	
td(An–E)	Address output delay time	No wait	Fig. 6	20		ns
		Wait 1				
		Wait 0		182		ns
td(A–E)	Address output delay time	No wait		20		ns
		Wait 1				
		Wait 0		162		ns
th(E–An)	Address hold time			40		ns
tw(ALE)	ALE pulse width	No wait		40		ns
		Wait 1				
		Wait 0		123		ns
tsu(A–ALE)	Address output setup time	No wait		10		ns
		Wait 1				
		Wait 0	93		ns	
th(ALE–A)	Address hold time	No wait	9		ns	
		Wait 1				
		Wait 0	40		ns	
td(ALE–E)	ALE output delay time	No wait	4		ns	
		Wait 1				
		Wait 0	40		ns	
td(E–DQ)	Data output delay time			90	ns	
th(E–DQ)	Data hold time		40		ns	
tw(EL)	E pulse width	No wait	131		ns	
		Wait 1				
		Wait 0	298		ns	
tpxz(E–DZ)	Floating start delay time			10	ns	
tpzx(E–DZ)	Floating release delay time		53		ns	
td(BHE–E)	BHE output delay time	No wait	20		ns	
		Wait 1				
		Wait 0	182		ns	
td(R/W–E)	R/W output delay time	No wait	20		ns	
		Wait 1				
		Wait 0	182		ns	
th(E–BHE)	BHE hold time		33		ns	
th(E–R/W)	R/W hold time		33		ns	
td(E–φ <sub>1</sub> )	φ <sub>1</sub> output delay time		0	30	ns	
td(φ <sub>1</sub> –HLDA)	HLDA output delay time			120	ns	

**Notes 1.** This applies when the main clock division selection bit = "0" and f(f<sub>2</sub>) = 6 MHz.

**2.** No wait : Wait bit = "1".

Wait 1 : The external memory area is accessed with wait bit = "0" and wait selection bit = "1".

Wait 0 : The external memory area is accessed with wait bit = "0" and wait selection bit = "0".

**Memory expansion mode and microprocessor mode**

**Bus timing data formulas** ( $V_{CC} = 2.7 - 5.5 V$ ,  $V_{SS} = 0 V$ ,  $T_a = -40$  to  $+85$  °C,  $f(X_{IN}) = 12$  MHz (Max., Note 1), unless otherwise noted)

Symbol	Parameter	Wait mode	Limits		Unit
			Min.	Max.	
td(A $\bar{n}$ -E)	Address output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 63$		ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 68$		ns
td(A-E)	Address output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 63$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 88$		ns
th(E-A $\bar{n}$ )	Address hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
tw(ALE)	ALE pulse width	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
tsu(A-ALE)	Address output setup time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 73$		ns
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 73$		ns
th(ALE-A)	Address hold time	No wait	9		ns
		Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
td(ALE-E)	ALE output delay time	No wait	4		ns
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
td(E-DQ)	Data output delay time			90	ns
th(E-DQ)	Data hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
tw(EL)	$\bar{E}$ pulse width	No wait	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
		Wait 1	$\frac{4 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
tpxz(E-DZ)	Floating start delay time			10	ns
tpzx(E-DZ)	Floating release delay time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
td(BHE-E)	$\overline{BHE}$ output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 63$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 68$		ns
td(R/W-E)	$R/\overline{W}$ output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 63$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 68$		ns
th(E-BHE)	$\overline{BHE}$ hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 50$		ns
th(E-R/W)	$R/\overline{W}$ hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 50$		ns
td(E- $\phi_1$ )	$\phi_1$ output delay time		0	30	ns

**Notes 1.** This applies when the main-clock division selection bit = "0".

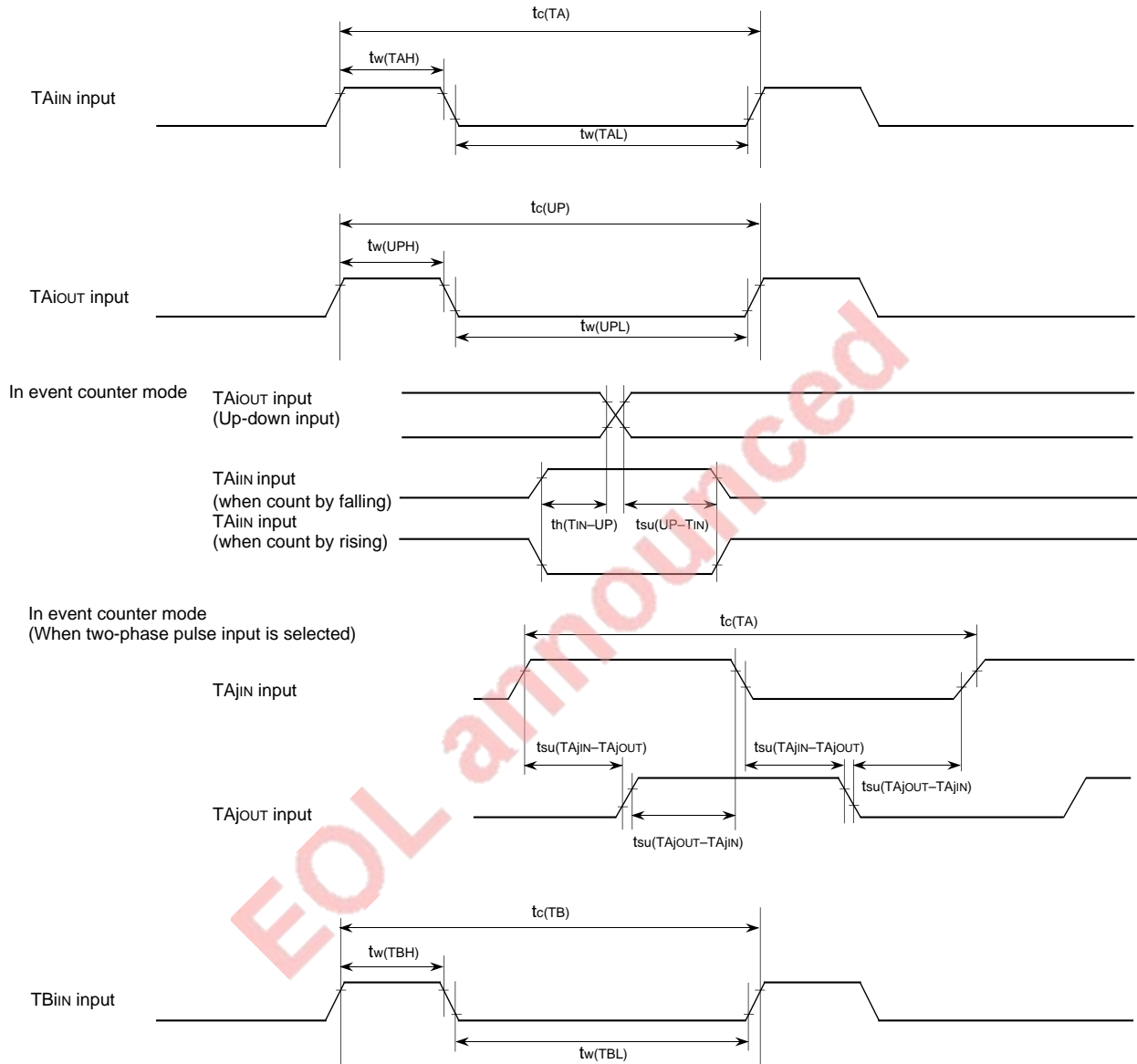
**2.**  $f(f_2)$  represents the clock  $f_2$  frequency.

For the relation to the main clock and sub clock, refer to Table 9 in data sheet "M37733MHBXXXFP".



**TIMING DIAGRAM**

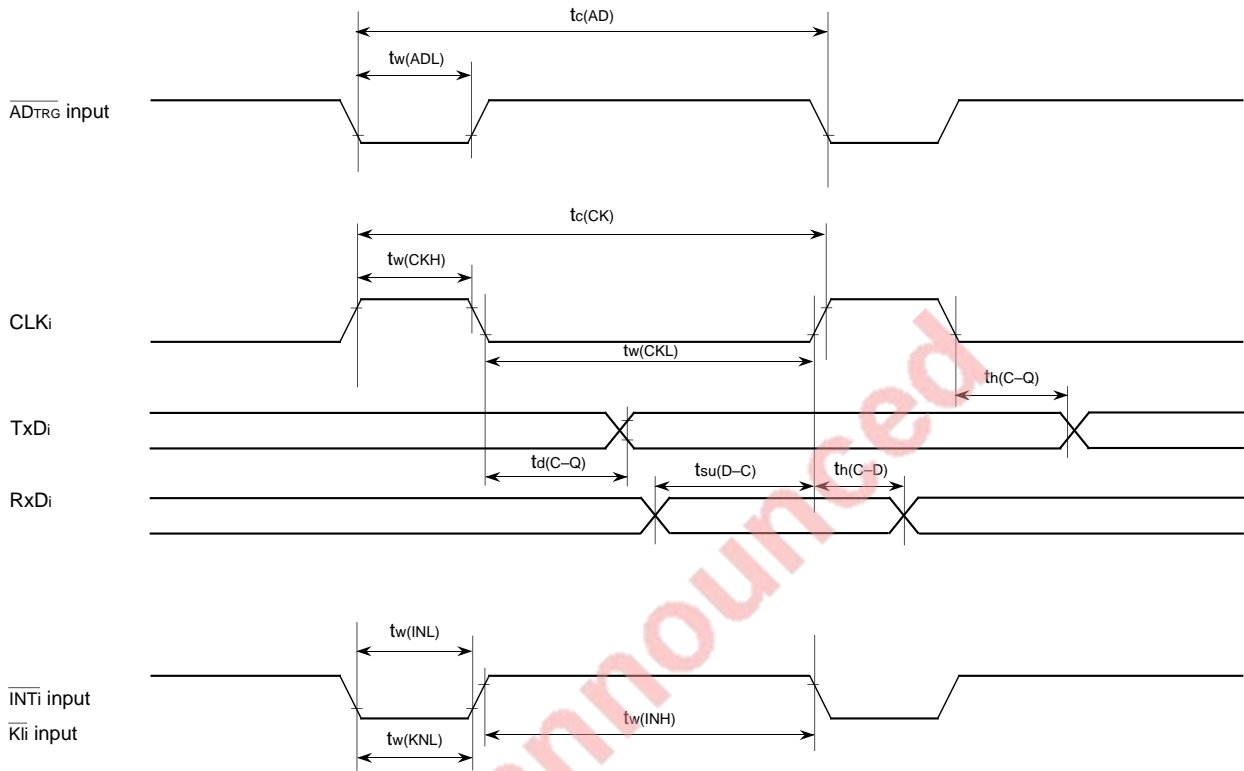




**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

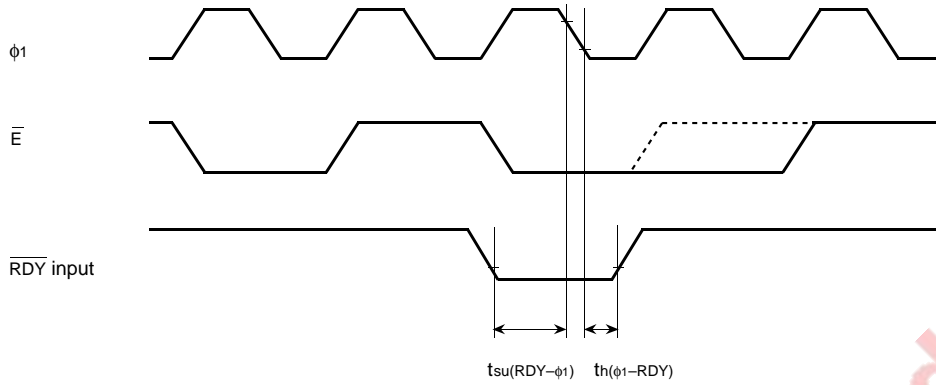
**mitsubishi MICROCOMPUTERS**  
**M37733EHLXXXHP**

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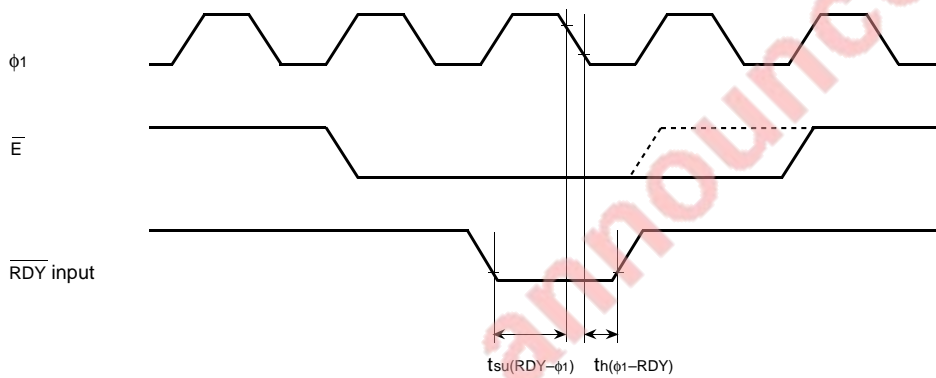


EOL announced

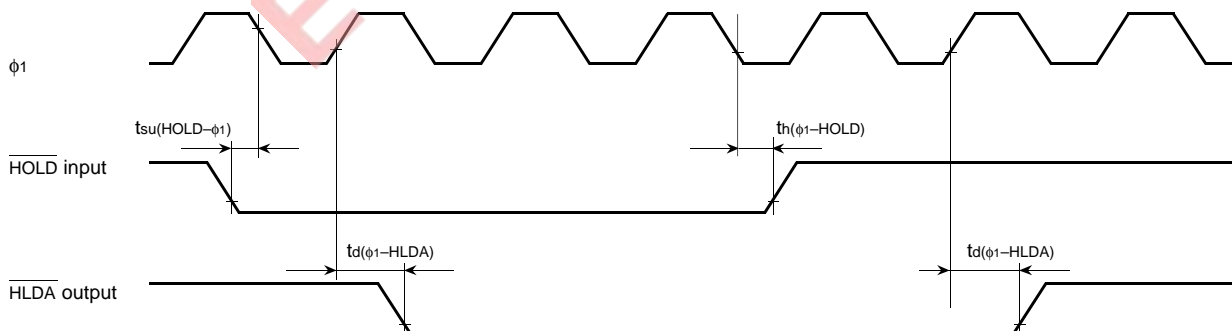
Memory expansion mode and microprocessor mode  
 (When wait bit = "1")



(When wait bit = "0")



(When wait bit = "1" or "0" in common)



Test conditions

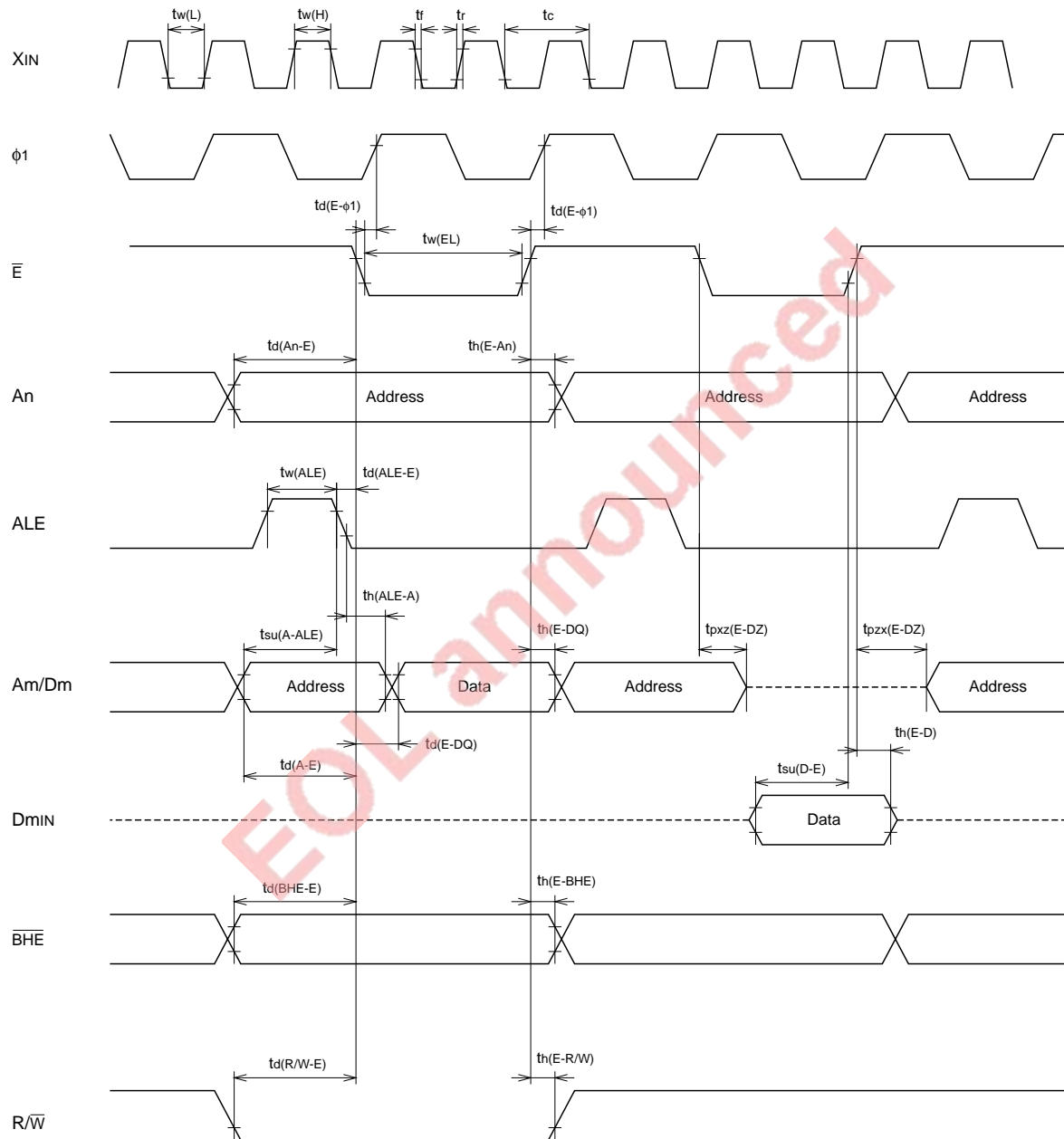
- $V_{CC} = 2.7 - 5.5 \text{ V}$
- Input timing voltage :  $V_{IL} = 0.2 V_{CC}$ ,  $V_{IH} = 0.8 V_{CC}$
- Output timing voltage :  $V_{OL} = 0.8 \text{ V}$ ,  $V_{OH} = 2.0 \text{ V}$

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

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Memory expansion mode and microprocessor mode  
 (No wait : When wait bit = "1")

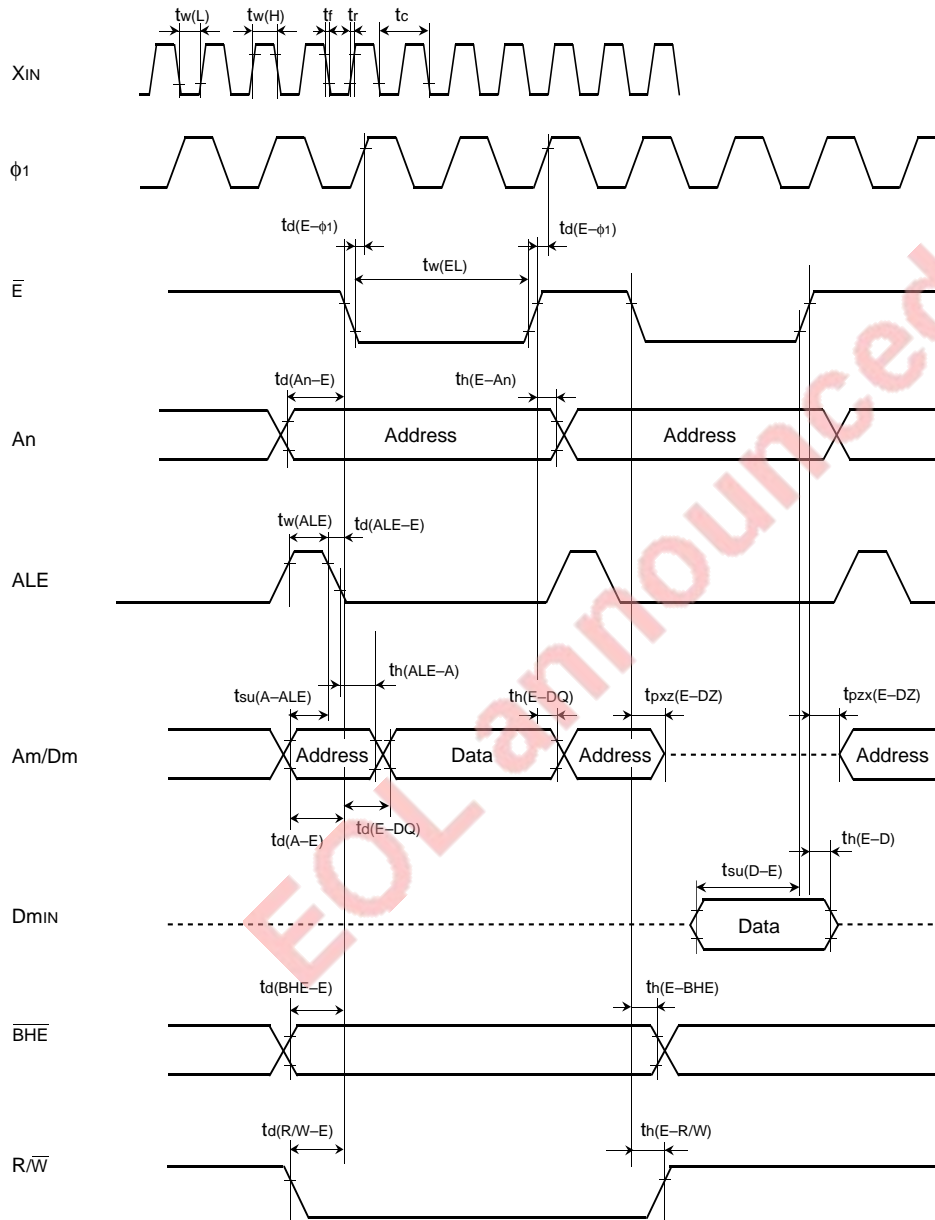


Test conditions

- $V_{CC} = 2.7 - 5.5 V$
- Output timing voltage :  $V_{OL} = 0.8 V$ ,  $V_{OH} = 2.0 V$
- Data input Dmin :  $V_{IL} = 0.16 V_{CC}$ ,  $V_{IH} = 0.5 V_{CC}$

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

Memory expansion mode and microprocessor mode  
 (Wait 1 : The external memory area is accessed when wait bit = "0" and wait selection bit = "1".)

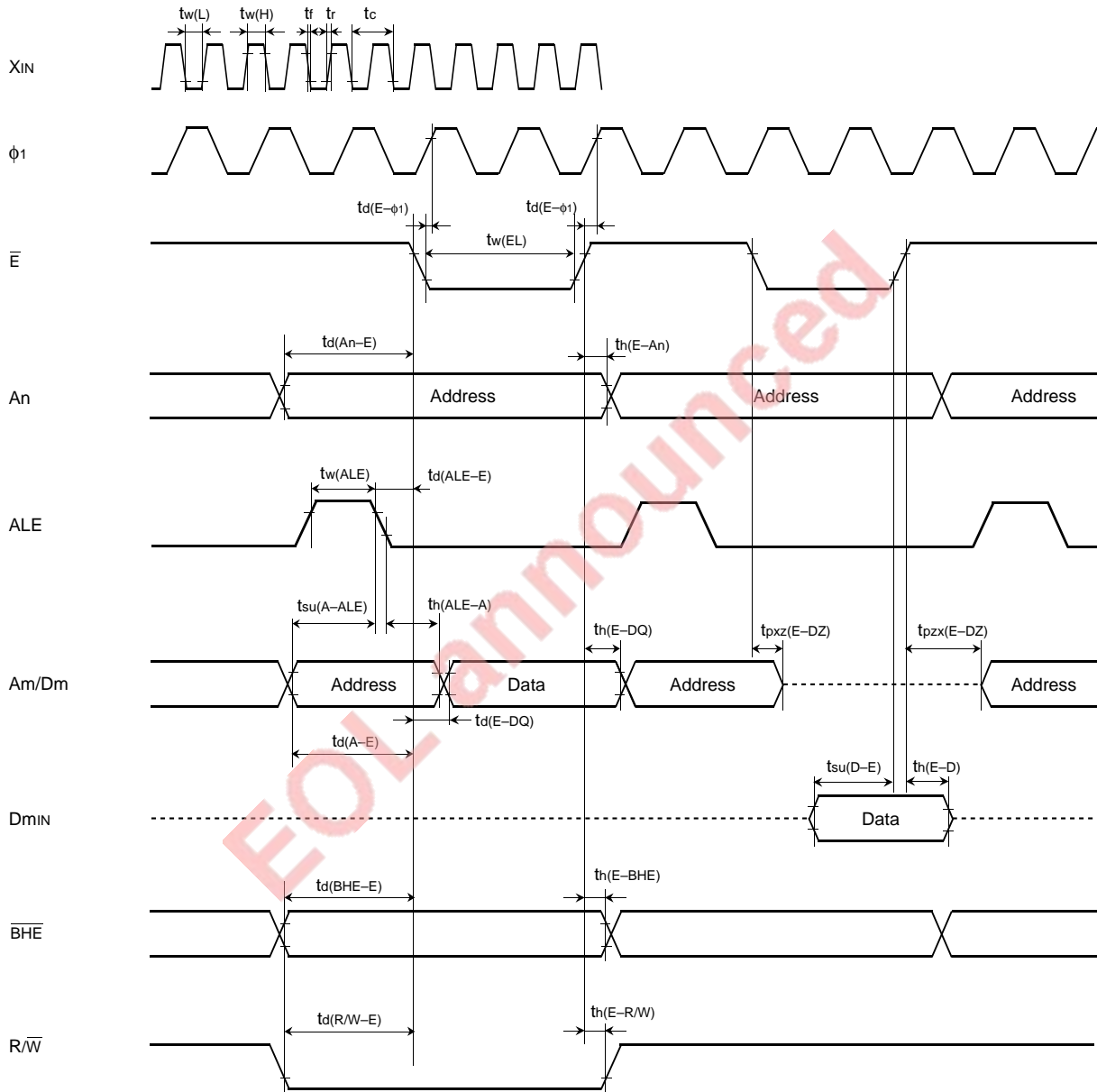


Test conditions

- $V_{CC} = 2.7 - 5.5 V$
- Output timing voltage :  $V_{OL} = 0.8 V$ ,  $V_{OH} = 2.0 V$
- Data input  $D_{min}$  :  $V_{IL} = 0.16 V_{CC}$ ,  $V_{IH} = 0.5 V_{CC}$

Memory expansion mode and microprocessor mode

(Wait 0 : The external memory area is accessed when wait bit = "0" and wait selection bit = "0".)



Test conditions

- $V_{CC} = 2.7 - 5.5 V$
- Output timing voltage :  $V_{OL} = 0.8 V, V_{OH} = 2.0 V$
- Data input  $D_{min}$  :  $V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}$

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

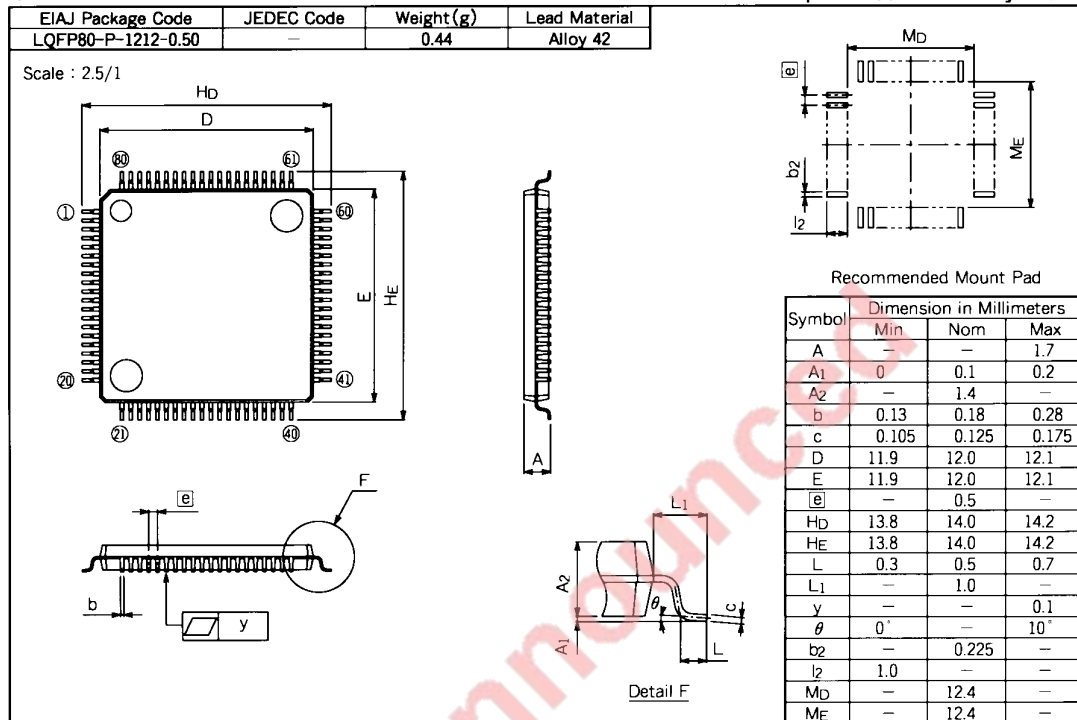
MITSUBISHI MICROCOMPUTERS  
**M37733EHLXXXHP**

PROM VERSION OF M37733MHLXXXHP

**PACKAGE OUTLINE**

**80P6D-A**

Plastic 80pin 12x12mm body LQFP





**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

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**M37733EHLXXXHP**

PROM VERSION OF M37733MHLXXXHP

GZZ-SH00-42B<68A0>

**7700 FAMILY WRITING TO PROM ORDER CONFIRMATION FORM**  
**SINGLE-CHIP 16-BIT MICROCOMPUTER**  
**M37733EHLXXXHP**  
**MITSUBISHI ELECTRIC**

ROM number	
------------	--

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ※

※	Customer	Company name	TEL ( )	Issuance signatures	Responsible officer	Supervisor
		Date issued	Date:			

※ 1. Confirmation

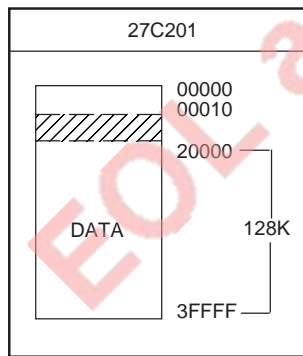
Specify the name of the product being ordered and the type of EPROMs submitted.  
 Three sets of EPROMs are required for each pattern.  
 If at least two of the three sets of EPROMs submitted contain the identical data, we will produce writing to PROM based on this data. We shall assume the responsibility for errors only if the written PROM data on the products we produce differ from this data.  
 Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas 

--	--	--	--

 (hexadecimal notation)

EPROM Type :



- (1) Set "FF<sub>16</sub>" in the shaded area.
  - (2) Address 0<sub>16</sub> to 0F<sub>16</sub> are the area for storing the data on model designation. This area must be written with the data shown below.
- Address and data are written in hexadecimal notation.

Address	Address		
4D	0	4C	8
33	1	FF	9
37	2	FF	A
37	3	FF	B
33	4	FF	C
33	5	FF	D
45	6	FF	E
48	7	FF	F

※ 2. Mark specification

Mark specification must be submitted using the correct form for the type of package being ordered fill out the appropriate 80P6D Mark Specification Form (for M37733EHLXXXHP) and attach to the Writing to PROM Order Confirmation Form.

※ 3. Comments

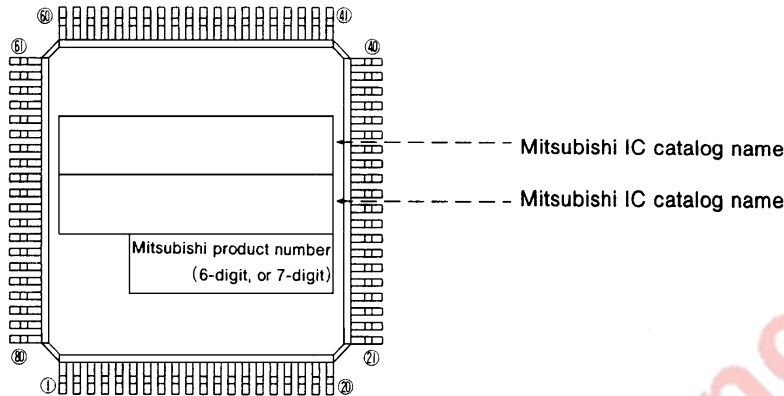
**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

**80P6S (80-PIN QFP) MARK SPECIFICATION FORM**  
**80P6D (80-PIN Fine-pitch QFP)**

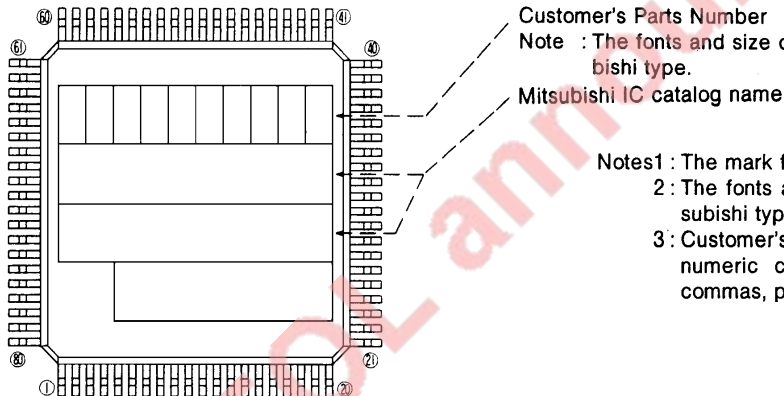
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

**A. Standard Mitsubishi Mark**



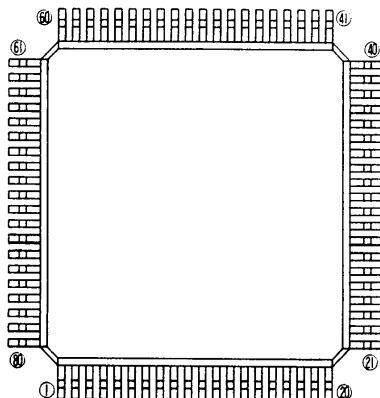
**B. Customer's Parts Number + Mitsubishi IC Catalog Name**



Customer's Parts Number  
 Note : The fonts and size of characters are standard Mitsubishi type.  
 Mitsubishi IC catalog name

- Notes1 : The mark field should be written right aligned.  
 2: The fonts and size of characters are standard Mitsubishi type.  
 3: Customer's parts number can be up to 10 alphanumeric characters for capital letters, hyphens, commas, periods and so on.

**C. Special Mark Required**



- Notes1 : If special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated technically as close as possible. Mitsubishi product number (6-digit, or 7-digit) and Mask ROM number (3-digit) are always marked for sorting the products.  
 2: If special character fonts (e.g., customer's trade mark logo) must be used in Special Mark, check the box below.  
 For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special character fonts required

**PRELIMINARY**

Notice: This is not a final specification.  
Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS

**M37733EHLXXXHP**

PROM VERSION OF M37733MHLXXXHP

**EOL announced**

## Renesas Technology Corp.

Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

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REVISION DESCRIPTION LIST

M37733EHLXXXHP Datasheet

Rev. No.	Revision Description		Rev. date												
1.00	First Edition		970604												
1.01	The following are added: <ul style="list-style-type: none"> <li>• PROM ORDER CONFIRMATION FORM</li> <li>• MARK SPECIFICATION FORM</li> </ul>		980421												
2.00	The following are revised:		980731												
	Page	Previous Version	Revised Version												
	P1 PIN CONFIGURATION (TOP VIEW)	Outline 80P6D-A	Outline 80P6D-A, <u>80P6Q-A</u>												
	P9 Fig. 5														
	P13 Right column Line 2	The M37733EHLXXXHP has 28 powerful addressing modes. Refer to the <u>MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS</u> for the details of each addressing mode.  <b>MACHINE INSTRUCTION LIST</b> The M37733EHLXXXHP has 103 machine instructions. Refer to the <u>MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS</u> for details.	The M37733EHLXXXHP has 28 powerful addressing modes. Refer to the "7700 Family Software Manual" for the details.  <b>MACHINE INSTRUCTION LIST</b> The M37733EHLXXXHP has 103 machine instructions. Refer to the "7700 Family Software Manual" for the details.												
	Line 10	(2) <u>80P6D</u> mark specification form	(2) <u>80P6D</u> , <u>80P6Q</u> mark specification form												
	P17 Memory expansion mode and microprocessor mode	Previous Version <table border="1" style="width:100%; border-collapse: collapse;"> <thead> <tr> <th rowspan="2">Symbol</th> <th rowspan="2">Parameter</th> <th colspan="2">Limits</th> <th rowspan="2">Unit</th> </tr> <tr> <th>Min.</th> <th>Max.</th> </tr> </thead> <tbody> <tr> <td>tsu(D-E)</td> <td>Data input setup time</td> <td style="text-align: center;">80</td> <td></td> <td>ns</td> </tr> </tbody> </table>		Symbol	Parameter	Limits		Unit	Min.	Max.	tsu(D-E)	Data input setup time	80		ns
Symbol	Parameter	Limits				Unit									
		Min.	Max.												
tsu(D-E)	Data input setup time	80		ns											
		Revised Version <table border="1" style="width:100%; border-collapse: collapse;"> <thead> <tr> <th rowspan="2">Symbol</th> <th rowspan="2">Parameter</th> <th colspan="2">Limits</th> <th rowspan="2">Unit</th> </tr> <tr> <th>Min.</th> <th>Max.</th> </tr> </thead> <tbody> <tr> <td>tsu(D-E)</td> <td>Data input setup time</td> <td style="text-align: center;">50</td> <td></td> <td>ns</td> </tr> </tbody> </table>		Symbol	Parameter	Limits		Unit	Min.	Max.	tsu(D-E)	Data input setup time	50		ns
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