8xC251TA, 8xC251TB, 8xC251TP, 8xC251TQ, Hardware Description

Addendum to the 8xC251SA, 8xC251SB, 8xC251SP, 8xC251SQ, User's Manual

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1.0 INTRODUCTION TO THE 8xC251Tx

This Hardware Description describes the 8xC251TA, 8xC251TB, 8xC251TP, 8xC251TQ (referred to collectively as the 8xC251Tx) embedded microcontroller, which is the newest member of the MCS® 251 microcontroller family. The 8xC251Tx is pin and code compatible with the 8xC251Sx but is enhanced with the addition of new features.

This document addresses the differences between the two members of the MCS 251 microcontroller family. For a detailed description of the MCS 251 microcontroller core and standard peripherals shared by both the 8xC251Sx and 8xC251Tx, please refer to the *8xC251SA, 8xC251SB, 8xC251SP, 8xC251SQ Embedded Microcontroller User's Manual* (272795).

1.1 Comparing the 8xC251Tx and 8xC251Sx

The differences between the 8xC251Tx and the 8xC251Sx are briefly described here.

- The maximum operating frequency of the 8xC251Tx is 24 Mhz compared to 16 MHz for the 8xC251Sx.
- The 8xC251Tx has two serial I/O ports while the 8xC251Sx has one. The pins for the second serial I/O port are multiplexed with other functional pins.
- The 8xC251Tx has a new configuration option (Extended Data Float timing) to allow interfacing with slower memories. This feature is supported by a bit in the configuration byte, UCONFIG1. The corresponding bit in the 8xC251Sx has a different function.
- The 8xC251Tx is offered in with factory programmed ROM while the 8xC251Sx is also offered with OTPROM/EPROM.

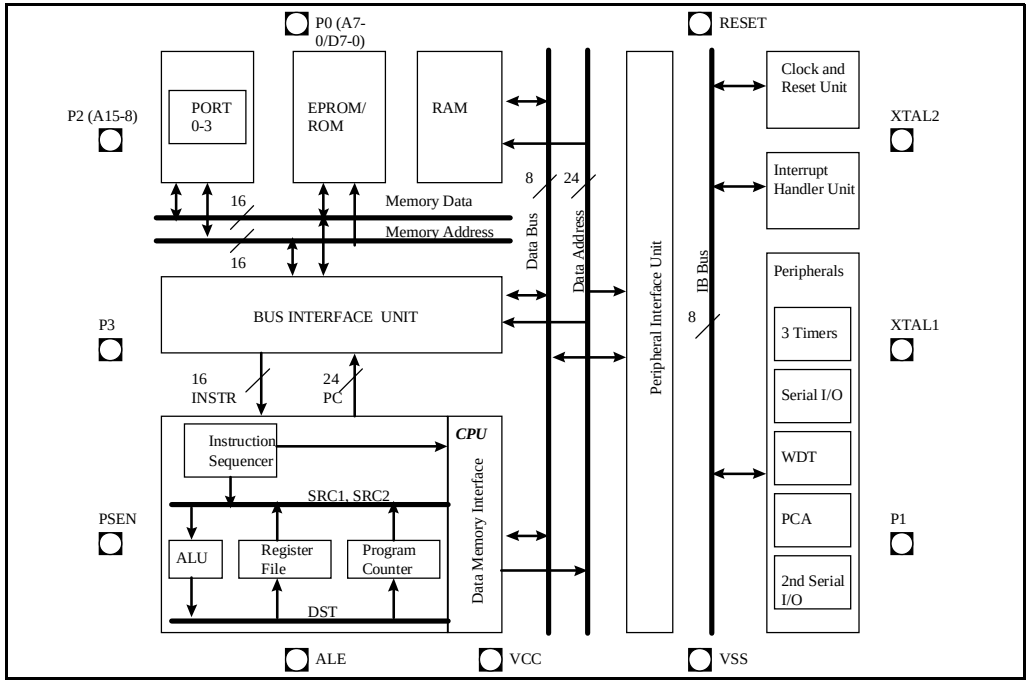

Figure 1. 8xC251Tx Block Diagram

2.0 SIGNAL SUMMARY

Table 1. 8xC251Tx Signal Summary

Address & Data		
Name	**PLCC**	**DIP**
AD0/P0.0	43	39
AD1/P0.1	42	38
AD2/P0.2	41	37
AD3/P0.3	40	36
AD4/P0.4	39	35
AD5/P0.5	38	34
AD6/P0.6	37	33
AD7/P0.7	36	32
A8/P2.0	24	21
A9/P2.1	25	22
A10/P2.2	26	23
A11/P2.3	27	24
A12/P2.4	28	25
A13/P2.5	29	26
A14/P2.6	30	27
A15P2.7	31	28
P3.7/RD#/A16	19	17
P1.7/CEX4/A17/WCLK	9	8

Processor Control		
Name	**PLCC**	**DIP**
P3.2/INT0#	14	12
P3.3/INT1#	15	13
EA#	35	31
RST	10	9
XTAL1	21	18
XTAL2	20	19

Input/Output		
Name	**PLCC**	**DIP**
P1.0/T2	2	1
P1.1/T2EX	3	2
P1.2/EC/RXD1	***4***	***3***
P1.3/CEX0/TXD1	***5***	***4***
P1.4/CEX1	6	5
P1.5/CEX2	7	6
P1.6/CEX3/WAIT#	8	7
P1.7/CEX4/A17/WCLK	9	8
P3.0/RXD	11	10
P3.1/TXD	13	11
P3.4/T0	16	14
P3.51/T1	17	15

Power & Ground		
Name	**PLCC**	**DIP**
V_{CC}	44	40
V_{CC2}	12	
V_{SS}	22	20
V_{SS1}	1	
V_{SS2}	23,24	

Bus Control & Status		
Name	**PLCC**	**DIP**
P3.6/WR#	18	16
P3.7/RD#/A16	19	17
ALE	33	30
PSEN#	32	29

NOTE: Pins in ***this font*** indicate functions associated with the second serial I/O port.

Table 2. 8xC251Tx Signal Descriptions (Sheet 1 of 3)

Signal Name	Type	Description	Alternate Function
A17	O	**Address Line 17.** Output to memory as the 18th external address bit (A17) in extended bus applications, depending on the values of bits RD0 and RD1 in configuration byte UCONFIG0 (see Chapter 4, "Device Configuration," of the *8xC251SA, 8xC251SB, 8xC251SP, 8xC251SQ Embedded Microcontroller User's Manual* (272795). See also RD# and PSEN#.	P1.7/CEX4/ WCLK
A16	O	**Address Line 16.** See RD#.	P3.7/RD#
A15:8*	O	**Address Lines.** Upper address lines for the external bus.	P2.7:0
A7:0	I/O	**Address/Data Lines.** Multiplexed lower address lines and data lines for external bus.	P0/7:0
ALE	O	**Address Latch Enable.** ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A15:8 and A7:0. An external latch can use ALE to demultiplex the address from the address/data bus.	
CEX0 CEX1 CEX2 CEX3 CEX4	I/O	**Programmable Counter Array (PCA) input/output pins.** These are input signals for the PCA capture mode and output signals for the PCA compare mode and PCA PWM mode.	P1.3/TXD1 P1.4 P1.5 P1.6/WAIT# P1.7/A17/ WCLK
EA#	I	**External Access.** Direct program accesses to on-chip or off-chip code memory. For EA# = 0, all program memory accesses are off chip. For EA# = 1, all program memory accesses are on-chip if the address is within the range of the on-chip program memory; otherwise the access is off-chip. The value of EA# is latched at reset. For devices without on-chip program memory, EA# must be strapped to ground.	
ECI	I	**PCA External Clock Input.** External clock input to the 16 bit PCA timer.	P1.2/RXD1
INT1:0#	I	**External Interrupts 0 and 1.** These inputs set IE1:0 in the TCON register. If bits IT1:0 in the TCON register are set, units IE1:0 are set by the falling edge on the INT1#/INT0#. If bits IT1:0 are clear, bits IE1:0 are set by a low level on INTO1:0#.	P3.3:2
P0.7:0	I/O	**Port 0.** This is an 8 bit, open drain, bidirectional I/O port.	AD7:0
P1.0 P1.1 P1.2 P1.3 P1.4 P1.5 P1.6 P1.7	I/O	**Port 1.** This is an 8 bit, bidirectional I/O port with internal pullups.	T2 T2EX ECI/RXD1 CEX0/TXD1 CEX1 CEX2 CEX3/WAIT# CEX4/A17/ WCLK
P2.7:0	I/O	**Port 2.** This is an 8 bit, bidirectional I/O port with internal pullups.	A15:8

* The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for non page mode configuration. If configured in page mode, Port 0 carries the lower address bits (A7:0) and Port 2 carries the upper address bits (A15:8) and the data (D7:0)

Table 2. 8xC251Tx Signal Descriptions (Sheet 2 of 3)

Signal Name	Type	Description	Alternate Function
P3.0 P3.1 P3.2 P3.3 P3.4 P3.5 P3.6 P3.7	I/O	**Port 3.** This is an 8 bit, bidirectional I/O port with internal pullups	RXD TXD INT0# INT1# T0 T1 WR# RD#/A16
PSEN#	O	**Program Store Enable.** Read signal output to external memory. Asserted for the address range specified by the configuration byte UCONFIG0, bits RD1:0.	
RD#	O	**Read.** Read signal output to external memory. Asserted for the address range specified by the configuration byte UCONFIG0, bits RD1:0.	P3.7/A16
RST	I	**Reset.** Reset input to the chip. Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The port pins are driven to their reset conditions when a voltage greater than VIH1 is applied, whether or not the oscillator is running. This signal has a Schmitt trigger input. Connecting the RST pin to V_{CC} through a capacitor provides power-on reset. Asserting RST when the chip is in idle mode or powerdown mode returns the chip to normal operation.	
RXD	I/O	**Receive Serial Data.** RXD send and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2 and 3.	P3.0
RXD1	I/O	**Receive Serial Data 1.** RXD send and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2 and 3 for the second serial I/O port.	P1.2/ECI
T1:0	I	**Timer 1:0 External Clock Inputs.** When Timer 1:0 operates as a counter, a falling edge on the T1:0 pin increments the count.	P3.5:4
T2	I/O	**Timer 2 Clock Input/Output.** For Timer 2 capture mode, this signal is the external clock input. For the clock-out mode, it is the timer 2 clock input.	P1.0
T2EX	I	**Timer 2 External Input.** In Timer 2 capture mode, a falling edge initiates a capture of Timer 2 registers. In auto-reload mode, a falling edge causes the Timer 2 registers to be reloaded. In the up-down counter mode, this signal determines the count direction: • 1=up • 0 = down.	P1.1
TXD	O	**Transmit Serial Data.** TXD outputs the shift clock in serial I/O mode 0 and transmits serial data in serial I/O modes 1, 2 and 3.	P3.1
TXD1	O	**Transmit Serial Data 1.** TXD outputs the shift clock in serial I/O mode 0 and transmits serial data in serial I/O modes 1, 2 and 3 for the second serial I/O port.	P1.3/CEX0
V_{CC}	PWR	**Supply Voltage.** Connect this pin to the +5 supply voltage.	

* The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for non page mode configuration. If configured in page mode, Port 0 carries the lower address bits (A7:0) and Port 2 carries the upper address bits (A15:8) and the data (D7:0)

Table 2. 8xC251Tx Signal Descriptions (Sheet 3 of 3)

Signal Name	Type	Description	Alternate Function
V_{CC2}	PWR	**Secondary Supply Voltage 2.** This supply voltage connection is provided to reduce power supply noise. Connection of this spin to the +5V supply voltage is recommended. However, when using the ZX3 as a pin for pin replacement for the 8XC51FX, V_{CC2} can be unconnected without loss of compatibility (Not available on DIP).	
V_{SS}	GND	**Circuit Ground.** Connect this pin to ground.	
V_{SS1}	GND	**Secondary Ground.** This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the ZX3 as a pin for pin replacement for the 8XC51FX, V_{SS1} can be unconnected without loss of compatibility. (Not available in DIP).	
V_{SS2}	GND	**Secondary Ground 2.** This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the ZX3 as a pin for pin replacement for the 8XC51FX, V_{SS1} can be unconnected without loss of compatibility. (Not available in DIP).	
WAIT#	I	**Real-time Wait State Input.** The real-time WAIT# input is enabled by writing a logical "1" to the WCON.0 (RTWE) bit at S:A7H. During bus cycles, the external memory system can signal 'system ready' to the microprocessor in real time by controlling the WAIT# input signal	P1.6/CEX3
WCLK	O	**Wait Clock Output.** The real-time Wait Clock output is driven by writing a logical "1" to the WCON.1 (RTWCE) bit at S:A7H. When enabled, the WCLK output produces a square wave signal with a period of one-half the oscillator frequency	P1.7/CEX4/ A17
WR#	O	**Write.** Write signal output to external memory. Asserted for the memory address range specified by configuration byte UCONFIG0, bits RD1:0.	P3.6
XTAL1	I	**Input to On-chip, Inverting Oscillator Amplifier.** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. XTAL1 is the clock source for the internal timing	
XTAL2	O	**Output of the On-chip, Inverting Oscillator Amplifier.** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave XTAL2 unconnected.	

* The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for non page mode configuration. If configured in page mode, Port 0 carries the lower address bits (A7:0) and Port 2 carries the upper address bits (A15:8) and the data (D7:0)

Table 3. Special Function Register (SFR) Map

F8		**CH00000000**	**CCAP0Hxxxxxxx**	**CCAP1Hxxxxxxx**	**CCAP2Hxxxxxxx**	**CCAP3Hxxxxxxx**	**CCAP4Hxxxxxxx**	
F0	B 00000000							
E8		CL 00000000	CCAP0L xxxxxxxx	CCAP1L xxxxxxxx	CCAP2L xxxxxxxx	CCAP3L xxxxxxxx	CCAP4L xxxxxxxx	
E0	ACC 00000000							
D8	CCON 00x00000	CMOD 00xxx000	CCAPM0 x0000000	CCAPM1 x0000000	CCAPM2 x0000000	CCAPM3 x0000000	CCAPM4 x0000000	
D0	PSW 00000000	PSW1 00000000						
C8	T2CON 00000000	T2MOD xxxxxx00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000		
C0								
B8	IPL0 x0000000	SADEN 00000000	*SADEN1 00000000*				SPH 00000000	
B0	P3 11111111	*IE1 xxxxxxx0*	*IP1L xxxxxxx0*	*IP1H xxxxxxx0*				IPH0 x0000000
A8	IE0 00000000	SADDR 00000000	*SADDR1 00000000*					
A0	P2 11111111						WDTRST xxxxxxxx	WCON xxxxxxxx
98	SCON 00000000	SBUF xxxxxxxx	*SCON1 00000000*	*SBUF1 xxxxxxxx*				
90	P1 11111111							
88	TCON00000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000		*BGCON 0000xxxx*
80	P0 11111111	SP 00000111	DPL 00000000	DPH 00000000	DPXL 00000001			PCON 00xx0000

NOTE: Registers in ***this font*** are special functions registers that are associated with the second serial I/O port.

3.0 THE SECOND SERIAL I/O PORT

The second serial I/O port is functionally the same as the standard serial I/O port shared by both the 8xC251Tx and the 8xC251Sx. This section provides information about the new special function registers (SFRs) associated with the second serial port. Detailed operation and programming of the serial I/O ports can be obtained from Chapter 10 of the *8xC251SA, 8xC251SB, 8xC251SP, 8xC251SQ Embedded Microcontroller User's Manual* (272795). All the SFRs and control bits for the standard serial I/O port in both the 8xC251Sx and 8xC251Tx have an equivalent in the second serial I/O port. This should be kept in mind when referencing Chapter 10 of the *8xC251SA, 8xC251SB, 8xC251SP, 8xC251SQ Embedded Microcontroller User's Manual* (272795).

3.1 Overview

The second serial I/O port provides synchronous and asynchronous communications modes. It operates as a universal asynchronous receiver and transmitter (UART) in three full-duplex modes (modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates. The second UART provides framing-bit error detection, multiprocessor communications and automatic address recognition. The second serial port also operates in a single synchronous mode (mode 0).

The synchronous mode (mode 0) operates at a single baud rate. Mode 2 operates at two baud rates. Modes 1 and 3 operate over a wide range of frequencies, which are generated by Timer 1 and Timer 2.

The second serial I/O port signals are defined in Table 4 and the special function registers are described in Table 5.

For the three asynchronous modes, the second serial I/O port transmits on the TXD1 pin and receives on the RXD1 pin. For the synchronous mode (mode 0), the second serial I/O port outputs a clock signal on the TXD1 pin and sends and receives messages on the RXD1 pin. The SBUF1 register holds received bytes and bytes to be transmitted. To send, software writes a byte to SBUF1; to receive, software reads SBUF1. The receive shift register allows reception of a second byte before the first byte has been read from SBUF1. However, if software has not read the first byte by the time the second byte is received, the second byte will overwrite the first. The second serial I/O port sets interrupts bits TI1 and RI1 on transmission and reception, respectively. These two share a single interrupt request and interrupt vector.

The serial port control 1 (SCON1) and the secondary serial port control (BGCON) registers configures and controls the second serial I/O port.

Table 4. Second Serial I/O Port Signals

Function Name	Type	Description	Multiplexed With
TXD1	O	**Transmit Serial Data.** TXD1 outputs the shift clock in serial I/O mode 0 and transmits serial data in serial I/O modes 1, 2 and 3 for the second serial I/O port	P1.3/CEX0
RXD1	I/O	**Receive Serial Data 1.** RXD1 send and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2 and 3 for the second serial I/O port	P1.2/ECI

Table 5. Second Serial I/O Port Special Function Registers

Mnemonic	Description	Address
SBUF1	**Serial Buffer 1.** Two separate registers comprise the SBUF1 register. Writing to SBUF1 loads the transmit buffer; reading SBUF1 access the receive buffer	9BH
SCON1	**Serial Port Control 1.** Selects the second serial I/O port operating mode. SCON1 enables and disables the receiver, framing bit error detection, multiprocessor communication, automatic address recognition and the serial port interrupt bits.	9AH
SADDR1	**Serial Address 1.** Defines the individual address for a slave device	AAH
SADEN1	**Serial Address Enable 1.** Specifies the mask byte that is used to define the given address for a slave device	BAH
BGCON	**Secondary Serial Port Control.** Contains controls to the second serial port including the double baud rate bit, read/write access to the SCON1.7 bit as well as bits to control Timer1 or 2 overflow as the baud rate generator for reception and transmission	8FH
IE1	**Interrupt Enable Register 1.** Contains the second serial I/O port interrupt enable bit	B1H
IPL0	**Interrupt Priority Low Control Register 1.** IPL0, together with IPH0, assigns the second serial I/O port interrupt level from 0 (lowest) to 3 (highest)	B2H
IPH0	**Interrupt Priority High Control Register 1.** IPH0, together with IPL0, assigns the second serial I/O port interrupt level from 0 (lowest) to 3 (highest)	B3H

The second serial I/O port interrupt is enabled by setting the ES1 bit in the IE1 register. The priority of the second serial I/O port's interrupt is set to one of four levels by programming the IPL1.0 and IPH1.0 bits in the IPL1 and IPH1 registers, respectively. The second serial I/O port is last in the interrupt polling sequence (see Chapter 6 of the *8xC251SA, 8xC251SB, 8xC251SP, 8xC251SQ Embedded Microcontroller User's Manual* (272795) for details of the interrupt system). The second serial I/O port's Interrupt Service Routine Vector Address is FF:0043H.

When the second serial I/O port is used, the alternate functions of RXD1 and TXD1 can no longer be used. Specifically, the PCA can no longer be clocked by an external clock input since ECI now functions as RXD1. The PCA can, however, be clocked by one of three other methods. They consist of two fixed frequencies (fixed in relation to the Oscillator frequency); $F_{OSC}/12$ and $F_{OSC}/4$ and Timer 0 overflow.

The other consequence of using the second serial I/O port is Module 0 of the PCA can now be used only as a 16 bit Software Timer. The 16-bit Capture, High Speed Output and Pulse Width Modulation modes are no longer available to Module 0 as these modes require the use of CEX0 (which, when the second serial I/O port is in operation, functions as TXD1).

3.2 Special Function Register Definitions

The following describes the special function registers associated with the second serial I/O port and their bit definitions.

3.2.1 SCON1

Address: 9AH
Reset Value: 0000 0000B

Table 6. SCON1 Special Function Register Definitions

Bit Number	Bit Mnemonic	Function
7	FE1SM0	**Framing Error Bit 1:** To Select this function, set the SMOD0 bit in the BGCON register. Set by hardware to indicate an invalid stop bit. Cleared by software, not by valid frames **Second Serial I/O Port Mode Bit 0:** To select this function, clear the SMOD0 bit in the BGCON register. Software writes to bit SM0 and SM1 to select the second serial I/O port operating mode. Refer to SM1 bit for mode selections
6	SM1	**Second Serial I/O Port Mode Bit 1:** Software write to bit SM0 and SM1 (above) to select the serial port operating mode. **SM0 SM1 Mode Description Baud Rate** 0 0 0 Shift Register Fosc/12 0 1 1 8 bit UART variable 1 0 2 9 bit UART Fosc/32* or Fosc/64* 1 1 3 9 bit UART variable * Select by programming the SMOD0 bit in the BGCON register
5	SM2	**Second Serial I/O Port Mode Bit 2:** Software writes to SM2 enable and disable the multiprocessor communication and automatic address recognition features. This allows the second serial I/O port to differentiate between data and command frames and to recognize slave and broadcast addresses
4	REN1	**Receive Enable Bit 1:** To enable reception, set this bit. To enable transmission, clear this bit
3	TB8	**Transmit Bit 8:** In modes 2 and 3, software writes the ninth data bit to be transmitted to TB8. Not used in modes 0 and 1
2	RB8	**Receive Bit 8:** Mode 0: not used Mode 1 (SM2 clear): Set or cleared by hardware to reflect the stop bit received Modes 2 and 3 (SM2 set): Set or cleared by hardware to reflect the ninth data bit received
1	TI1	**Second Serial I/O Port Transmit Interrupt Flag Bit:** Set by transmitter after the last data bit is transmitted. Cleared by software
0	RI1	**Second Serial I/O Port Receive Interrupt Flag Bit:** Set by the receiver after the last data bit of a frame has been received. Cleared by software

3.2.2 SBUF1

Address: 9BH
Reset Value: xxxx xxxxB

To send serial data, software writes a byte to SBUF1 and to receive serial data, software reads from SBUF1.

3.2.3 SADDR1

Address: AAH
Reset Value: 0000 0000B

Slave Individual Address Register1 (SADDR1) contains the device's individual address for multiprocessor communications.

3.2.4 SADEN1

Address: BAH
Reset Value: 0000 0000B

Mask Byte Register 1 (SADEN1) masks bits in the SADDR1 register to form the devices given address for multiprocessor communications.

3.2.5 BGCON

Address: 8FH
Reset Value: 0000 xxxxB

Table 7. BGCON Special Function Register Definitions

Bit Number	Bit Mne-monic	Function
7	SMOD1	**Double Baud Rate Bit:** When set, doubles the baud rate for the second serial I/O port when timer 1 is used and mode 1, 2 or 3 is selected in the SCON1 register.
6	SMOD0	**SCON1.7 Select:** When set, read/write accesses to SCON1.7 are to the FE1 bit. When cleared, read/write accesses to SCON1.7 are to the SM0 bit.
5	RCLK1	**Second Serial I/O Port Receive Clock Bit:** Selects timer 2 overflow pulses (RCLK1 = 1) or timer 1 overflow pulses (RCLK1 = 0) as the baud rate generator for the serial port modes 1 and 3.
4	TCLK1	**Second Serial I/O Port Transmit Clock Bit:** Selects timer 2 overflow pulses (TCLK = 1) or timer 1 overflow pulses (TCLK1 = 0) as the baud rate generator for the serial port modes 1 and 3.
3 - 0	-	Reserved.

3.2.6 IE1

Address: B1H
Reset Value: xxxx xxx0B

Table 8. IE1 Special Function Register Definitions

Bit Number	Bit Mnemonic	Function
7 - 1	-	Reserved
0	ES1	**Second serial I/O port Interrupt Enable:** Setting this bit enables the second serial I/O port interrupt

3.2.7 IPH1

Address: B3H
Reset Value: xxxx xxx0B

Table 9. IPH1 Special Function Register Definitions

Bit Number	Bit Mnemonic	Function
7 - 1	-	Reserved
0	IPH1.0	Second serial I/O port Interrupt Priority High Bit

3.2.8 IPL1

Address: B2H
Reset Value: xxxx xxx0B

Table 10. IPL1 Special Function Register Definitions

Bit Number	Bit Mnemonic	Function
7 - 1	-	Reserved
0	IPL1.0	Second serial I/O port Interrupt Priority Low Bit

Interrupt priority of the second serial I/O port can be programmed to one of four levels depending on the IPH1.0 and IPL1.0 bits.

Table 11. Interrupt Priority of Second Serial I/O Port

IPH1.0	IPL1.0	Priority Level
0	0	0 (Lowest Priority)
0	1	1
1	0	2
1	1	3 (Highest Priority)

4.0 EXTENDED DATA FLOAT TIMING

The Extended Data Float Timing feature seeks to provide a solution to users that may be using slower memory devices. Essentially, this feature extends the TRHDZ1 AC timing specification to accommodate slower memory devices which require a longer period of dead time between a data and address bus cycles. This feature is controlled by a bit in the Configuration byte (UCONFIG1). Bit 3 of UCONFIG1 in the 8xC251Tx is defined as EDF#. In the 8xC251Sx, Bit 3 is defined as WSB. The implications of this change are discussed below. Refer to Chapter 4 of the *8xC251SA, 8xC251SB, 8xC251SP, 8xC251SQ Embedded Microcontroller User's Manual* (272795) for details of the device configuration for the 8xC251Sx. The information in that chapter is valid for the 8xC251Tx with the exception of the change noted in this section.

4.1 Summary of the Extended Data Float Timing Changes

EDF# is used to determine whether the Extended Data Float Timing is enabled. Table 12 shows the definition of UCONFIG1 for the 8xC251Tx. Only bit 3 has been redefined.

Table 12. UCONFIG1 bit definitions for the 8xC251Tx

Bit Number	Bit Mnemonic	Function
7:5	-	**Reserved for Internal or Future Use.** Set these bits when programming UCONFIG1
4	INTR	**Interrupt Mode:** If this bit is set, interrupts push 4 bytes onto the stack (the 3 bytes of the PC and PSW1). If this bit is clear, interrupts push the 2 lower bytes of the PC onto the stack.
3	EDF#	**Extended Data Float Timings:** When cleared, the extended data float timings are enabled. When set, 8xC251Sx compatible AC timings are enabled
2:1	WSB1:0#	**External Wait State B (Region 01:):** WSB1# WSB2# 0 0 Inserts 3 wait states for region 01: 0 1 Inserts 2 wait states for region 01: 1 0 Inserts 1 wait state for region 01: 1 1 Zero wait states for region 01:
0	EMAP	**EPROM Map:** For devices with 16 Kbytes of on-chip code memory, clear this bit to map the upper half of the on-chip code memory to region 00: (data memory). Maps FF:2000H-FF:3FFFH to 00:E000H-00:FFFFH. If this bit is set, mapping does not occur and the addresses in the range 00:E000H-00:FFFFH access external RAM.

Refer to the *8xC251SA, 8xC251SB, 8xC251SP, 8xC251SQ Embedded Microcontroller User's Manual* (272795) for the AC timings specifications.

Table 13 shows the effect of programming EDF# and WSB#[1:0] on the extended data float timing feature as well as the insertion of wait states for region 01:. It should be noted that enabling the extended data float timing allows region 01: to have 1 or 3 wait states inserted (depending on WSB#[1:0]) but not 0 or 2 wait states.

Table 13. Summary of the EDF# and WSB#[1:0] Configuration Options

EDF#	WSB#[1:0]	Wait State	Extended Data Float Timings
1	11	0	No
1	10	1	No
1	01	2	No
1	00	3	No
0	11	1	Yes
0	10	1	Yes
0	01	3	Yes
0	00	3	Yes

The external user configuration cycle (UCONF = 1 and EA# = 0) will be executed with the extended TRHDZ1 timing bus cycle.