

TBB1004

Twin Built in Biasing Circuit MOS FET IC VHF/UHF RF Amplifier

REJ03G0842-1100 Rev.11.00 Aug 22, 2006

Features

- Small SMD package CMPAK-6 built in twin BBFET; To reduce using parts cost & PC board space.
- Suitable for World Standard Tuner RF amplifier.
- Very useful for total tuner cost reduction.
- Withstanding to ESD; Built in ESD absorbing diode. Withstand up to 200V at C=200pF, Rs=0 conditions.
- Provide mini mold packages; CMPAK-6

Outline

RENESAS Package code: PTSP0006JA-A (Package name: CMPAK-6)



- 1. Drain(1)
- 2. Source
- 3. Gate-1(1)
- 4. Gate-1(2)
- 5. Gate-2
- 6. Drain(2)

Notes: 1. Marking is "DM".

2. TBB1004 is individual type number of RENESAS TWIN BBFET.

Absolute Maximum Ratings

 $(Ta = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DS}	6	V
Gate1 to source voltage	V _{G1S}	+6	V
		-0	
Gate2 to source voltage	V_{G2S}	+6	V
		-0	
Drain current	I _D	30	mA
Channel power dissipation	Pch ^{*3}	250	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Note: 3. Value on the glass epoxy board ($49\text{mm} \times 38\text{mm} \times 1\text{mm}$).

Electrical Characteristics

 $(Ta = 25^{\circ}C)$

The below specification are applicable for UHF unit (FET1)

Item	Symbol	Min	Тур	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	_		V	$I_D = 200 \ \mu A, \ V_{G1S} = V_{G2S} = 0$
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	_		V	$I_{G1} = +10 \mu A, V_{G2S} = V_{DS} = 0$
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	_		V	$I_{G2} = +10 \mu A, V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff current	I _{G1SS}		_	+100	nA	$V_{G1S} = +5 \text{ V}, V_{G2S} = V_{DS} = 0$
Gate2 to source cutoff current	I_{G2SS}		_	+100	nA	$V_{G2S} = +5 \text{ V}, V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.5	0.7	1.0	V	$V_{DS} = 5 \text{ V}, V_{G2S} = 4 \text{ V}$
						I _D = 100 μA
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	0.7	1.0	V	$V_{DS} = 5 \text{ V}, V_{G1S} = 5 \text{ V}$
						$I_D = 100 \mu\text{A}$
Drain current	I _{D(op)}	13	17	21	mA	$V_{DS} = 5 \text{ V}, V_{G1} = 5 \text{ V}$
						$V_{G2S} = 4 \text{ V}, R_G = 100 \text{ k}\Omega$
Forward transfer admittance	y _{fs}	21	26	31	mS	$V_{DS} = 5 \text{ V}, V_{G1} = 5 \text{ V}, V_{G2S} = 4 \text{ V}$
						$R_G = 100 \text{ k}\Omega, f = 1 \text{ kHz}$
Input capacitance	Ciss	1.4	1.8	2.2	pF	$V_{DS} = 5 \text{ V}, V_{G1} = 5 \text{ V}$
Output capacitance	Coss	1.0	1.4	1.8	pF	$V_{G2S} = 4 \text{ V}, R_G = 100 \text{ k}\Omega$
Reverse transfer capacitance	Crss	_	0.02	0.04	pF	f = 1 MHz
Power gain	PG	16	21	_	dB	$V_{DS} = V_{G1} = 5 \text{ V}, V_{G2S} = 4 \text{ V}$
Noise figure	NF	_	1.7	2.5	dB	$R_G = 100 \text{ k}\Omega, f = 900 \text{ MHz}$
						Zi = S11*, Zo = S22*(:PG)
						Zi = S11opt (:NF)

Electrical Characteristics (cont.)

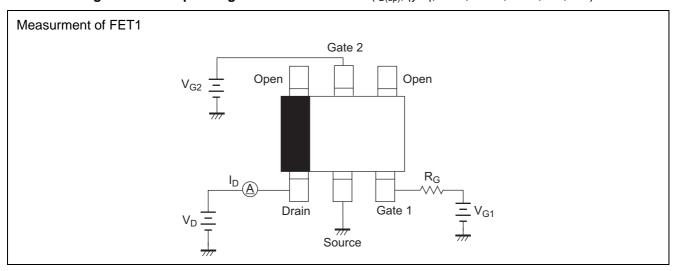
 $(Ta = 25^{\circ}C)$

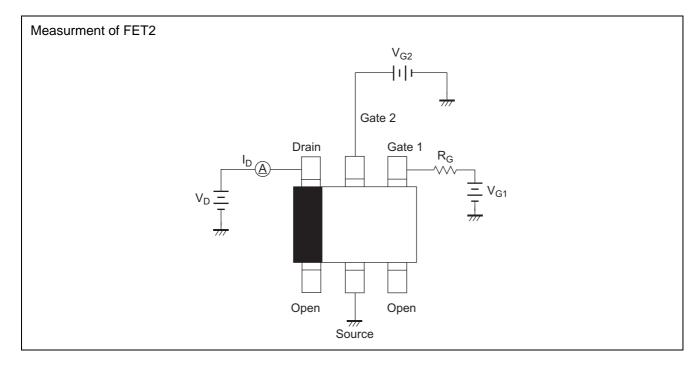
The below specification are applicable for VHF unit (FET2)

Item	Symbol	Min	Тур	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	_	_	V	$I_D = 200 \mu\text{A}, V_{G1S} = V_{G2S} = 0$
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	_	_	V	$I_{G1} = +10 \mu A, V_{G2S} = V_{DS} = 0$
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	_	_	V	$I_{G2} = +10 \mu A, V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff current	I _{G1SS}	1	_	+100	nA	$V_{G1S} = +5 \text{ V}, V_{G2S} = V_{DS} = 0$
Gate2 to source cutoff current	I _{G2SS}	1	_	+100	nA	$V_{G2S} = +5 \text{ V}, V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.5	0.75	1.0	V	$V_{DS} = 5 \text{ V}, V_{G2S} = 4 \text{ V}$
						$I_D = 100 \mu A$
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	0.75	1.0	V	$V_{DS} = 5 \text{ V}, V_{G1S} = 5 \text{ V}$
						$I_D = 100 \mu\text{A}$
Drain current	$I_{D(op)}$	16	20	24	mA	$V_{DS} = 5 \text{ V}, V_{G1} = 5 \text{ V}$
						$V_{G2S} = 4 \text{ V}, R_G = 100 \text{ k}\Omega$
Forward transfer admittance	y _{fs}	27	32	37	mS	$V_{DS} = 5 \text{ V}, V_{G1} = 5 \text{ V}, V_{G2S} = 4 \text{ V}$
						$R_G = 100 \text{ k}\Omega, f = 1 \text{ kHz}$
Input capacitance	Ciss	2.3	2.7	3.1	pF	$V_{DS} = 5 \text{ V}, V_{G1} = 5 \text{ V}$
Output capacitance	Coss	1.4	1.8	2.2	pF	$V_{G2S} = 4 \text{ V}, R_G = 100 \text{ k}\Omega$
Reverse transfer capacitance	Crss		0.03	0.05	pF	f = 1 MHz
Power gain	PG	24	29		dB	$V_{DS} = V_{G1} = 5 \text{ V}, V_{G2S} = 4 \text{ V}$
Noise figure	NF	_	1.2	1.7	dB	$R_G = 100 \text{ k}\Omega, f = 200 \text{ MHz}$

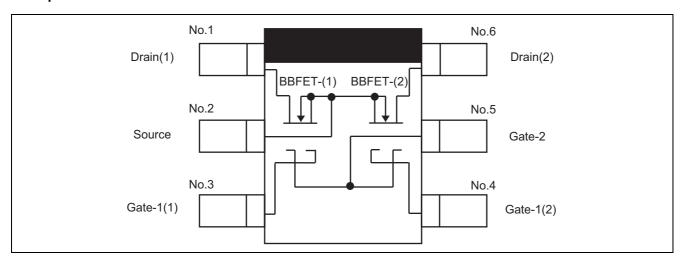
Test Circuits

 $\bullet \ \, \textbf{DC Biasing Circuit for Operating Characteristic Items} \ (I_{D(op)}, \ |yfs|, \ Ciss, \ Coss, \ Crss, \ NF, \ PG) \\$

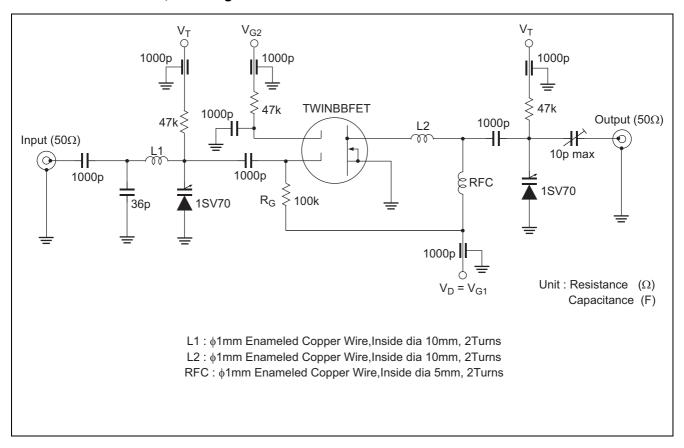


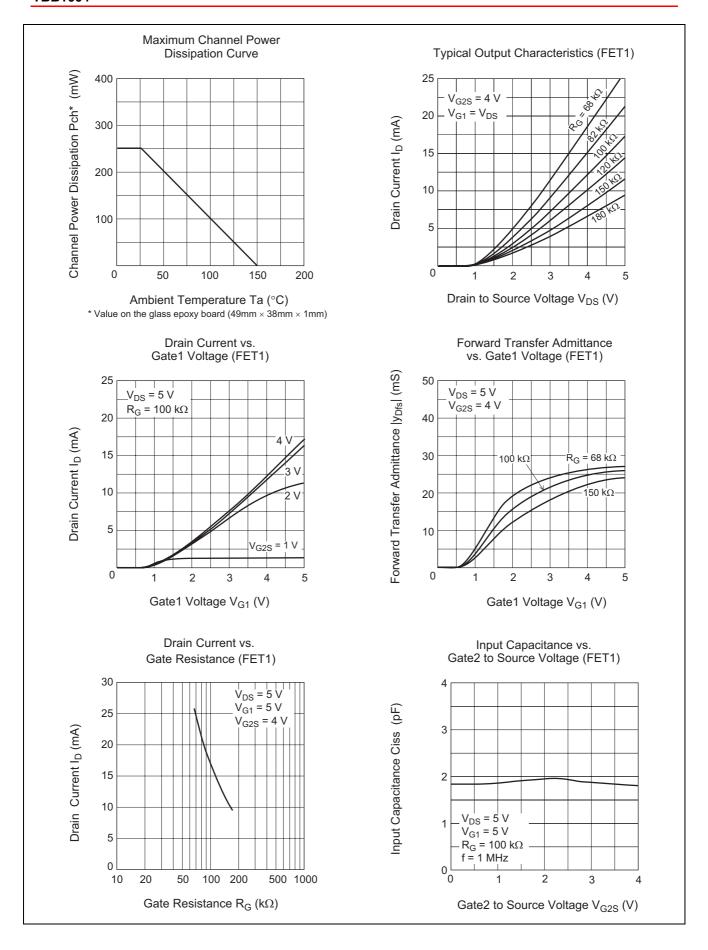


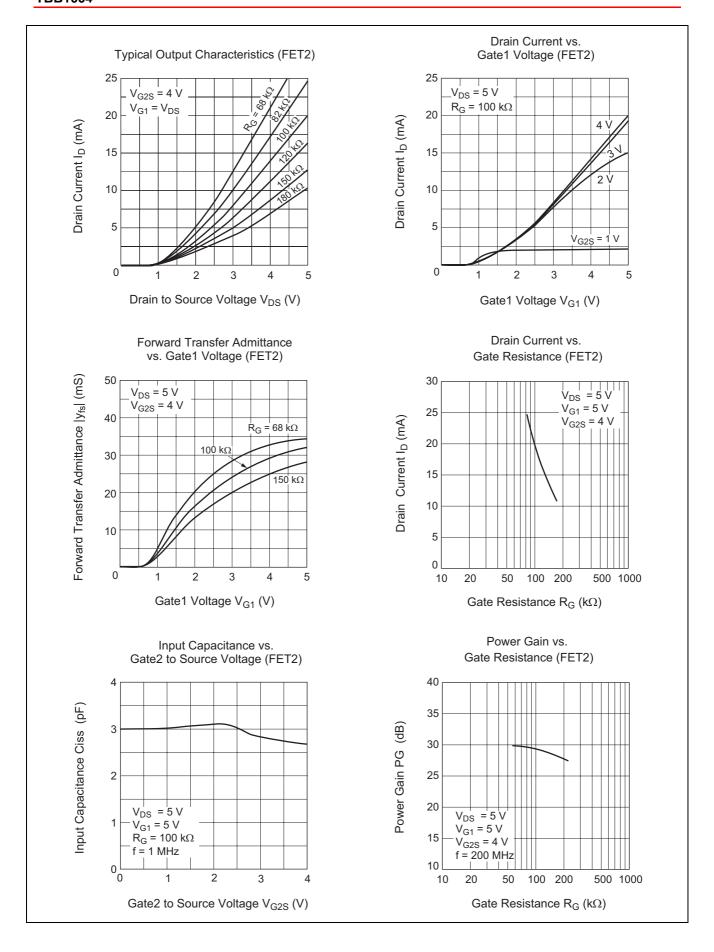
• Equivalent Circuit

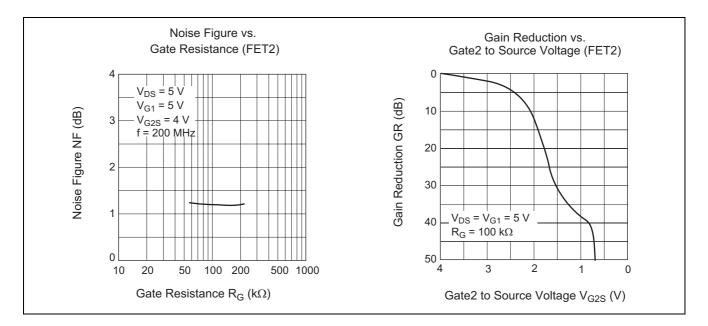


• 200 MHz Power Gain, Noise Figure Test Circuit

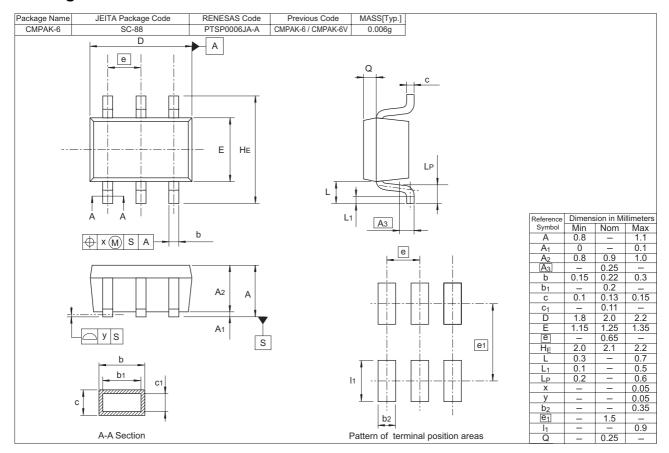








Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
TBB1004DMTL-E	3000	φ 178 mm Reel, 8 mm Emboss Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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