



NICAM 728 - Stereo Encoder

The MC44C404 NICAM Stereo Encoder is the industry's first single-chip CMOS implementation of a Near Instantaneous Companding Audio Multiplex 728 (NICAM) stereo encoder.

- Intended for use in set-top boxes, VCRs, DVD players/recorders, game stations, and other applications that are required to output high-quality stereo sound through a single RF coaxial cable.
- Engineered to process analog audio signals to generate a QPSK modulated signal in compliance with the EN 300 163 standard.
- Designed to output this signal to a Freescale RF modulator, which in turn produces a stereo encoded RF channel for use with any NICAM stereo television receiver.

Features

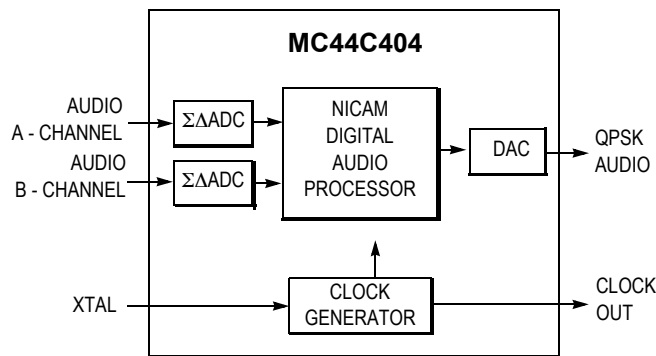
- Supports B, G, H, I, K1, L system standards
- NICAM digital audio processing encodes and transports stereo signals
- Integrated A/D converter input and D/A converter output circuitry
- Extended low frequency response (below 25 Hz)
- Simple passive interface to MC44BS373/4 UHF modulators
- Low power consumption - typically < 50 mW
- RoHS compliant

Benefits

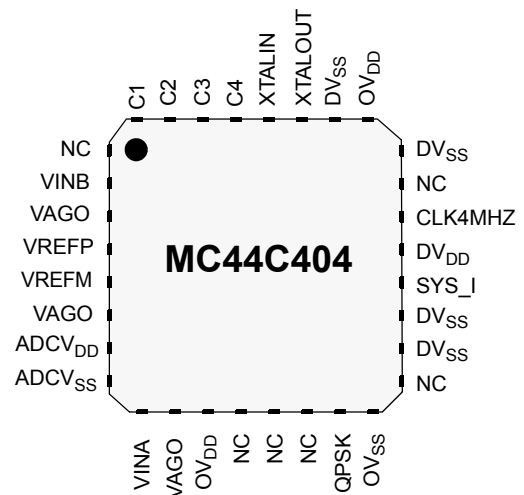
- Preservation of original surround sound fidelity
- Multi standard
- Low system component count, small board size and significantly low overall system cost
- No manual alignment of filters or phase controls

Reference Documentation

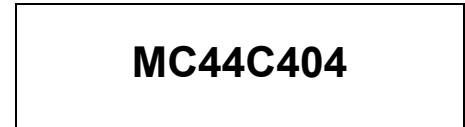
NICAM 728: Transmission of two-channel digital sound with terrestrial television systems B, G, H, I, K1 and L. (EN 300 163 V1.2.1)



Functional Block Diagram



MC44C404 32TQFN Package



ORDERING INFORMATION			
Device	Temp. Range	Package	RoHS
MC44C404EP	0°C to +70°C	32TQFN	Yes
MC44C404EPR2		Tape & Reel	Yes

This document contains information on a preproduction product. Specifications and information herein are subject to change without notice.

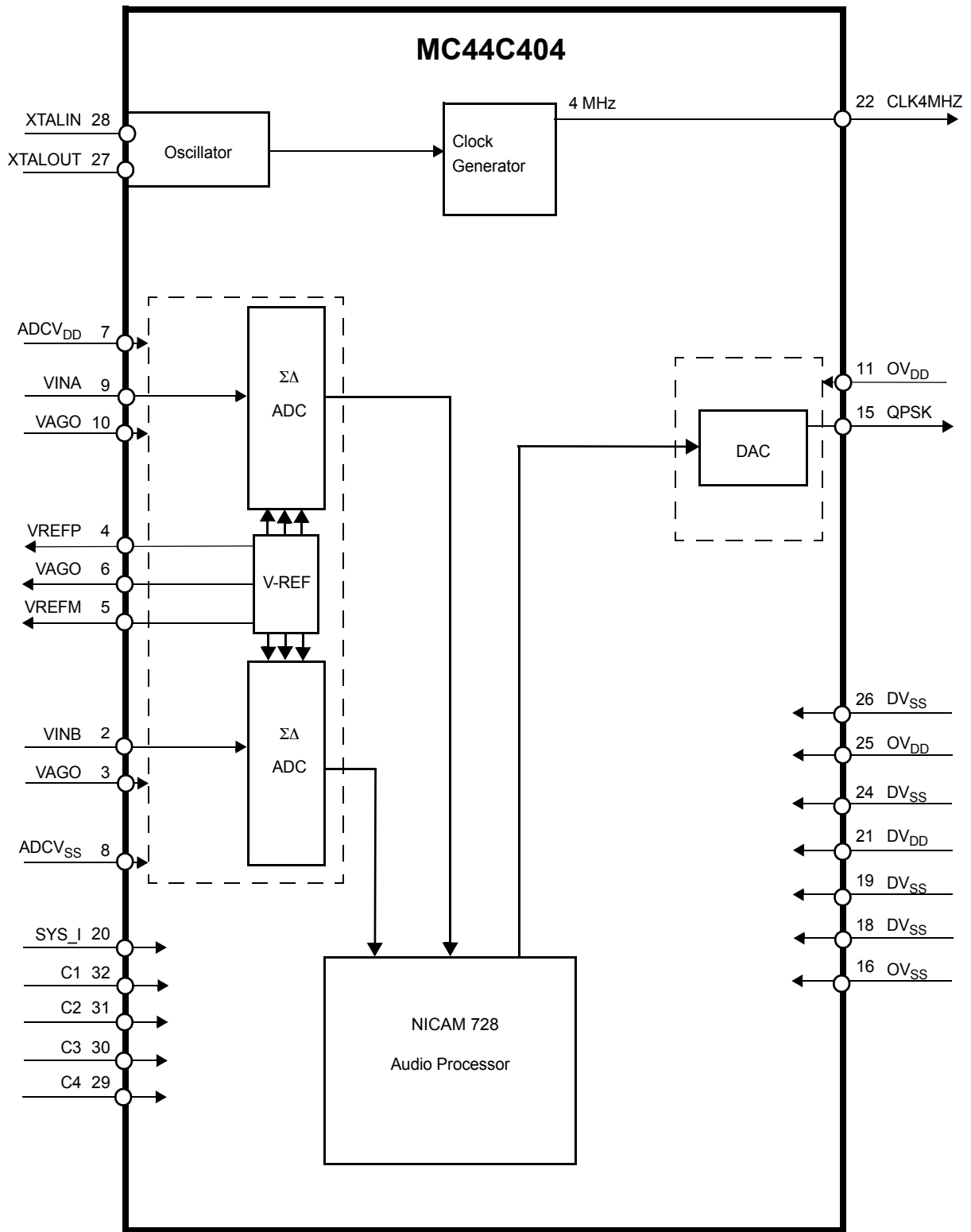


Figure 1. MC44C404 Block Diagram

PIN DESCRIPTION

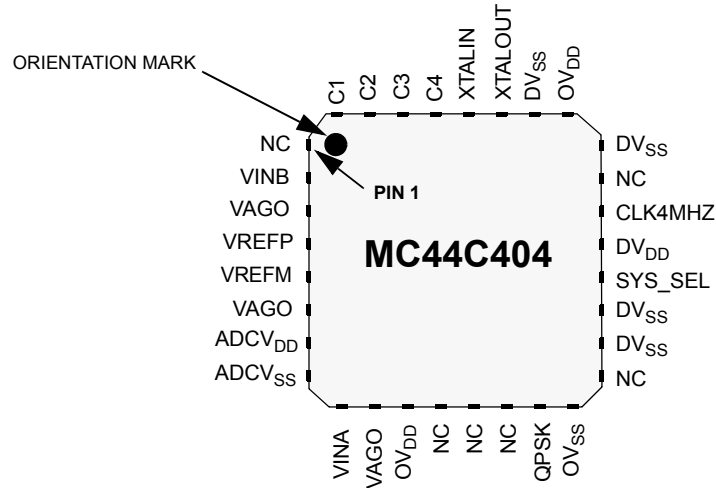


Figure 2. MC44C404 32-Lead TQFN Package

Table 1. Pin Descriptions (Listed by Function)

Signal Name	Pin #	Description
Analog		
VINA	9	A channel input
VREFP	4	ADC voltage ref. bypass plus
VAGO	3, 6, 10	Analog virtual ground
VREFM	5	ADC voltage ref. bypass minus
VINB	2	B channel input
Digital		
C1	32	Control inputs 1, 2 and 3. See Table 2, Application Control Bits for setting these application control bits.
C2	31	
C3	30	
C4	29	Control input 4 is the reserve sound switching flag. C4 = 0: The analog signal is not carrying the same program as the digital signal. C4 = 1: The analog sound signal is carrying the same program as the digital signal.
SYS_I	20	Output system format select. SYS_I = 0: The output format is System B, G, H, K1 or L. SYS_I = 1: The output format is System I.
QPSK	15	QPSK NICAM audio output
NC	1, 12, 13, 14, 17, 23	No connection
Clocks		
XTALIN	28	Crystal oscillator input
XTALOUT	27	Crystal oscillator output
CLK4MHZ	22	4 MHz clock output for Audio/Video modulator IC
Power Supply		
ADCV _{DD}	7	ADC analog supply voltage, 3.3 V
ADCV _{SS}	8	ADC analog ground
DV _{DD}	21	Digital logic supply voltage, 1.8 V
DV _{SS} and OV _{SS}	16, 18, 19, 24, 26	Digital logic/I/O ground
OV _{DD}	11, 25	I/O supply voltage, 3.3 V

Table 2. Application Control Bits

C1	C2	C3	Contents of the 704-Bit Sound/Data Blocks
0	0	0	Stereo signal
0	1	0	Two independent mono sound signals
1	0	0	One mono signal and one 352 Kbits/sec data channel
1	1	0	One 704 Kbits/sec data channel
X	X	1	Reserved

ELECTRICAL SPECIFICATIONS

Table 3. Absolute Maximum Ratings

Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Characteristic	Symbol	Min	Max	Units
Digital Logic Supply Voltage	DV _{DD}	-0.3	+2.0	V
Digital Output Supply Voltage	OV _{DD}	-0.3	+4.0	V
ADC Supply Voltage	ADCV _{DD}	-0.3	+4.0	V
Input Voltage	V _{in}	-0.3	xV _{DD} + 0.3	V
Storage Temperature Range	T _{stg}	-55	+150	°C

Table 4. General Specifications

Characteristic	Symbol	Min	Typ	Max	Units
ESD Protection (Charge Device Model)	CDM	500	—	—	V
ESD Protection (Human Body Model)	HBM	2000	—	—	V
Latch-Up Immunity	LU	200	—	—	mA

Table 5. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Units
Digital Logic Supply Voltage	DV _{DD}	1.62	1.8	1.98	V
Digital Output Supply Voltage	OV _{DD}	2.97	3.3	3.63	V
ADC Supply Voltage	ADCV _{DD}	2.97	3.3	3.63	V
A/B Channel Input Level	V _{INA} , V _{INB}	—	—	1.8	V _{pp}
Ambient Temperature	T _A	0	—	70	°C

Table 6. DC Characteristics

Characteristic ⁽¹⁾	Symbol	Min	Typ	Max	Units
Digital Logic Supply Current	IDV _{DD}	—	7.5	8.5	mA
Digital Output Supply Current	IOV _{DD}	—	2.0	8.0	mA
ADC Supply Current	IADCV _{DD}	—	7.0	9.0	mA
ADC Voltage Ref. Bypass Plus	VREFP	—	2.0	—	V
ADC Voltage Ref. Bypass Minus	VREFM	—	1.0	—	V
ADC Voltage Ref. Ground	VAGO	—	1.5	—	V
CLK4MHZ, Clock Output Low @ I = 0.6 mA	V _{ol}	2.97	—	—	V
CLK4MHZ, Clock Output High @ I = 0.6 mA	V _{oh}	—	—	3.63	V

1. Unless otherwise noted: DV_{DD} = 1.8 ± 0.18 Vdc, OV_{DD} = ADCV_{DD} = 3.3 ± 0.33 Vdc, GND = 0 Vdc, 0 ≤ T_A ≤ 70°C

Table 7. AC Characteristics (Test setup as shown in Figure 3, MC44C404 Typical Application Circuit for B, G and H Systems)

Characteristic ⁽¹⁾	Symbol	Min	Typ	Max	Units
Input Impedance (A/B Input)	R _{in}	—	22	—	KΩ
QPSK Audio Output Level ⁽²⁾		—	0.85	—	V _{pp}
QPSK Output Level		—	—	2.2	V _{pp}
Signal to Noise Ratio ^{(2),(3)}	SNR	72	75	—	dB
Total Harmonic Distortion ^{(2),(3)}	THD	—	0.1	0.3	%
-1 dB Bandwidth	BW	20	—	14500	Hz

1. Unless other wise noted: DV_{DD} = 1.8 ± 0.18 Vdc, OV_{DD} = ADCV_{DD} = 3.3 ± 0.33 Vdc, GND = 0 Vdc, 0 ≤ T_A ≤ 70°C

2. Test conditions, mono, 1 kHz @ 1.5 V_{pp}

3. Measured in 20 Hz to 13.5 kHz bandwidth

SYSTEM APPLICATION NOTES

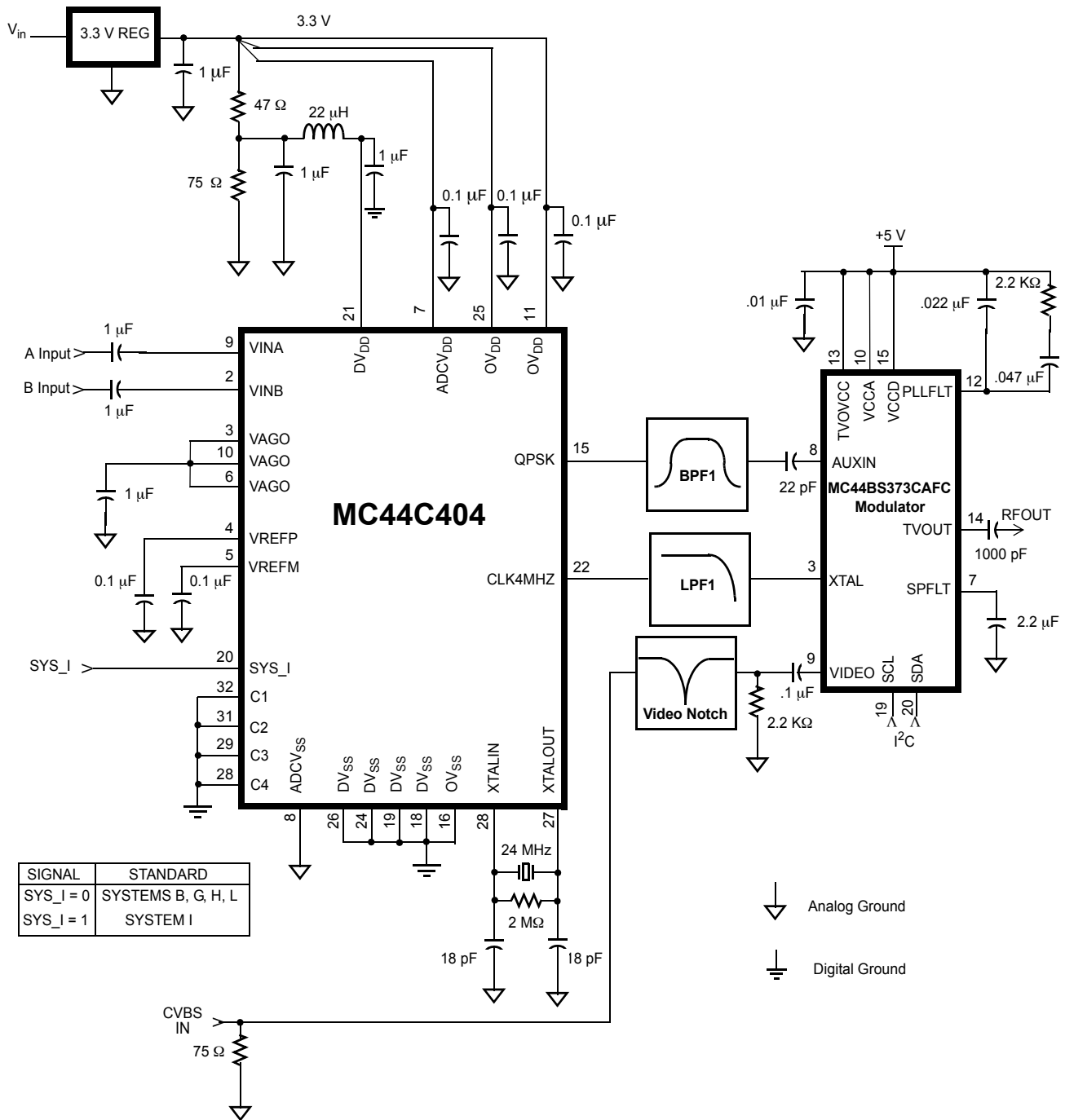
DESIGN CONSIDERATIONS

When developing an application using the MC44C404 NICAM Stereo Encoder, the user can significantly improve performance by following the suggestions below.

1. There must be a notch in the video because video spectra that fall into the audio range will severely impact the audio performance.
2. A band pass filter is required on the QPSK output.

Modulator Interface

3. The 4 MHz clock drive to the MC44BS373 must be filtered and the level set correctly. This can be achieved by using a Low Pass Filter (LPF), as shown in LPF1 in Figure 3, MC44C404 Typical Application Circuit for B, G and H Systems.
4. To set the application control bits see Table 1, Pin Descriptions (Listed by Function) and Table 2, Application Control Bits



SIGNAL	STANDARD
SYS_I = 0	SYSTEMS B, G, H, L
SYS_I = 1	SYSTEM I

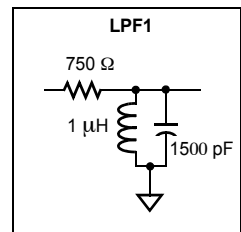
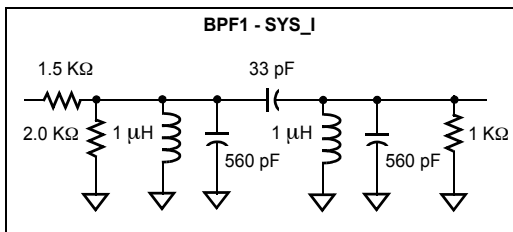
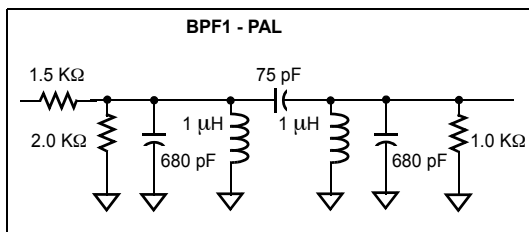
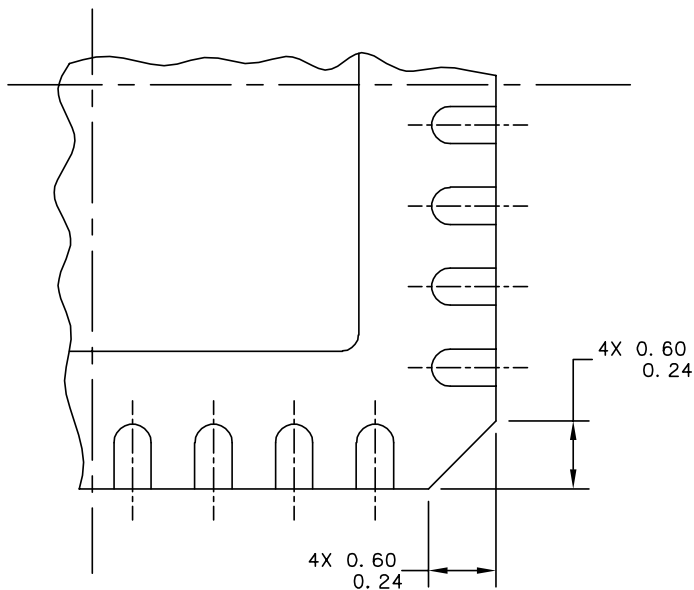
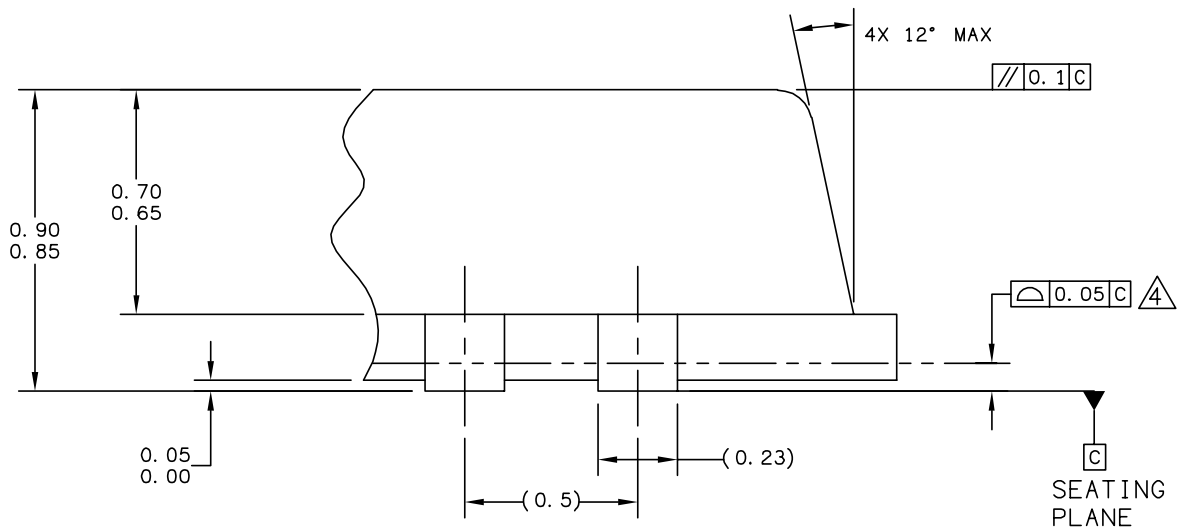


Figure 3. MC44C404 Typical Application Circuit for B, G and H Systems

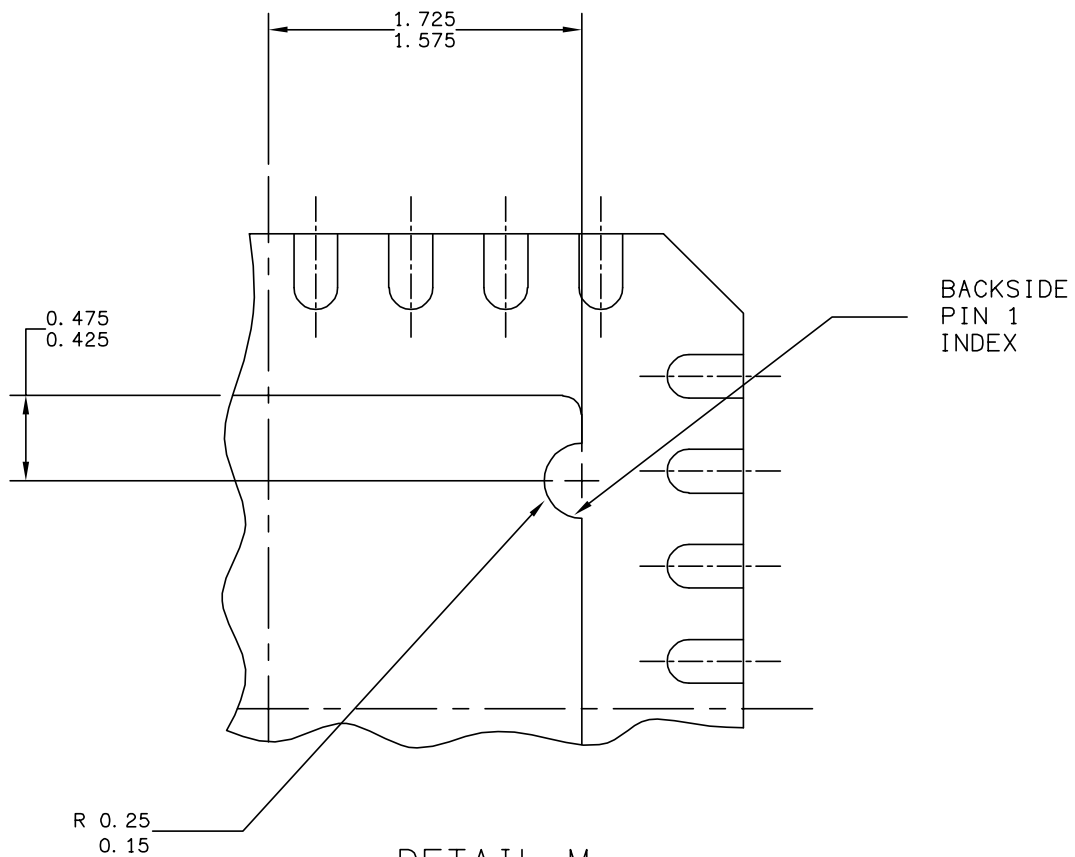


DETAIL N
CORNER CONFIGURATION



DETAIL G
VIEW ROTATED 90° CW

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	CASE NUMBER: 1457-01	07 JUN 2005	
	STANDARD: NON-JEDEC		



DETAIL M
PIN 1 BACKSIDE INDEX

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MC44C404

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFP-N.

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