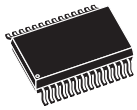
M41ST87Y
M41ST87W

5.0 V and 3.3/3.0 V secure serial RTC and NVRAM supervisor with tamper detection and 128 bytes of clearable NVRAM

Features

- 5.0, 3.3, or 3.0 V operation
- 400 kHz I^2C bus
- NVRAM supervisor to non-volatize external LPSRAM
- 2.5 to 5.5 V oscillator operating voltage
- Automatic switchover and deselect circuitry
- Choice of power-fail deselect voltages
  - M41ST87Y:
    THS = 1: $V_{PFD} \approx 4.63$ V; V_{CC} = 4.75 to 5.5 V
    THS = 0: $V_{PFD} \approx 4.37$ V; V_{CC} = 4.5 to 5.5 V
  - M41ST87W:
    THS = 1: $V_{PFD} \approx 2.9$ V; V_{CC} = 3.0 to 3.6 V
    THS = 0: $V_{PFD} \approx 2.63$ V; V_{CC} = 2.7 to 3.6 V
- Two independent power-fail comparators (1.25 V reference)
- Counters for tenths/hundredths of seconds, seconds, minutes, hours, day, date, month, year, and century
- 128 bytes of clearable, general purpose NVRAM
- Programmable alarm and interrupt function (valid even during battery backup mode)
- Programmable watchdog timer
- Unique electronic serial number (8-byte)
- 32 kHz frequency output available upon power-on
- Microprocessor power-on reset output
- Battery low flag
- Ultra-low battery supply current of 500 nA (typ)

Embedded crystal



28-pin, (300 mil)

SOX28 (MX)

Security features

- Tamper indication circuits with timestamp and RAM clear
- LPSRAM clear function (TP_{CLR})
- Packaging includes a 28-lead, embedded crystal SOIC
- Oscillator stop detection

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1 Description

The M41ST87Y/W serial TIMEKEEPER®/controller SRAM is a low power 1280-bit, static CMOS SRAM organized as 160 bytes by 8 bits. A built-in 32.768 kHz oscillator (internal crystal-controlled) and 8 bytes of the SRAM (see *Table 7*) are used for the clock/calendar function and are configured in binary coded decimal (BCD) format.

An additional 11 bytes of RAM provide calibration, status/control of alarm, watchdog, tamper, and square wave functions. 8 bytes of ROM and finally 128 bytes of user RAM are also provided. Addresses and data are transferred serially via a two line, bidirectional I^2C interface. The built-in address register is incremented automatically after each WRITE or READ data byte. The M41ST87Y/W has a built-in power sense circuit which detects power failures and automatically switches to the battery supply when a power failure occurs. The energy needed to sustain the SRAM and clock operations can be supplied by a small lithium button-cell supply when a power failure occurs.

Functions available to the user include a non-volatile, time-of-day clock/calendar, alarm interrupts, tamper detection, watchdog timer, and programmable square wave output. Other features include a power-on reset as well as two additional debounced inputs ($\overline{\text{RSTIN1}}$ and $\overline{\text{RSTIN2}}$) which can also generate an output reset ($\overline{\text{RST}}$). The eight clock address locations contain the century, year, month, date, day, hour, minute, second and tenths/hundredths of a second in 24 hour BCD format. Corrections for 28, 29 (leap year), 30 and 31 day months are made automatically.

1.1 Security features

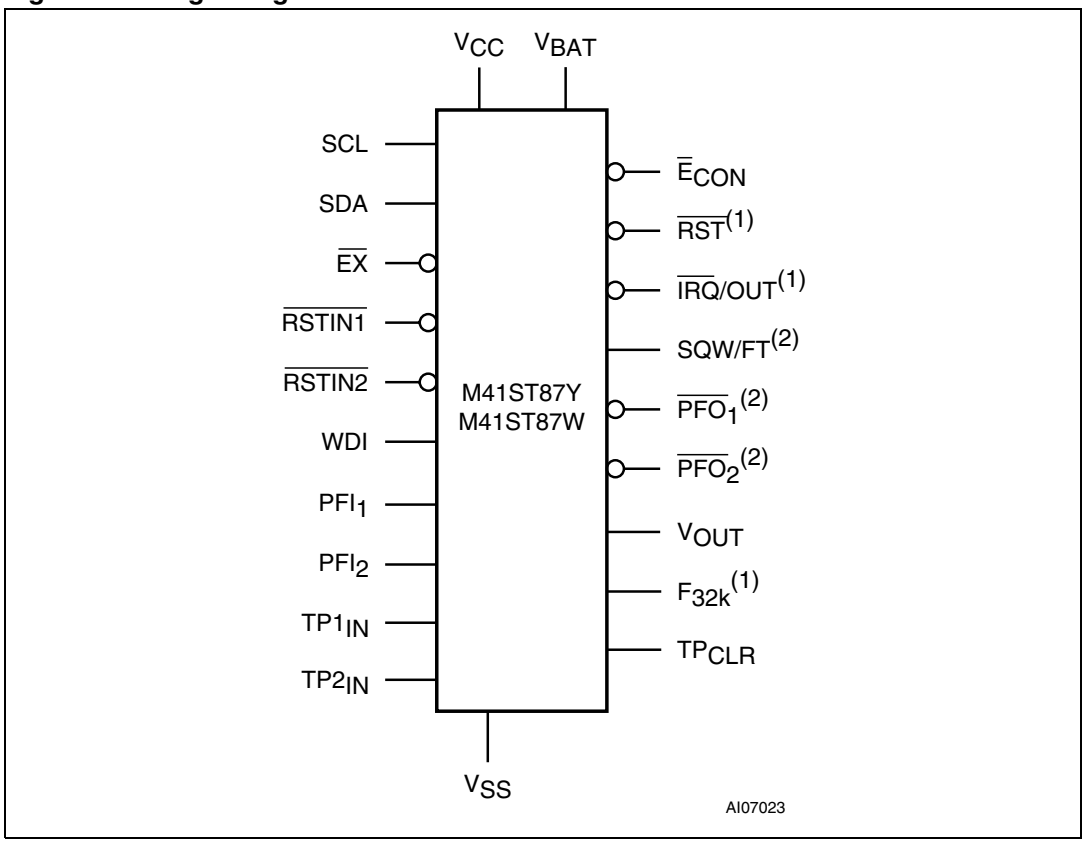
Two fully independent tamper detection Inputs allow monitoring of multiple locations within the system. Programmable bits provide both, “normally open” and “normally closed” switch monitoring. Time stamping of the tamper event is automatically provided. There is also an option allowing data stored in either internal memory (128 bytes), and/or external memory to be cleared, protecting sensitive information in the event tampering occurs. By embedding the 32 kHz crystal in the package, the clock is completely isolated from external tampering. An oscillator fail bit (OF) is also provided to ensure correct operation of the oscillator.

The M41ST87Y/W is supplied in a 28-pin, 300 mil SOIC package (MX) which includes an embedded 32 kHz crystal.

The SOIC package is shipped in plastic anti-static tubes or in tape & reel form.

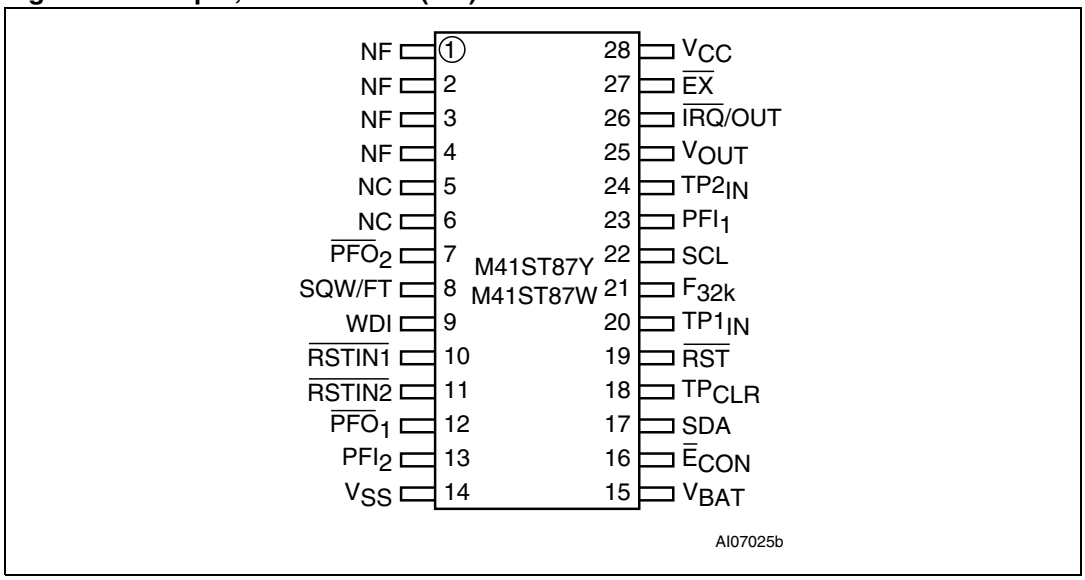
The 300 mil, embedded crystal SOIC requires only a user-supplied battery to provide non-volatile operation.

Figure 1. Logic diagram



1. Open drain output
2. Programmable output (open drain or full-CMOS)

Figure 2. 28-pin, 300 mil SOIC (MX) connections



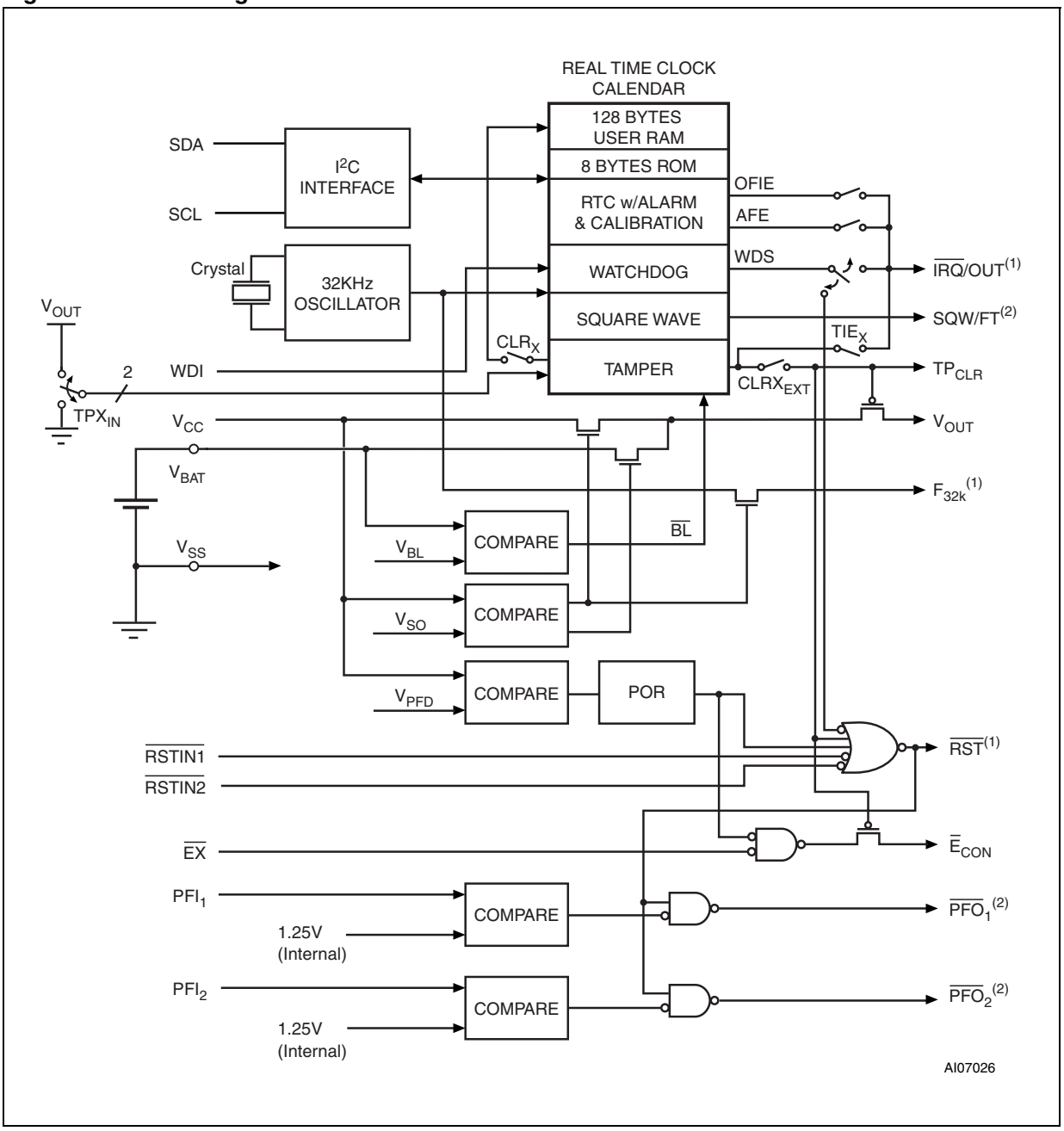
Note: No function (NF) and no connect (NC) pins should be tied to V_{SS}. Pins 1, 2, 3, and 4 are internally shorted together.

Table 1. Signal names

$\overline{E}_{CON}$	Conditioned chip enable output
EX	External chip enable
$\overline{IRQ}$/OUT(1)	Interrupt/out output (open drain)
PFI_1	Power fail input 1
PFI_2	Power fail input 2
$\overline{PFO}_1$(2)	Power fail output 1
$\overline{PFO}_2$(2)	Power fail output 2
$\overline{RST}$(1)	Reset output (open drain)
$\overline{RSTIN1}$	Reset 1 input
$\overline{RSTIN2}$	Reset 2 input
SCL	Serial clock input
SDA	Serial data input/output
SQW/FT(2)	Square wave output/frequency test
WDI	Watchdog input
V_{CC}	Supply voltage
V_{OUT}	Voltage output
V_{SS}	Ground
F_{32k}(1)	32 kHz square wave output (open drain)
$TP1_{IN}$	Tamper pin 1 input
$TP2_{IN}$	Tamper pin 2 input
TP_{CLR}	Tamper pin RAM clear
V_{BAT}	Positive battery pin input
NF(3)	No function
NC(3)	No connect

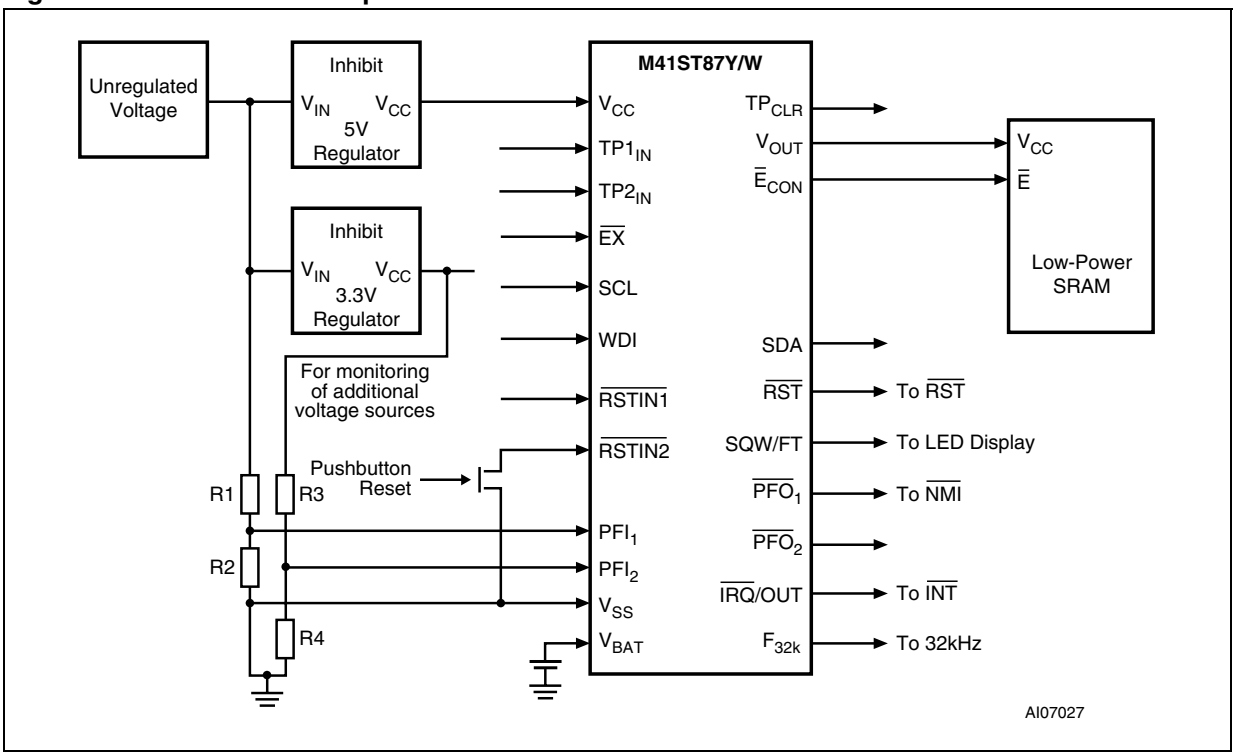
1. Open drain output
2. Programmable output (open drain or full-CMOS)
3. Should be connected to V_{SS}.

Figure 3. Block diagram



1. Open drain output.
2. Programmable output (open drain or full-CMOS); if open drain option is selected and if pulled-up to supply other than V_{CC}, this supply must be equal to, or less than 3.0 V when V_{CC} = 0 V (during battery backup mode).

Figure 4. Hardware hookup



2 Operating modes

The M41ST87Y/W clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 160 bytes contained in the device can then be accessed sequentially in the following order:

00h. Tenths/hundredths of a second register

01h. Seconds register

02h. Minutes register

03h. Century/hours register

04h. Day register

05h. Date register

06h. Month register

07h. Year register

08h. Control register

09h. Watchdog register

0Ah-0Eh. Alarm registers

0Fh. Flag register

10h-12h. Reserved

13h. Square wave

14h. Tamper register 1

15h. Tamper register 2

16h-1Dh. Serial number (8 bytes)

1Eh-1Fh. Reserved (2 bytes)

20h-9Fh. User RAM (128 bytes)

The M41ST87Y/W clock continually monitors V_{CC} for an out-of-tolerance condition. Should V_{CC} fall below V_{PFD}, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from a an out-of-tolerance system. When V_{CC} falls below V_{SO}, the device automatically switches over to the battery and powers down into an ultra low current mode of operation to conserve battery life. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}.

Write protection continues until V_{CC} reaches V_{PFD} (min) plus t_{rec} (min).

For more information on battery storage life refer to application note AN1012.

2.1 2-wire bus characteristics

The bus is intended for communication between different ICs. It consists of two lines: a bidirectional data signal (SDA) and a clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line, while the clock line is high, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

2.1.1 Bus not busy

Both data and clock lines remain high.

2.1.2 Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

2.1.3 Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

2.1.4 Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

2.1.5 Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this

case the transmitter must leave the data line high to enable the master to generate the STOP condition.

Figure 5. Serial bus data transfer sequence

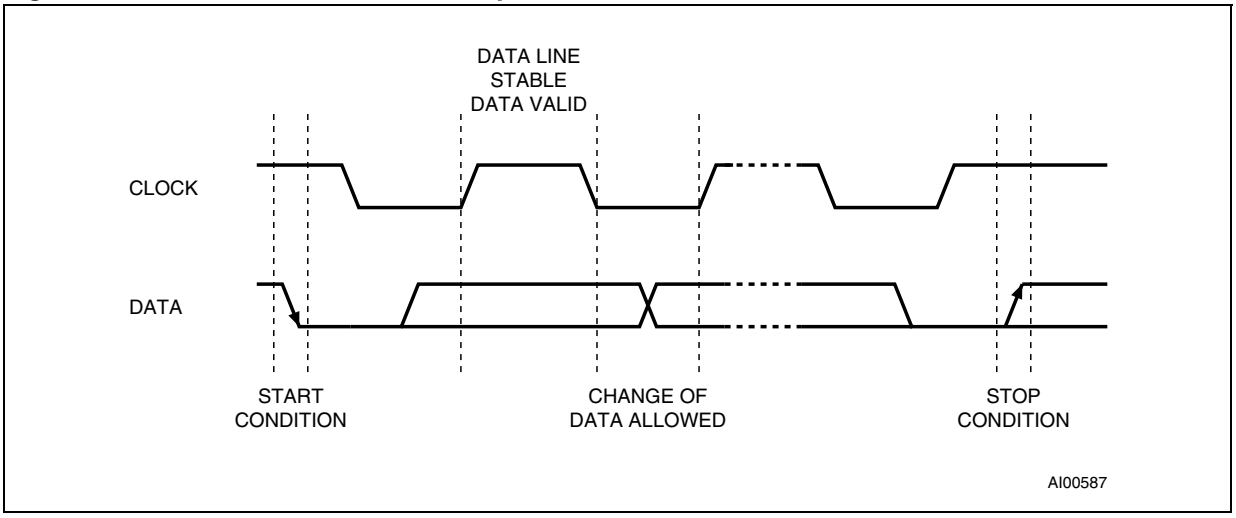


Figure 6. Acknowledgement sequence

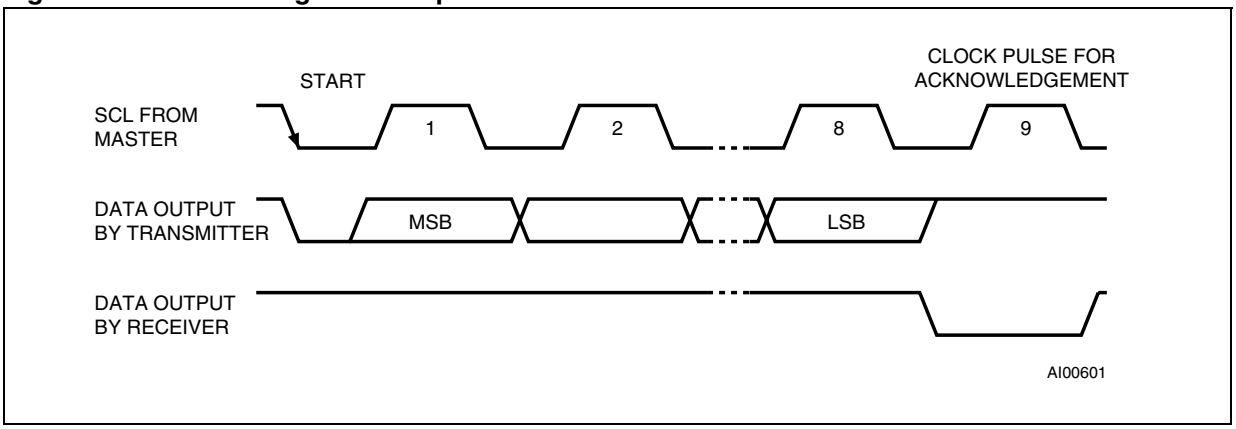


Figure 7. Bus timing requirements sequence

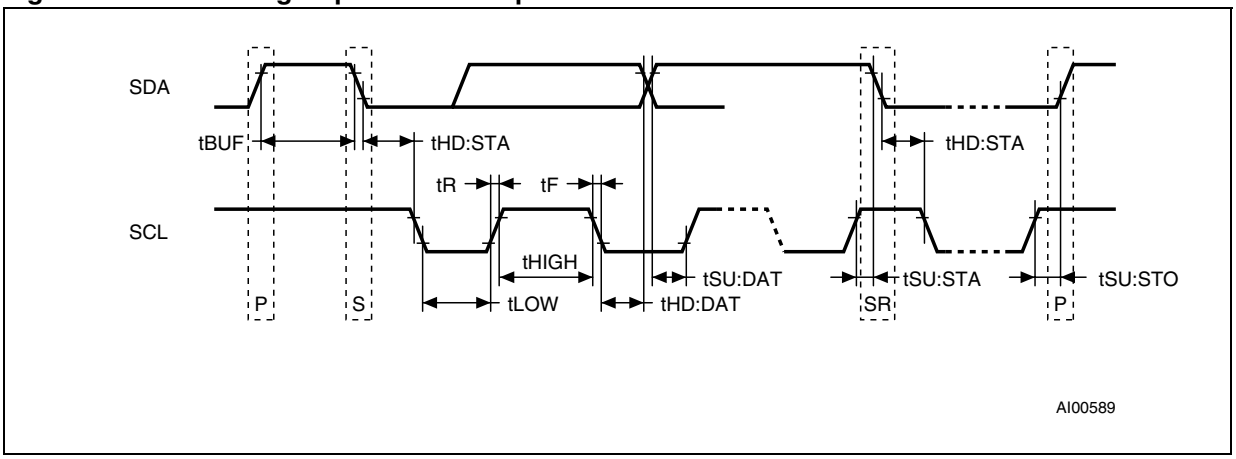


Table 2. AC characteristics

Symbol	Parameter[1]		Min	Max	Unit
f_{SCL}	SCL clock frequency		0	400	kHz
t_{BUF}	Time the bus must be free before a new transmission can start		1.3		µs
t_{EXPD}	$\overline{EX}$ to $\overline{E}_{CON}$ propagation delay	M41ST87Y		10	ns
		M41ST87W		15	ns
t_F	SDA and SCL fall time			300	ns
$t_{HD:DAT}$[2]	Data hold time		0		µs
$t_{HD:STA}$	START condition hold time (after this period the first clock pulse is generated)		600		ns
t_{HIGH}	Clock high period		600		ns
t_{LOW}	Clock low period		1.3		µs
t_R	SDA and SCL rise time			300	ns
$t_{SU:DAT}$	Data setup time		100		ns
$t_{SU:STA}$	START condition setup time (only relevant for a repeated start condition)		600		ns
$t_{SU:STO}$	STOP condition setup time		600		ns

1. Valid for ambient operating temperature: T_A = –40 to 85°C; V_{CC} = 4.5 to 5.5 V or 2.7 to 3.6 V (except where noted).
2. Transmitter must internally provide a hold time to bridge the undefined region (300 ns max) of the falling edge of SCL.

2.2 READ mode

In this mode the master reads the M41ST87Y/W slave after setting the slave address (see *Figure 8 on page 15*). Following the WRITE mode control bit (R/$\overline{W}$=0) and the acknowledge bit, the word address 'An' is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ mode control bit (R/$\overline{W}$=1). At this point the master transmitter becomes the master receiver.

The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge clock. The M41ST87Y/W slave transmitter will now place the data byte at address An+1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to An+2.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter (see *Figure 9 on page 15*).

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume either due to a Stop Condition or when the pointer increments to a non-clock or RAM address.

Note: This is true both in READ mode and WRITE mode.

An alternate READ mode may also be implemented whereby the master reads the M41ST87Y/W slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see *Figure 10 on page 15*).

Figure 8. Slave address location

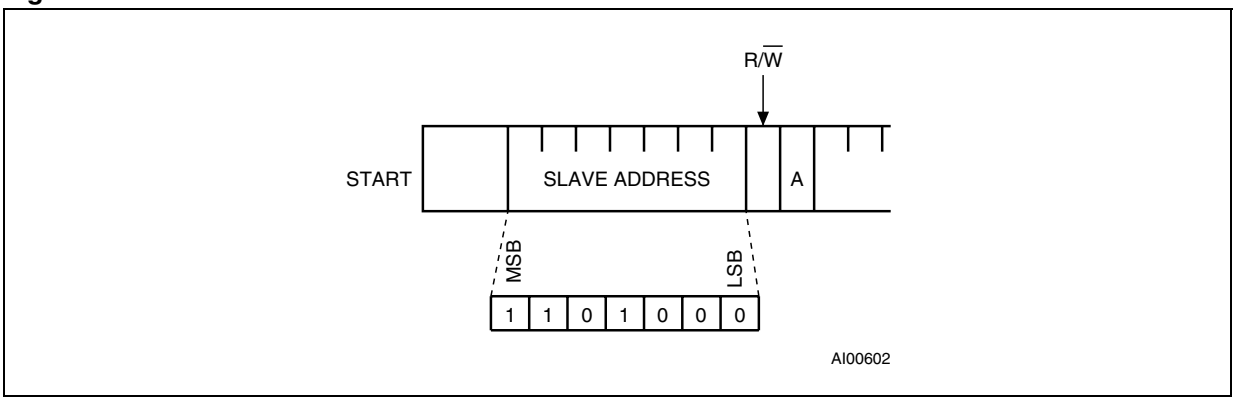


Figure 9. READ mode sequence

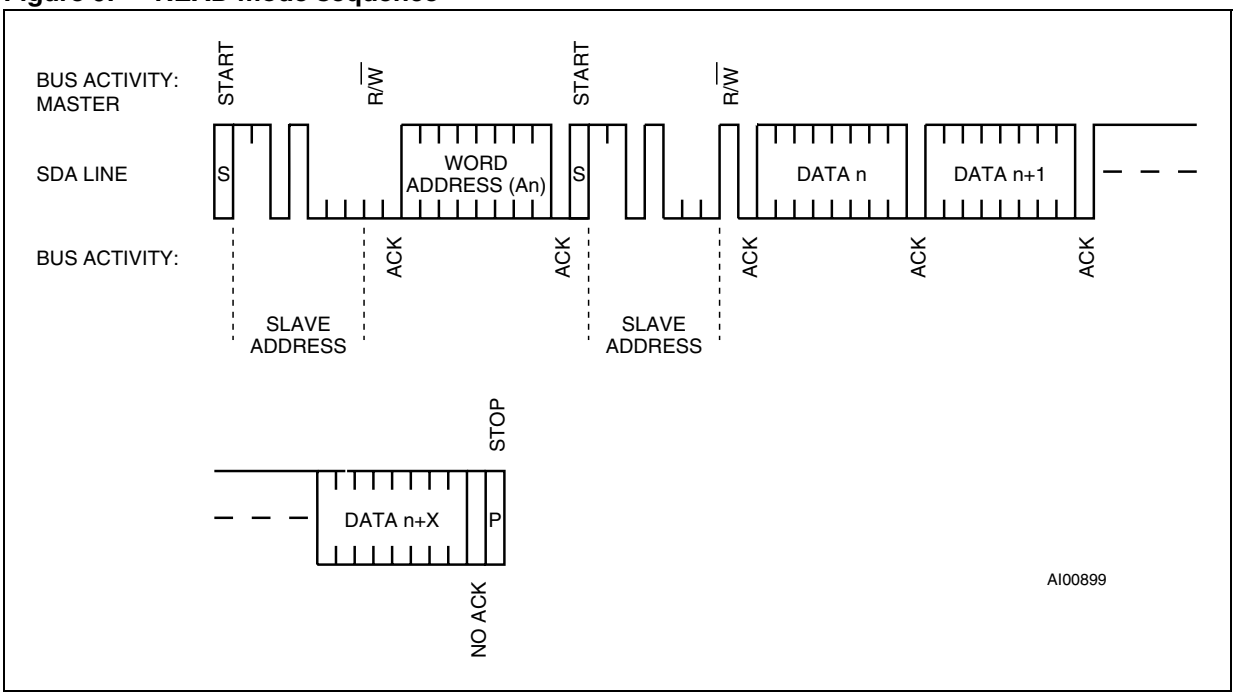
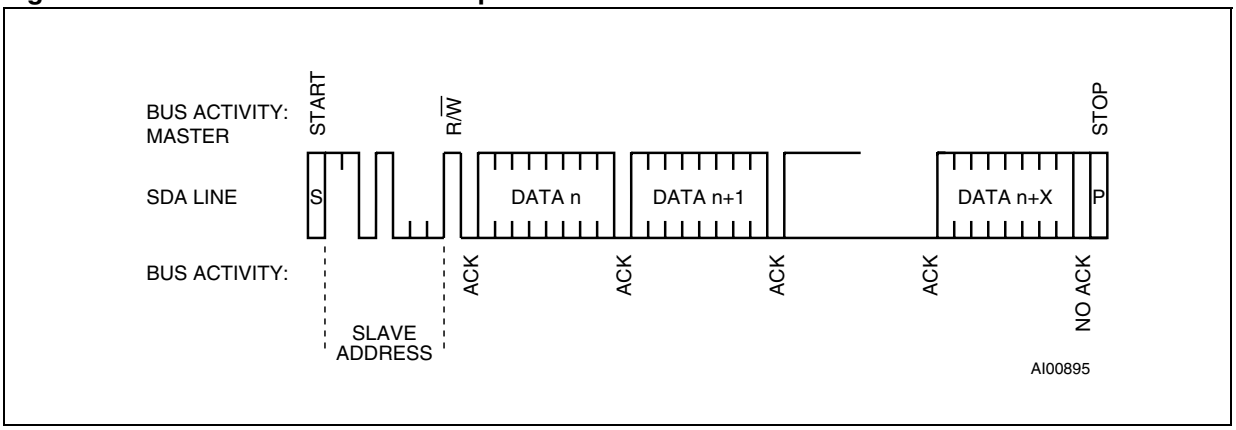


Figure 10. Alternate READ mode sequence



2.3 WRITE mode

In this mode the master transmitter transmits to the M41ST87Y/W slave receiver. Bus protocol is shown in *Figure 11*. Following the START condition and slave address, a logic '0' (R/$\overline{W}$=0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The M41ST87Y/W slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address (see *Figure 8 on page 15*) and again after it has received the word address and each data byte.

Figure 11. WRITE mode sequence

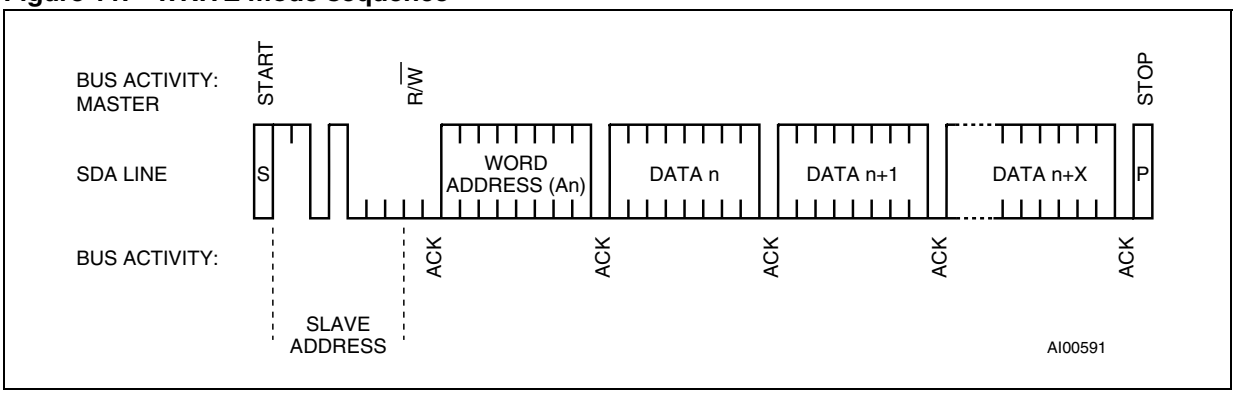
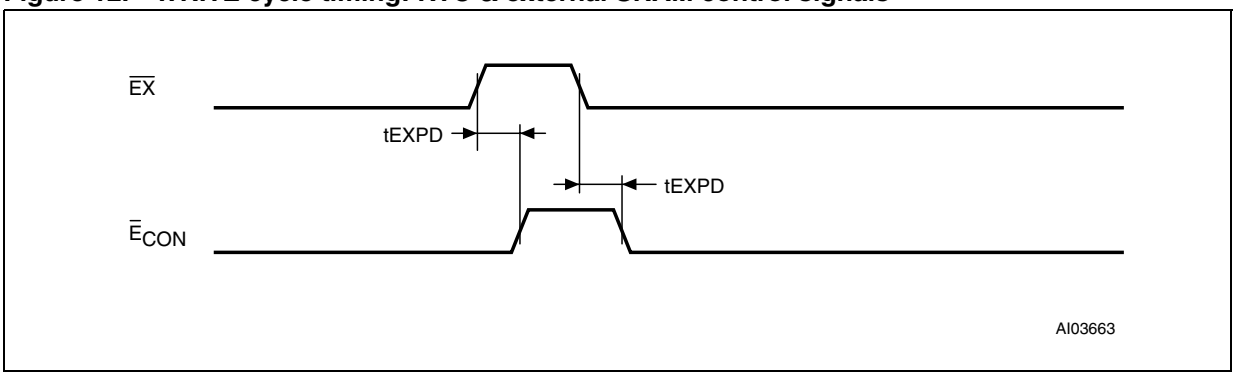


Figure 12. WRITE cycle timing: RTC & external SRAM control signals



2.4 Data retention mode

With valid V_{CC} applied, the M41ST87Y/W can be accessed as described above with READ or WRITE Cycles. Should the supply voltage decay, the M41ST87Y/W will automatically deselect, write protecting itself (and any external SRAM) when V_{CC} falls between V_{PFD} (max) and V_{PFD} (min) (see *Figure 27 on page 43*, *Table 18 on page 44*). This is accomplished by internally inhibiting access to the clock registers. At this time, the Reset pin ($\overline{RST}$) is driven active and will remain active until V_{CC} returns to nominal levels. External RAM access is inhibited in a similar manner by forcing $\overline{E}_{CON}$ to a high level. This level is within 0.2 volts of the V_{BAT}. $\overline{E}_{CON}$ will remain at this level as long as V_{CC} remains at an out-of-tolerance condition. When V_{CC} falls below the battery backup switchover voltage (V_{SO}),

power input is switched from the V_{CC} pin to the battery, and the clock registers and external SRAM are maintained from the attached battery supply.

All outputs become high impedance. The V_{OUT} pin is capable of supplying 100µA (for M41ST87W) or 150µA (for M41ST87Y) of current to the attached memory with less than 0.3 volts drop under this condition. On power up, when V_{CC} returns to a nominal value, write protection continues for t_{rec} by inhibiting $\overline{E}_{CON}$. The $\overline{RST}$ signal also remains active during this time (see *Figure 27 on page 43*).

Note: Most low power SRAMs on the market today can be used with the M41ST87Y/W RTC SUPERVISOR. There are, however some criteria which should be used in making the final choice of an SRAM to use. The SRAM must be designed in a way where the chip enable input disables all other inputs to the SRAM. This allows inputs to the M41ST87Y/W and SRAMs to be "Don't Care" once V_{CC} falls below V_{PFD}(min). The SRAM should also guarantee data retention down to V_{CC} = 2.0 volts. The chip enable access time must be sufficient to meet the system needs with the chip enable output propagation delays included. If the SRAM includes a second chip enable pin (E2), this pin should be tied to V_{OUT}.

If data retention lifetime is a critical parameter for the system, it is important to review the data retention current specifications for the particular SRAMs being evaluated. Most SRAMs specify a data retention current at 3.0 volts. Manufacturers generally specify a typical condition for room temperature along with a worst case condition (generally at elevated temperatures). The system level requirements will determine the choice of which value to use. The data retention current value of the SRAMs can then be added to the I_{BAT} value of the M41ST87Y/W to determine the total current requirements for data retention. The available battery capacity for the battery of your choice can then be divided by this current to determine the amount of data retention available.

For a further more detailed review of lifetime calculations, please see Application Note AN1012.

2.5 Tamper detection circuit

The M41ST87Y/W provides two independent input pins, the tamper pin 1 input ($TP1_{IN}$) and tamper pin 2 input ($TP2_{IN}$), which can be used to monitor two separate signals which can result in the associated setting of the tamper bits (TB1 and/or TB2, in flag register 0Fh) if the tamper enable bits (TEB1 and/or TEB2) are enabled, for the respective tamper 1 or tamper 2. The $TP1_{IN}$ pin or $TP2_{IN}$ pin may be set to indicate a tamper event has occurred by either 1) closing a switch to ground or V_{OUT} (normally open), or by 2) opening a switch that was previously closed to ground or V_{OUT} (normally closed), depending on the state of the TCM_X bits and the TPM_X bits in the tamper register (14h and/or 15h).

2.6 Tamper register bits (tamper 1 and tamper 2)

2.6.1 Tamper enable bits (TEB1 and TEB2)

When set to a logic '1,' this bit will enable the tamper detection circuit. This bit must be set to '0' in order to clear the associated tamper bits (TB_X, in 0Fh).

Note: TEB_X should be reset whenever the tamper detect condition is modified.

2.6.2 Tamper bits (TB1 and TB2)

If the TEB_X bit is set, and a tamper condition occurs, the TB_X bit will be set to '1.' This bit is "Read-only" and is reset only by setting the TEB_X bit to '0.' These bits are located in the flags register 0Fh.

2.6.3 Tamper interrupt enable bits (TIE1 and TIE2)

If this bit is set to a logic '1,' the $\overline{IRQ}$/OUT pin will be activated when a tamper event occurs. This function is also valid in battery backup if the ABE bit (alarm in battery backup) is also set to '1' (see *Figure 14 on page 20*).

Note: In order to avoid an inadvertent activation of the $\overline{IRQ}$/OUT pin due to a prior tamper event, the flag register (0Fh) should be read prior to resetting the TEB_X bit.

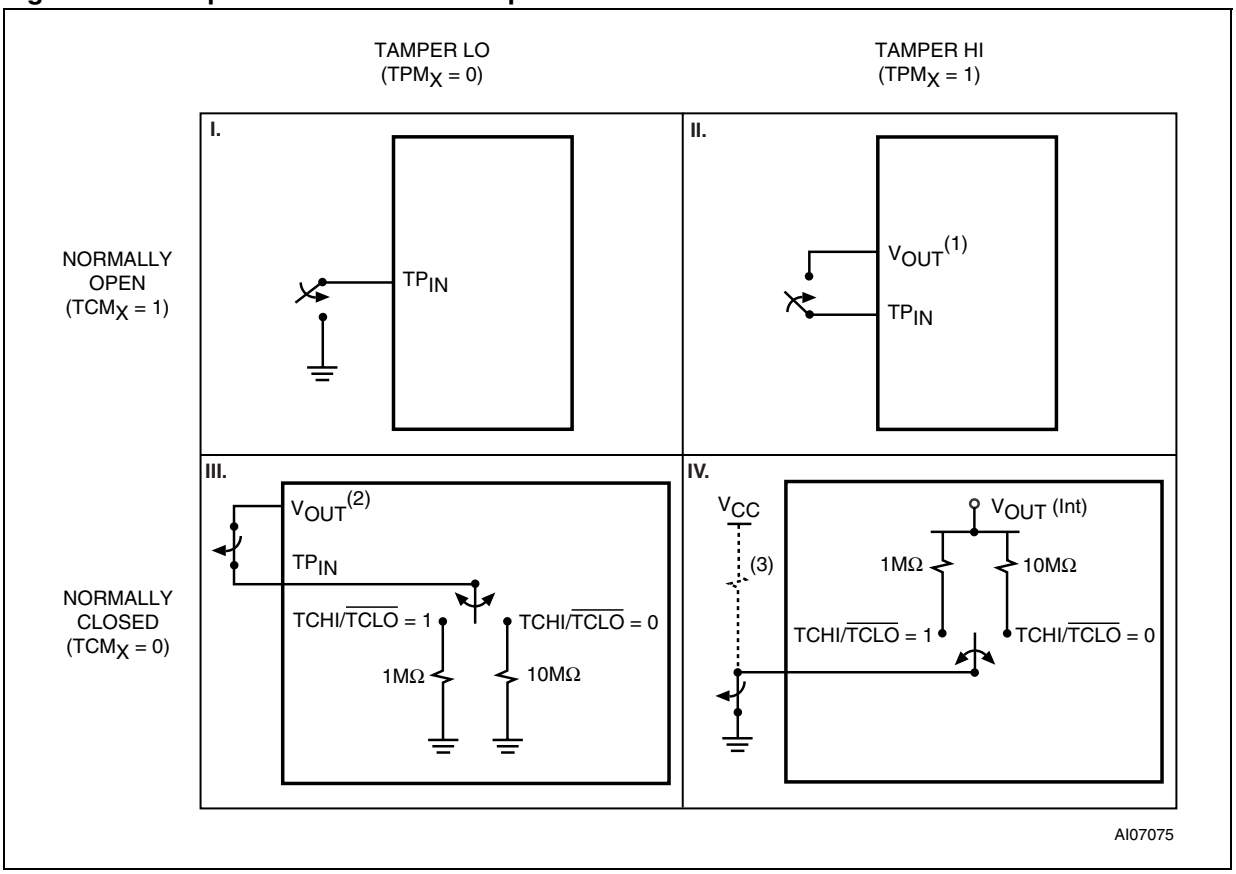
2.6.4 Tamper connect mode bit (TCM1 and TCM2)

This bit indicates whether the position of the external switch selected by the user is in the normally open (TCM_X = '1') or normally closed (TCM_X = '0') position (see *Figure 13 on page 19* and *Figure 15 on page 20*).

2.6.5 Tamper polarity mode bits (TPM1 and TPM2)

The state of this bit indicates whether the tamper pin input will be taken high (to V_{OUT} if TPM_X = '1') or low (to V_{SS} if TPM_X = '0') during a tamper event (see *Figure 13 on page 19* and *Figure 15 on page 20*).

Figure 13. Tamper detect connection options



Note: These options are connected to those in Table 3.

1. If the $CLRX_{EXT}$ bit is set, a second tamper to V_{OUT} (TPM2 = '1') during t_{CLR} will not be detected.
2. If the $CLRX_{EXT}$ bit is set, a second tamper to V_{OUT} (TPM2 = '1') will trigger automatically.
3. Optional external resistor to V_{CC} allows the user to bypass sampling when power is “on.”

Table 3. Tamper detection truth table

Option	Mode	TCM_X	TPM_X
I	Normally open/tamper to GND(1)	1	0
II	Normally open/tamper to V_{OUT}(1)	1	1
III	Normally closed/tamper to GND	0	0
IV	Normally closed/tamper to V_{OUT}	0	1

1. No battery current drawn during battery backup.

Figure 14. Tamper detect output options

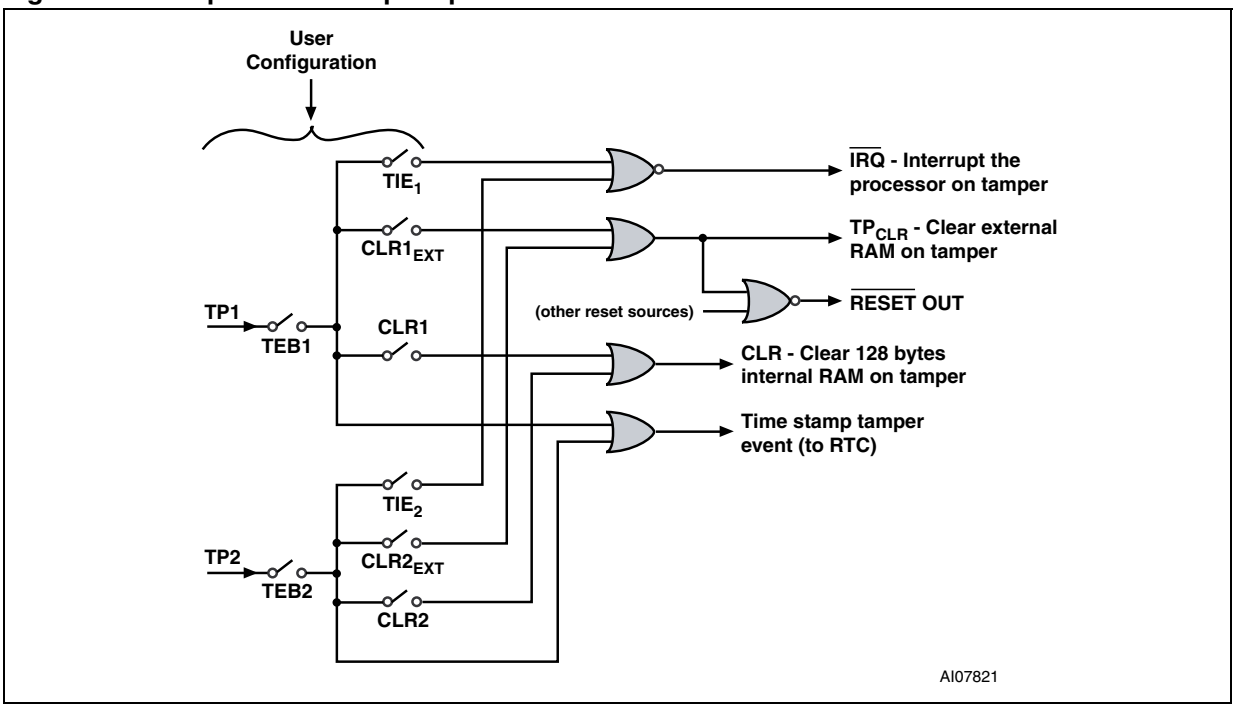
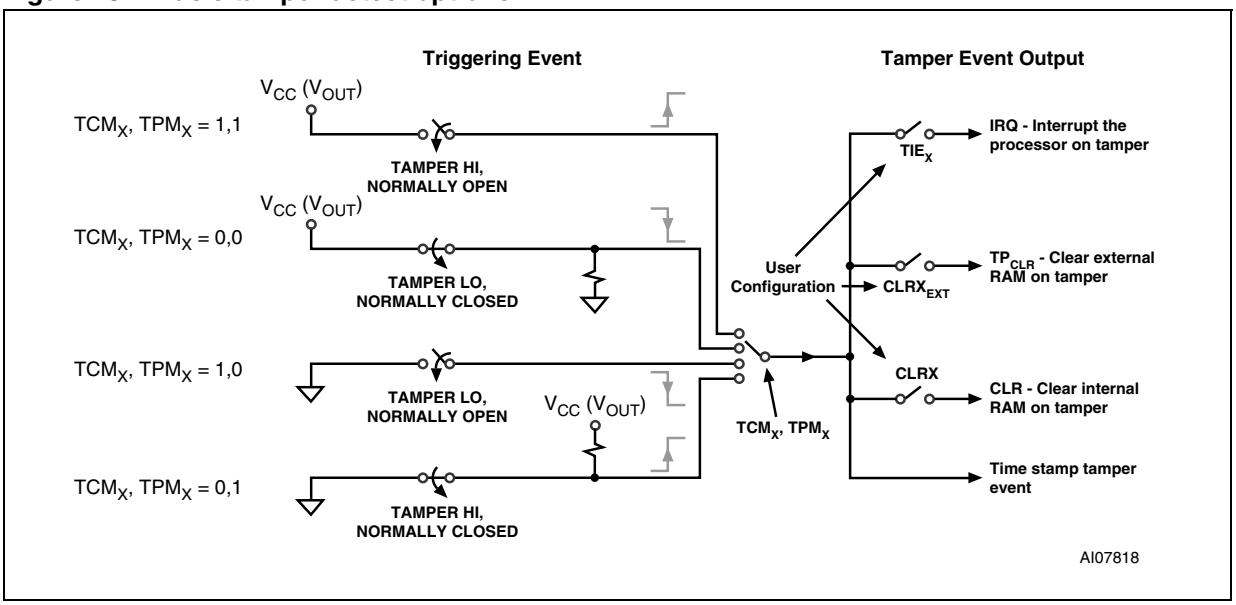


Figure 15. Basic tamper detect options



2.6.6 Tamper detect sampling (TDS1 and TDS2)

This bit selects between a 1Hz sampling rate or constant monitoring of the tamper input pin(s) to detect a tamper event when the normally closed switch mode is selected. This allows the user to reduce the current drain when the TEB_X bit is enabled while the device is in battery backup (see *Table 4 on page 22* and *Figure 16 on page 22*). Sampling is disabled if the TCM_X bit is set to logic '1' (Normally Open). In this case the state of the TDS_X bit is a "Don't care."

Note: The crystal oscillator must be "on" for sampling to be enabled.

2.6.7 Tamper current high/tamper current low (TCHI/$\overline{\text{TCLO}}$1 and TCHI/$\overline{\text{TCLO}}$2)

This bit selects the strength of the internal pull-up or pull-down used during the sampling of the normally closed condition. The state of the TCHI/$\overline{\text{TCLO}}_X$ bit is a "Don't care" for normally open (TCM_X = '1') mode (see *Figure 17 on page 23*).

2.6.8 RAM clear (CLR1 and CLR2)

When either of these bits and the TEB_X bit are set to a logic '1,' the internal 128 bytes of user RAM (see *Figure 14 on page 20*) will be cleared to all zeros in the event of a tamper condition. The 128 bytes of user RAM will be deselected (invalid data will be read) until the corresponding TEB_X bit is reset to '0.'

2.6.9 RAM clear external ($CLR1_{EXT}$ and $CLR2_{EXT}$)

When either of these bits are set to a logic '1' and the TEB_X bit is also set to logic '1,' the external SRAM will be cleared and the $\overline{\text{RST}}$ output enabled (see *Figure 14 on page 20* and *Figure 19 on page 24*).

Note: The reset output resulting from a tamper event will be the same as a reset resulting from a power-down condition, a watchdog time-out, or a manual reset ($\overline{\text{RSTIN1}}$ or $\overline{\text{RSTIN2}}$).

This is accomplished by forcing TP_{CLR} high, which if used to control the inhibit pin of the DC regulator (see *Figure 19 on page 24*) will also switch off V_{OUT}, depriving the external SRAM of power to the V_{CC} pin. V_{OUT} will automatically be disconnected from the battery if the tamper occurs during battery back-up (see *Figure 18 on page 23*). By inhibiting the DC regulator, the user will also prevent other inputs from sourcing current to the external SRAM, allowing it to retain data.

The user may optionally connect an inverting charge pump to the V_{CC} pin of the external SRAM (see *Figure 19 on page 24*). Depending on the process technology used for the manufacturing of the external SRAM, clearing the memory may require varying durations of negative potential on the V_{CC} pin. This device configuration will allow the user to program the time needed for their particular application. Control Bits CLRPW0 and CLRPW1 determine the duration TP_{CLR} will be enabled (see *Figure 18 on page 23* and *Table 5 on page 24*).

Note: When using the inverting charge pump, the user must also provide isolation in the form of two additional small-signal power MOSFETs. These will isolate the V_{OUT} pin from both the negative voltage generated by the charge pump during a tamper condition, and from being pulled to ground by the output of the charge pump when it is in shut-down mode ($\overline{\text{SHDN}}$ = logic low). The gates of both MOSFETs should be connected to TP_{CLR} as shown in Figure 19 on page 24. One n-channel enhancement MOSFET should be placed between

the output of the inverting charge pump and the V_{OUT} of the M41ST87. The other MOSFET should be an enhancement mode p-channel, and placed between V_{OUT} of the M41ST87 and V_{CC} of the external SRAM. When TP_{CLR} goes high after a tamper condition occurs, the n-channel MOSFET will turn on and the p-channel will turn off. During normal operating conditions, TP_{CLR} will be low and the p-channel will be on, while the n-channel will be off.

Table 4. Tamper detection current (normally closed - TCM_X = '0')

TDS_X	$TCHI/\overline{TCLO}_X$	Tamper circuit mode	Current at 3.0 V (typ)(1)(2)	Unit
0	0	Continuous monitoring / 10 MΩ pull-up/-down	0.3	µA
0	1	Continuous monitoring / 1 MΩ pull-up/-down	3.0	µA
1	0	Sampling (1Hz) / 10 MΩ pull-up/-down	0.3	nA
1	1	Sampling (1Hz) / 1 MΩ pull-up/-down	3.0	nA

1. When calculating battery lifetime, this current should be added to I_{BAT} current listed in *Table 17 on page 42*.
2. Per tamper detect input

Figure 16. Tamper detect sampling options

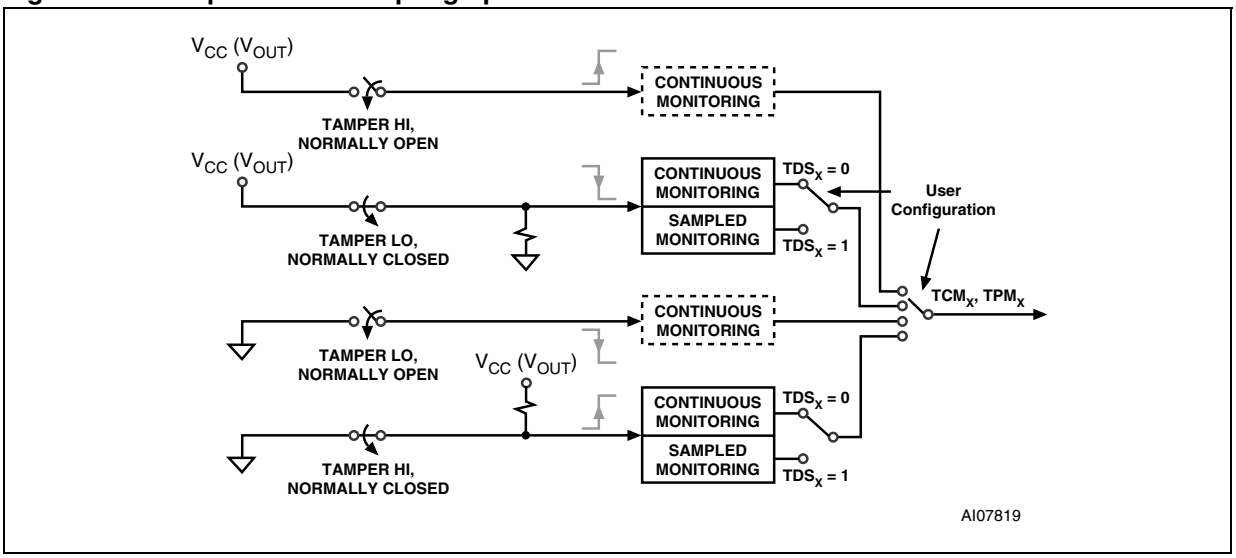


Figure 17. Tamper current options

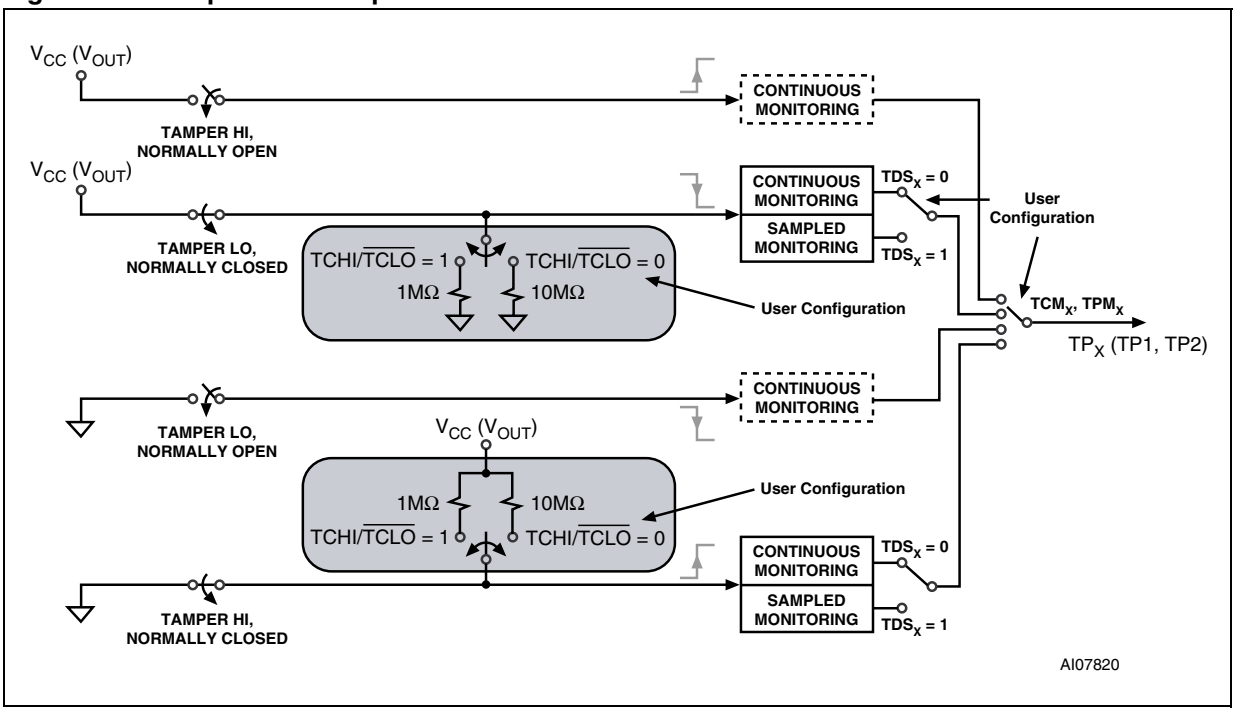
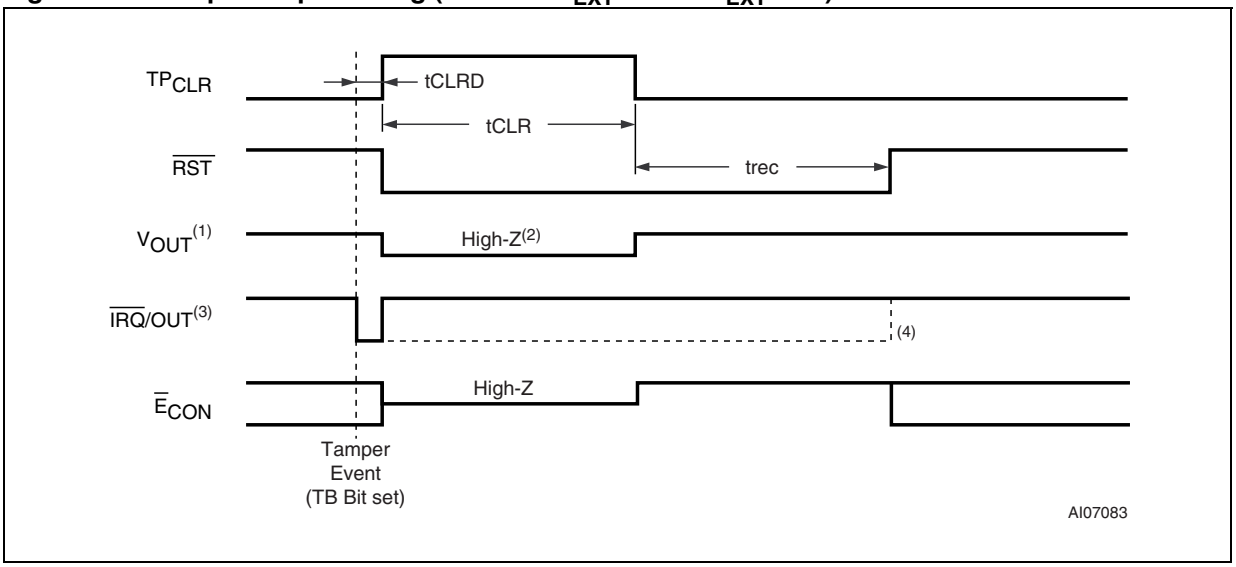


Figure 18. Tamper output timing (with $CLR1_{EXT}$ or $CLR2_{EXT}$ = '1')



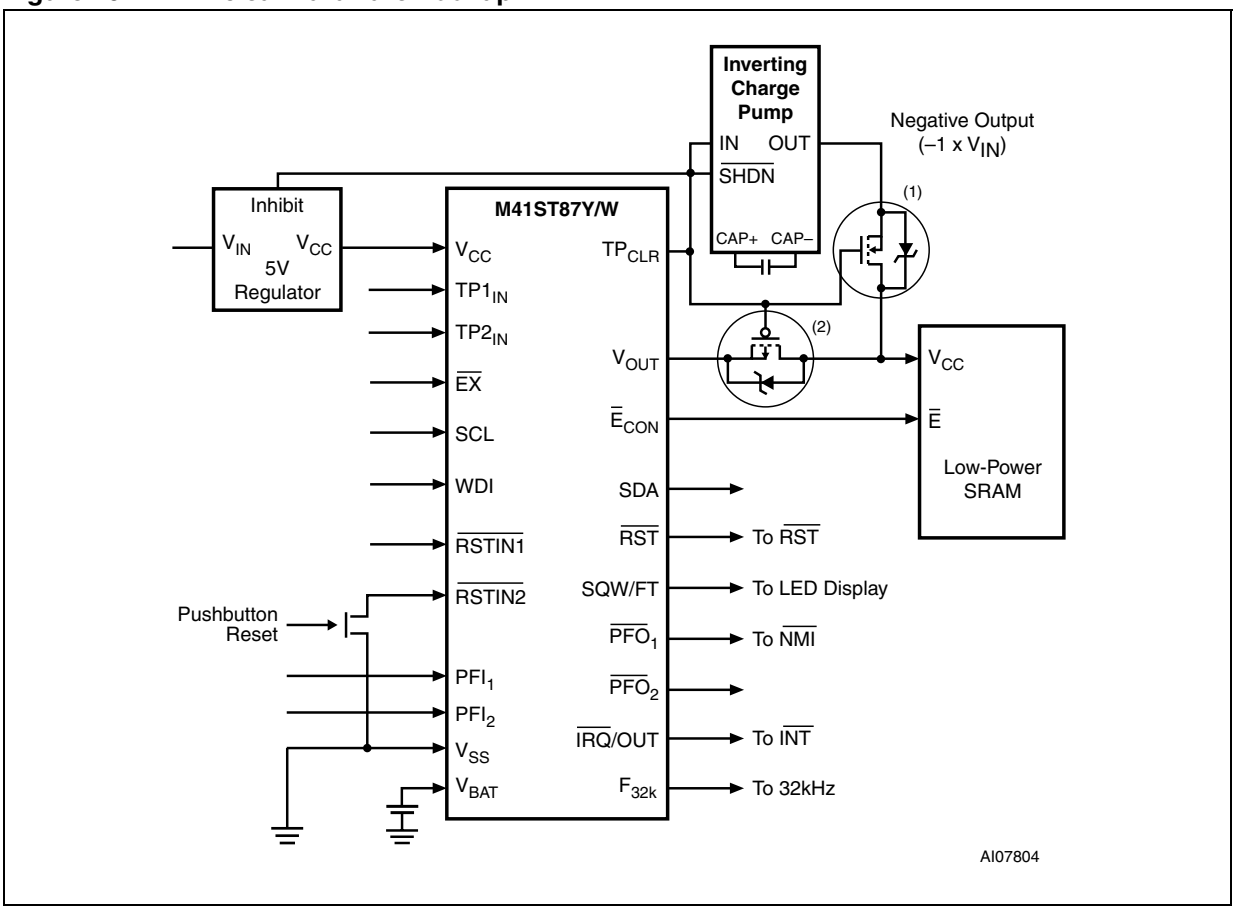
1. If connected to a negative charge pump device, this pin must be isolated from the charge pump by using both n-channel and p-channel MOSFETs as illustrated in *Figure 19 on page 24*.
2. If the device is in battery back-up; NOT on V_{CC} (see *Section 2.6.9: RAM clear external ($CLR1_{EXT}$ and $CLR2_{EXT}$) on page 21*).
3. If TIE_X = '1.'
4. If ABE = '1.'

Table 5. Tamper detect timing

Symbol	Parameter	CLRPW 1	CLRPW 0	Min	Typ	Max	Unit
t_{CLRD}(1)	Tamper RAM clear ext delay	X	X	1.0(2)	1.5	2.0	ms
t_{CLR}	Tamper clear timing	0	0		1		s
		0	1		4		s
		1	0		8		s
		1	1		16		s

1. With input capacitance = 70 pF and resistance = 50 Ω.
2. If the OF bit is set, t_{CLRD}(min) = 0.5 ms.

Figure 19. RAM clear hardware hookup



1. Most inverting charge pumps drive OUT to ground when device shut down is enabled (SHDN = logic low). Therefore, an n-channel enhancement mode MOSFET should be used to isolate the OUT pin from the V_{OUT} of the M41ST87.
2. In order to avoid turning on an on-chip parasitic diode when driving V_{OUT} negative, a p-channel enhancement mode MOSFET should be used to isolate the V_{OUT} pin from the negative voltage generated by the inverting charge pump.

2.7 Tamper detection operation

The tamper pins are triggered based on the state of an external switch. Two switch mode options are available, “normally open” or “normally closed,” based on the setting of the

tamper connect mode bit (TCM_X). If the selected switch mode is normally open (TCM_X = '1'), the tamper pin will be triggered by being connected to V_{SS} (if the TPM_X bit is set to '0') or to V_{CC} (if the TPM_X bit is set to '1'), through the closing of the external switch. When the external switch is closed, the tamper bit will be immediately set, allowing the user to determine if the device has been physically tampered with. If the selected switch mode is normally closed (TCM_X = '0'), the tamper pin will be triggered by being pulled to V_{SS} or to V_{OUT} (depending on the state of the TPM_X bit), through an internal pull-up/pull-down resistor as a result of opening the external switch.

When a tamper event occurs, the tamper bits (TB1 and/or TB2) will be immediately set if TEB_X = '1.'

If the tamper interrupt enable bit (TIE_X) is set to a '1,' the $\overline{IRQ}$/OUT pin will also be activated. The $\overline{IRQ}$/OUT output is cleared by a READ of the flags register (as seen in *Figure 23 on page 33*), a reset of the TIE bit to '0,' or the $\overline{RST}$ output is enabled.

Note: In order to avoid an inadvertent activation of the $\overline{IRQ}$/OUT pin due to a prior tamper event, the flag register (0Fh) should be read prior to resetting the TEB_X bit.

The tamper bits are “read only” bits and are reset only by writing the tamper enable bit (TEB_X) to '0.'

The tamper detect function operates both under normal power, and in battery backup. Even if the trigger event occurs during a power-down condition, the bit will be set correctly.

2.8 Sampling

As the switch mode normally closed (TCM_X = '0') requires a greater amount of current to maintain constant monitoring, the M41ST87Y/W offers a programmable tamper detect sampling bit (TDS_X) to reduce the current drawn on V_{CC} or V_{BAT} (see *Figure 16 on page 22*). When enabled, the sampling frequency is once per second (1Hz), for approximately 1 ms.

When TEB_X is disabled, no current will be drawn by the tamper detection circuit. After a tamper event has been detected, no additional current will be drawn.

Note: The oscillator must be running for tamper detection to operate in the sampling mode. If the oscillator is stopped, the tamper detection circuit will revert to constant monitoring.

Note: Sampling in the tamper high mode (TPM_X = '1') may be bypassed while on V_{CC} by connecting the TPX_{IN} pin to V_{CC} through an external resistor. This will allow constant monitoring when V_{CC} is “on” and revert to sampling when in battery backup (see Figure 13 on page 19).

2.9 Internal tamper pull-up/down current

Depending on the capacitive and resistive loading of the tamper pin input (TP_{XIN}), the user may require more or less current from the internal pull-up/down used when monitoring the normally closed switch mode. The state of the tamper current hi/tamper current low bit (TCHI/$\overline{TCLO}_X$) determines the sizing of the internal pull-up/-down. TCHI/$\overline{TCLO}_X$ = '1' uses a 1 MΩ pull-up/-down resistor, while TCHI/$\overline{TCLO}_X$ = '0' uses a 10 MΩ pull-up/-down resistor (see *Figure 17 on page 23*).

2.10 Avoiding inadvertent tampers (normally closed configuration)

In some applications it may be necessary to use a low pass filter to reduce electrical noise on the tamper input pin when the TCM_X bit = 0 (normally closed). This is especially true if the tamper detect switch is located some distance (> 6") from the tamper input pin. A low pass filter can prevent unwanted, higher frequency noise from inadvertently being detected as a tamper condition caused by the "antenna-effect" (produced by a longer signal wire or mesh). This low pass filter can be constructed using a series resistor (R) in conjunction with a capacitor (C) on the tamper input pin.

The cut-off frequency f_c is determined according to the formula:

$$f_c = 1/(2 \cdot Pi \cdot R \cdot C)$$

Figure 20. Low-pass filter implementation for noise immunity

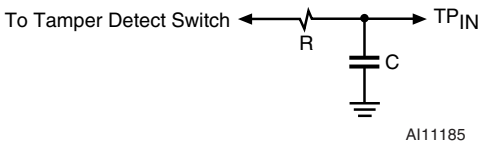


Table 6. Calculated cut-off frequency for typical capacitance and resistance values

R (Ω)	C (F)	f_c	$1/f_c$ (s)
1000	1.00E-09	15.9 MHz	6.28 µs
1000	1.00E-06	159.2 Hz	6.28 ms
5000	1.00E-09	31.8 kHz	31.4 µs
5000	1.00E-06	31.8 Hz	31.4 ms
10000	1.00E-09	15.9 kHz	62.8 µs
10000	1.00E-06	15.9 Hz	62.8 ms

2.11 Tamper event time-stamp

Regardless of which tamper occurs first, not only will the appropriate tamper bit be set, but the event will also be automatically time-stamped. This is accomplished by freezing the normal update of the clock registers (00h through 07h) immediately following a tamper event. Thus, when tampering occurs, the user may first read the time registers to determine exactly when the tamper event occurred, then re-enable the clock update to the current time (and reset the tamper bit, TB_X) by resetting the tamper enable bit (TEB_X).

The time update will then resume and the clock can be read to determine the current time. Both tamper enable bits (TEB_X) must always be set to '0' in order to read the current time.

In the event of multiple tampers, the time-stamp will reflect the initial tamper event.

Note: If the TEB_X bit is set, the tamper event time-stamp will take precedence over the power down time-stamp (see Section 3.0.1: Power-down time-stamp on page 28) and the HT bit (halt update) will not be set during the power-down event. If both are needed, the power down time-stamp may be accomplished by writing the time into the general purpose RAM memory space when $\overline{PFO}$ is asserted.

3 Clock operation

The eight byte clock register (see *Table 7 on page 29*) is used to both set the clock and to read the date and time from the clock, in a binary coded decimal format. Tenths/hundredths of seconds, seconds, minutes, and hours are contained within the first four registers.

Note: A WRITE to any clock register will result in the tenths/hundredths of seconds being reset to "00," and tenths/hundredths of seconds cannot be written to any value other than "00."

Bits D6 and D7 of clock register 03h (century/hours register) contain the CENTURY bit 0 (CB0) and CENTURY bit 1 (CB1). Bits D0 through D2 of register 04h contain the day (day of week). Registers 05h, 06h, and 07h contain the date (day of month), month, and years. The ninth clock register is the control register (this is described in the clock calibration section). Bit D7 of register 01h contains the STOP bit (ST). Setting this bit to a '1' will cause the oscillator to stop. If the device is expected to spend a significant amount of time on the shelf, the oscillator may be stopped to reduce current drain. When reset to a '0' the oscillator restarts within one second (typical).

Note: A WRITE to ANY location within the first eight bytes of the clock register (00h-07h), including the OFIE bit, CLRPW0 bit, CLRPW1 bit, THS bit, and so forth, will result in an update of the system clock and a reset of the divider chain. This could result in a significant corruption of the current time, especially if the HT bit (see Section 3.0.1: Power-down time-stamp) has not been previously reset. These non-clock related bits should be written prior to setting the clock, and remain unchanged until such time as a new clock time is also written.

The eight clock registers may be read one byte at a time, or in a sequential block. The control register (address location 08h) may be accessed independently. Provision has been made to assure that a clock update does not occur while any of the eight clock addresses are being read. If a clock address is being read, an update of the clock registers will be halted. This will prevent a transition of data during the READ.

3.0.1 Power-down time-stamp

Upon power-up following a power failure, the halt update bit (HT) will automatically be set to a '1.' This will prevent the clock from updating the TIMEKEEPER® registers, and will allow the user to read the time of the power-down event.

Note: When the HT bit is set or a tamper event occurs, the tenths/hundredths of a second register (00h) will automatically be reset to a value of "00." All other date and time registers (01h - 07h) will retain the value last updated prior to the power-down or tamper event. The internal clock remains accurate and no time is lost as a result of the zeroing of the tenth/hundredths of a second register. When updates are resumed (due to resetting the HT bit or TEB bit), the correct time will be displayed.

Resetting the HT bit to a '0' will allow the clock to update the TIMEKEEPER registers with the current time.

Note: If the TEB bit is set, the power down time-stamp will be disabled, and the tamper event time-stamp will take precedence (see Section 2.7: Tamper detection operation on page 24).

3.1 TIMEKEEPER® registers

The M41ST87Y/W offers 22 internal registers which contain clock, control, alarm, watchdog, flag, square wave, and tamper data. The clock registers are memory locations which contain external (user accessible) and internal copies of the data (usually referred to as BiPORT™ TIMEKEEPER cells). The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy. The internal divider (or clock) chain will be reset upon the completion of a WRITE to any clock address (00h to 07h).

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume either due to a stop condition or when the pointer increments to a non-clock or RAM address.

TIMEKEEPER and alarm registers store data in BCD format. Control, watchdog and square wave registers store data in binary format.

Table 7. TIMEKEEPER® register map

Addr	Data								Function/range BCD format	
	D7	D6	D5	D4	D3	D2	D1	D0		
00h	0.1 seconds				0.01 seconds				10s/100s seconds	00-99
01h	ST	10 seconds			Seconds				Seconds	00-59
02h	OFIE	10 minutes			Minutes				Minutes	00-59
03h	CB1	CB0	10 hours		Hours (24-hour format)				Century/ Hours	0-1/ 00-23
04h	TR	THS	CLRPW1	CLRPW0	32kE	Day of week			Day	01-7
05h	PFOD	0	10 date		Date: day of month				Date	01-31
06h	0	0	0	10M	Month				Month	01-12
07h	10 Years				Year				Year	00-99
08h	OUT	FT	S	Calibration					Control	
09h	WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	AFE	SQWE	ABE	Al 10M	Alarm month				Al month	01-12
0Bh	RPT4	RPT5	Al 10 date		Alarm date				Al date	01-31
0Ch	RPT3	HT	Al 10 hour		Alarm hour				Al hour	00-23
0Dh	RPT2	Alarm 10 minutes			Alarm minutes				Al min	00-59
0Eh	RPT1	Alarm 10 seconds			Alarm seconds				Al sec	00-59
0Fh	WDF	AF	0	BL	0	OF	TB1	TB2	Flags	
10h	0	0	0	0	0	0	0	0	Reserved	
11h	0	0	0	0	0	0	0	0	Reserved	
12h	0	0	0	0	0	0	0	0	Reserved	
13h	RS3	RS2	RS1	RS0	SQWOD	0	0	0	SQW	
14h	TEB1	TIE1	TCM1	TPM1	TDS1	$\overline{TCHI}$/ $\overline{TCLO}$1	$CLR1_{EXT}$	CLR1	Tamper1	
15h	TEB2	TIE2	TCM2	TPM2	TDS2	$\overline{TCHI}$/ $\overline{TCLO}$2	$CLR2_{EXT}$	CLR2	Tamper2	
16h-1Dh	ROM								Serial number	8-byte
1Eh-1Fh	Reserved									2-byte
20h-9Fh									128 user bytes	

Keys:

0 = Must be set to zero
32kE = 32 kHz output enable bit
ABE = Alarm in battery backup mode enable bit
AF = Alarm flag (read only)
AFE = Alarm flag enable bit
BL = Battery low flag (read only)
BMB0-BMB4 = Watchdog multiplier bits
CB0-CB1 = Century bits
CLR (1 and 2) = RAM clear bits
CLR (1 and 2)$_{EXT}$ = RAM clear external bits
CLRPW0 = RAM clear pulse width 0 bit
CLRPW1 = RAM clear pulse width 1 bit
FT = Frequency test bit
HT = Halt update bit
OF = Oscillator fail bit
OFIE = Oscillator fail interrupt enable bit
OUT = Output level
PFOD = Power-fail output open drain bit
RB0-RB1 = Watchdog resolution bits
RPT1-RPT5 = Alarm repeat mode bits
RS0-RS3 = SQW frequency
S = Sign bit
SQWE = Square wave enable
SQWOD = Square wave open drain bit
ST = Stop bit
TB (1 and 2) = Tamper bits (read only)
TCHI/$\overline{\text{TCLO}}$ (1 and 2) = Tamper current hi/tamper current low bits
TCM (1 and 2) = Tamper connect mode bits
TDS (1 and 2) = Tamper detect sampling bits
TEB (1 and 2) = Tamper enable bits
THS = Threshold bit
TIE (1 and 2) = Tamper interrupt enable bits
TPM (1 and 2) = Tamper polarity mode bits
TR = t_{rec} bit
WDS = Watchdog steering bit
WDF = Watchdog flag (read only)

3.2 Calibrating the clock

The M41ST87Y/W is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not exceed ±35 ppm (parts per million) oscillator frequency error at 25^{o}C, which equates to about ±1.53 minutes per month. When the Calibration circuit is properly employed, accuracy improves to better than ±2 ppm at 25°C.

The oscillation rate of crystals changes with temperature (see *Figure 21 on page 31*). Therefore, the M41ST87Y/W design employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in *Figure 22: Calibration waveform on page 32*. The number of times pulses which are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in the control register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The calibration bits occupy the five lower order bits (D4-D0) in the control register (08h). These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of

adjustment per calibration step in the calibration register. Assuming that the oscillator is running at exactly 32,768 Hz, each of the 31 increments in the calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M41ST87Y/W may require.

The first involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time. Calibration values, including the number of seconds lost or gained in a given period, can be found in application note AN934, “TIMEKEEPER® calibration.” This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses the calibration byte.

The second approach is better suited to a manufacturing environment, and involves the use of the SQW/FT pin. The pin will toggle at 512 Hz, when the stop bit (ST) is '0,' the frequency test bit (FT) is '1,' and SQWE is '0.'

Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.010124 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10 (XX001010) to be loaded into the calibration byte for correction. Note that setting or changing the calibration byte does not affect the frequency test output frequency.

If the SQWOD Bit = '1,' the SQW/FT pin is an open drain output which requires a pull-up resistor to V_{CC} for proper operation. A 500 to10 k resistor is recommended in order to control the rise time. The FT bit is cleared on power-down.

Figure 21. Crystal accuracy across temperature

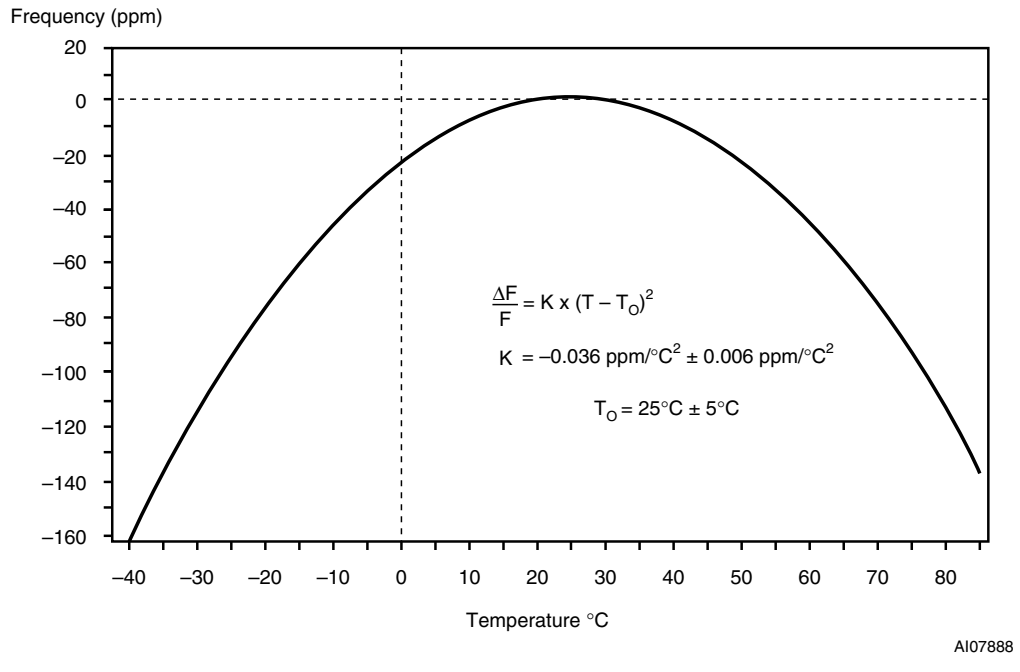
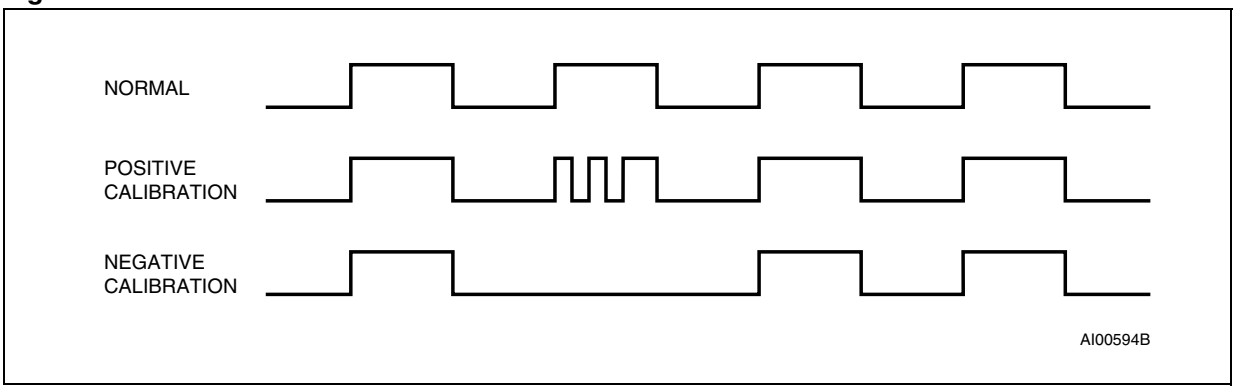


Figure 22. Calibration waveform



3.3 Setting alarm clock registers

Address locations 0Ah-0Eh contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific month, date, hour, minute, or second, or repeat every year, month, day, hour, minute, or second. It can also be programmed to go off while the M41ST87Y/W is in the battery back-up to serve as a system wake-up call.

Bits RPT5–RPT1 put the alarm in the repeat mode of operation. *Table 8 on page 33* shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

When the clock information matches the alarm clock settings based on the match criteria defined by RPT5–RPT1, the AF (alarm flag) is set. If AFE (alarm flag enable) is also set, the alarm condition activates the $\overline{\text{IRQ}}$/OUT pin as shown in *Figure 24 on page 33*. To disable alarm, write '0' to the alarm date register and to RPT5–RPT1.

If the address pointer is allowed to increment to the flag register address, an alarm condition will not cause the interrupt/flag to occur until the address pointer is moved to a different address. It should also be noted that if the last address written is the “alarm seconds,” the address pointer will increment to the flag address, causing this situation to occur.

The $\overline{\text{IRQ}}$/OUT output is cleared by a READ to the flags register. A subsequent READ of the flags register is necessary to see that the value of the alarm flag has been reset to '0.'

The $\overline{\text{IRQ}}$/OUT pin can also be activated in the battery backup mode. The $\overline{\text{IRQ}}$/OUT will go low if an alarm occurs and both ABE (alarm in battery backup mode enable) and AFE are set. The ABE and AFE bits are reset during power-up, therefore an alarm generated during power-up will only set AF. The user can read the flag register at system boot-up to determine if an alarm was generated while the M41ST87Y/W was in the deselect mode during power-up. *Figure 24 on page 33* illustrates the backup mode alarm timing.

Figure 23. Alarm interrupt reset waveform

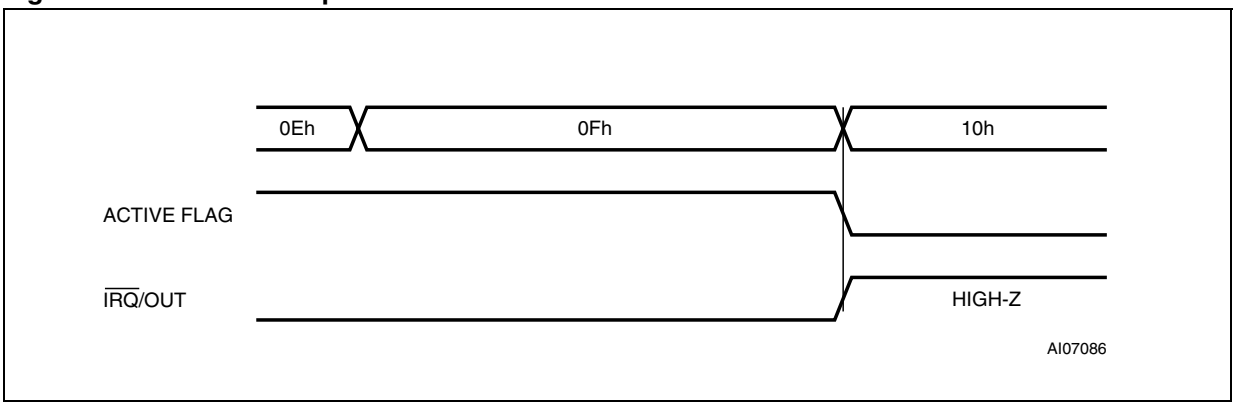
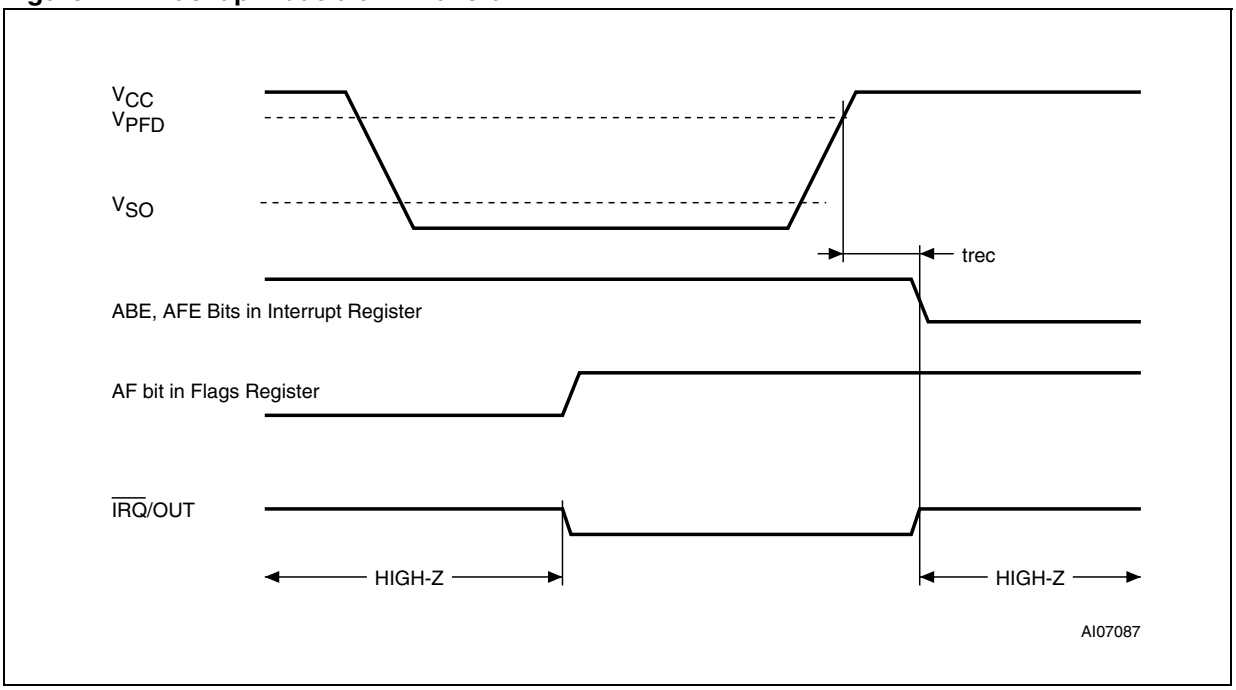


Table 8. Alarm repeat modes

RPT5	RPT4	RPT3	RPT2	RPT1	Alarm setting
1	1	1	1	1	Once per second
1	1	1	1	0	Once per minute
1	1	1	0	0	Once per hour
1	1	0	0	0	Once per day
1	0	0	0	0	Once per month
0	0	0	0	0	Once per year

Figure 24. Backup mode alarm waveform



3.4 Watchdog timer

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the watchdog register, address 09h. Bits BMB4-BMB0 store a binary multiplier and the two lower order bits RB1-RB0 select the resolution, where 00=1/16 second, 01=1/4 second, 10=1 second, and 11=4 seconds. The amount of time-out is then determined to be the multiplication of the five-bit multiplier value with the resolution. (For example: writing 00001110 in the watchdog register = 3*1 or 3 seconds).

Note: The accuracy of the timer is within ± the selected resolution.

If the processor does not reset the timer within the specified period, the M41ST87Y/W sets the WDF (watchdog flag) and generates a watchdog interrupt or a microprocessor reset.

The most significant bit of the watchdog register is the watchdog steering bit (WDS). When set to a '0,' the watchdog will activate the $\overline{IRQ}$/OUT pin when timed-out. When WDS is set to a '1,' the watchdog will output a negative pulse on the $\overline{RST}$ pin for t_{rec}. The watchdog register, FT, AFE, ABE and SQWE bits will reset to a '0' at the end of a watchdog time-out when the WDS bit is set to a '1.'

The watchdog timer can be reset by two methods: 1) a transition (high-to-low or low-to-high) can be applied to the watchdog input pin (WDI) or 2) the microprocessor can perform a WRITE of the watchdog register. The time-out period then starts over.

Note: The WDI pin should be tied to V_{SS} if not used.

In order to perform a software reset of the watchdog timer, the original time-out period can be written into the watchdog register, effectively restarting the count-down cycle.

Should the watchdog timer time-out, and the WDS bit is programmed to output an interrupt, either a transition of the WDI pin, or a value of 00h needs to be written to the watchdog register in order to clear the $\overline{IRQ}$/OUT pin. This will also disable the watchdog function until it is again programmed correctly. A READ of the flags register will reset the watchdog flag (bit D7; register 0Fh).

The watchdog function is automatically disabled upon power-up and the watchdog register is cleared.

3.5 Square wave output

The M41ST87Y/W offers the user a programmable square wave function which is output on the SQW/FT pin. RS3-RS0 bits located in 13h establish the square wave output frequency. These frequencies are listed in *Table 9*. Once the selection of the SQW frequency has been completed, the SQW/FT pin can be turned on and off under software control with the square wave enable bit (SQWE) located in Register 0Ah.

The SQW/FT output is programmable as an N-channel, open drain output driver, or a full-CMOS output driver. By setting the square wave open drain bit (SQWOD) to a '1,' the output will be configured as an open drain (with I_{OL} as specified in *Table 17 on page 42*). When SQWOD is set to '0,' the output will be configured as full-CMOS (sink and source current as specified in *Table 17 on page 42*).

Note: When configured as open drain (SQWOD = '1'), the SQW/FT pin requires an external pull-up resistor.

Table 9. Square wave output frequency

Square wave bits				Square wave	
RS3	RS2	RS1	RS0	Frequency	Units
0	0	0	0	None	–
0	0	0	1	32.768	kHz
0	0	1	0	8.192	kHz
0	0	1	1	4.096	kHz
0	1	0	0	2.048	kHz
0	1	0	1	1.024	kHz
0	1	1	0	512	Hz
0	1	1	1	256	Hz
1	0	0	0	128	Hz
1	0	0	1	64	Hz
1	0	1	0	32	Hz
1	0	1	1	16	Hz
1	1	0	0	8	Hz
1	1	0	1	4	Hz
1	1	1	0	2	Hz
1	1	1	1	1	Hz

3.6 Full-time 32 kHz square wave output

The M41ST87Y/W offers the user a special 32kHz square wave function which defaults to output on the F_{32k} pin (pin 21) as long as $V_{CC} \geq V_{SO}$, and the oscillator is running (ST bit = '0'). This function is available within one second (typ) of initial power-up and can only be disabled by setting the 32 kE bit to '0' or the ST bit to '1.' If not used, the F_{32k} pin should be disconnected and allowed to float.

Note: The F_{32k} pin is an open drain which requires an external pull-up resistor.

3.7 Power-on reset

The M41ST87Y/W continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point, the $\overline{RST}$ pulls low (open drain) and remains low on power-up for t_{rec} after V_{CC} passes V_{PFD}(max). The $\overline{RST}$ pin is an open drain output and an appropriate pull-up resistor should be chosen to control rise time.

Note: A power-on reset will result in resetting the following control bits to '0': OFIE, AFE, ABE, SQWE, FT, WDS, BMB0-BMB4, RB0, RB1, TIE1, and TIE2 (see Table 13 on page 39).

3.8 Reset inputs ($\overline{RSTIN1}$ & $\overline{RSTIN2}$)

The M41ST87Y/W provides two independent inputs which can generate an output reset. The function of these resets is identical to a reset generated by a power cycle. *Table 10* and *Figure 25* illustrate the AC reset characteristics of this function. Pulses shorter than t_{R1} and

t_{R2} will not generate a reset condition. $\overline{RSTIN1}$ and $\overline{RSTIN2}$ are each internally pulled up to V_{CC} through a 100 kΩ resistor.

Figure 25. $\overline{RSTIN1}$ & $\overline{RSTIN2}$ timing waveforms

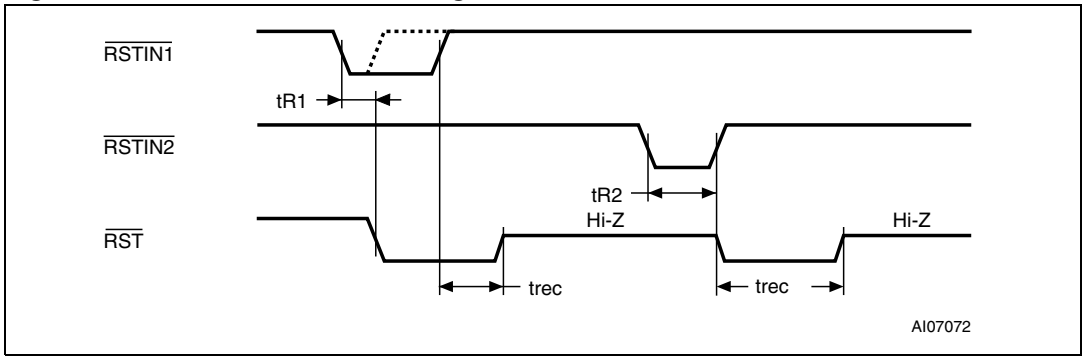


Table 10. Reset AC characteristics

Symbol	Parameter[1]	Min	Max	Unit
t_{R1}[2]	$\overline{RSTIN1}$ low to $\overline{RST}$ low (min pulse width)	100	200	ns
t_{R2}[2]	$\overline{RSTIN2}$ low to $\overline{RSTIN2}$ high (min pulse width)	100	200	ns
t_{rec}[3]	$\overline{RSTIN1}$ or $\overline{RSTIN2}$ high to $\overline{RST}$ high	96	98[3]	ms

1. Valid for ambient operating temperature: T_A = –40 to 85°C; V_{CC} = 4.5 to 5.5 V or 2.7 to 3.6 V (except where noted).
2. Pulse widths of less than 100 ns will result in no RESET (for noise immunity).
3. Programmable (see *Table 12 on page 39*). Same function as power-on reset.

3.9 Power-fail comparators (1 and 2)

Two power-fail inputs (PFI_1 and PFI_2) are compared to an internal reference voltage (1.25V). If either PFI_1 or PFI_2 is less than the power-fail threshold (V_{PFI}), the associated power-fail output ($\overline{PFO_1}$ or $\overline{PFO_2}$) will go low. This function is intended for use as an under-voltage detector to signal a failing power supply. Typically PFI_1 and PFI_2 are connected through external voltage dividers (see *Figure 4 on page 10*) to either the unregulated DC input (if it is available) or the regulated output of the V_{CC} regulator. The voltage divider can be set up such that the voltage at PFI_1 or PFI_2 falls below V_{PFI} several milliseconds before the regulated V_{CC} input to the M41ST87Y/W or the microprocessor drops below the minimum operating voltage.

During battery back-up, the power-fail comparator turns off and $\overline{PFO_1}$ and $\overline{PFO_2}$ go (or remain) low. This occurs after V_{CC} drops below V_{PFD}(min). When power returns, $\overline{PFO_1}$ and $\overline{PFO_2}$ are forced high, irrespective of V_{PFI} for the write protect time (t_{rec}), which is the time from V_{PFD}(max) until the inputs are recognized. At the end of this time, the power-fail comparator is enabled and $\overline{PFO_1}$ and $\overline{PFO_2}$ follow PFI_1 and PFI_2. If the comparator is unused, PFI_1 or PFI_2 should be connected to V_{SS} and the associated $\overline{PFO_1}$ or $\overline{PFO_2}$ left unconnected.

3.10 Power-fail outputs

The $\overline{PFO_1}$ and $\overline{PFO_2}$ outputs are programmable as N-channel, open drain output drivers, or full-CMOS output drivers. By setting the power-fail output open drain bit (PFOD) to a '1,' the

output will be configured as open drain (with I_{OL} as specified in *Table 17 on page 42*). When PFOD is set to '0,' the outputs will be configured as full-CMOS (sink and source current as specified in *Table 17 on page 42*).

Note: When configured as open drain (PFOD = '1'), $\overline{PFO}_1$ and $\overline{PFO}_2$ will require an external pull-up resistor.

3.11 Century bits

These two bits will increment in a binary fashion at the turn of the century, and handle leap years correctly. See *Table 11 on page 38* for additional explanation.

3.12 Output driver pin

When the TIE bit, OFIE bit, AFE bit, and watchdog register are not set to generate an interrupt, the $\overline{IRQ}$/OUT pin becomes an output driver that reflects the contents of D7 of the control register. In other words, when D7 (OUT Bit) is a '0,' then the $\overline{IRQ}$/OUT pin will be driven low. With the ABE bit set to '1,' the OUT pin will continue to be driven low in battery backup.

Note: The $\overline{IRQ}$/OUT pin is an open drain which requires an external pull-up resistor.

3.13 Battery low warning

The M41ST87Y/W automatically performs battery voltage monitoring upon power-up and at factory-programmed time intervals of approximately 24 hours. The battery low (BL) bit, bit D4 of flags register 0Fh, will be asserted if the battery voltage is found to be less than approximately 2.5 V. The BL bit will remain asserted until completion of battery replacement and subsequent battery low monitoring tests, either during the next power-up sequence or the next scheduled 24-hour interval.

If a battery low is generated during a power-up sequence, this indicates that the battery is below approximately 2.5 volts and may not be able to maintain data integrity in the SRAM. Data should be considered suspect and verified as correct. A fresh battery should be installed.

If a battery low indication is generated during the 24-hour interval check, this indicates that the battery is near end of life. However, data is not compromised due to the fact that a nominal V_{CC} is supplied. In order to insure data integrity during subsequent periods of battery back-up mode, the battery should be replaced. The battery may be replaced while V_{CC} is applied to the device.

The M41ST87Y/W only monitors the battery when a nominal V_{CC} is applied to the device. Thus applications which require extensive durations in the battery back-up mode should be powered-up periodically (at least once every few months) in order for this technique to be beneficial. Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique.

3.14 t_{rec} bit

Bit D7 of clock register 04h contains the t_{rec} bit (TR). t_{rec} refers to the automatic continuation of the deselect time after V_{CC} reaches V_{PFD}. This allows for a voltage settling time before WRITEs may again be performed to the device after a power-down condition. The t_{rec} bit will allow the user to set the length of this deselect time as defined by *Table 12 on page 39*.

3.15 Electronic serial number

The M41ST87Y/W has a unique 8-byte lasered, serial number with parity. This serial number is “read only” and is generated such that no two devices will contain an identical number.

3.16 Oscillator stop detection

If the oscillator fail (OF) bit is internally set to a '1,' this indicates that the oscillator has either stopped, or was stopped for some period of time and can be used to judge the validity of the clock and date data. This bit will be set to '1' any time the oscillator stops. The following conditions can cause the OF bit to be set:

- The first time power is applied (defaults to a '1' on power-up).
- The voltage present on V_{CC} or battery is insufficient to support oscillation.
- The ST bit is set to '1.'

If the oscillator fail interrupt enable bit (OFIE) is set to a '1,' the $\overline{IRQ}$/OUT pin will also be activated. The $\overline{IRQ}$/OUT output is cleared by resetting the OF bit to '0,' resetting the OFIE bit to '0,' or the $\overline{RST}$ output is enabled (NOT by reading the flag register).

The OF bit will remain set to '1' until written to logic '0.' The oscillator must start and have run for at least 4 seconds before attempting to reset the OF bit to '0.' This function operates both under normal power and in battery backup. If the trigger event occurs during a power-down condition, this bit will be set correctly.

Note: The ABE bit must be set to '1' for the $\overline{IRQ}$/OUT pin to be activated in battery backup.

3.17 Initial power-on defaults

See *Table 13 on page 39*.

Table 11. Century bits examples

CB0	CB1	Leap year?	Example(1)
0	0	Yes	2000
0	1	No	2100
1	0	No	2200
1	1	No	2300

1. Leap year occurs every four years (for years evenly divisible by four), except for years evenly divisible by 100. The only exceptions are those years evenly divisible by 400 (the year 2000 was a leap year, year 2100 is not).

Table 12. t_{rec} definitions

t_{rec} bit (TR)	STOP bit (ST)	t_{rec} time		Units
		Min	Max	
0	0	96	98(1)	ms
0	1	40	200	ms
1	X	50	2000	µs

1. Default setting

Table 13. Default values

Condition	TR	ST	OF	OFIE	HT(1)	Out	FT	AFE
Initial power-up	0	0	1	0	1	1	0	0
Subsequent power-up (with battery backup)(2)(3)	UC	UC	UC	0 ⇑	1 ⇓	UC	0 ⇓	0 ⇑

Condition	ABE	SQWE	SQWOD	PFOD	Watchdog register(4)
Initial power-up	0	0	1	1	0
Subsequent power-up (with battery backup)(2)(3)	0 ⇑	0 ⇑	UC	UC	0 ⇓

Condition	32kE	THS	TEB1 and 2	TCM1 and 2	TPM1 and 2	TDS1 and 2
Initial power-up	1(5)	0	0	0	0	0
Subsequent power-up (with battery backup)(2)	UC	UC	UC	UC	UC	UC

Condition	TCHI/$\overline{\text{TCLO}}$1 and 2	CLR1 and 2	TIE1 and 2	CLRPW0	CLRPW1	$CLR1_{EXT}$ and $CLR2_{EXT}$
Initial power-up	0	0	0	0	0	0
Subsequent power-up (with battery backup)(2)	UC	UC	0 ⇑	UC	UC	UC

1. When TEB_X is set to '1,' the HT bit will not be set on power-down (tamper time-stamp will have precedence).
2. UC = unchanged.
3. ⇑ = V_{CC} rising; ⇓ = V_{CC} falling.
4. WDS, BMB0-BMB4, RB0, RB1.
5. 32 kHz output valid only on V_{CC}.

Note: All other control bits are undetermined.

4 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 14. Absolute maximum ratings

Symbol	Parameter		Value	Unit
T_{STG}	Storage temperature (V_{CC} off, oscillator off)		–55 to 125	°C
T_{SLD}(1)	Lead solder temperature for 10 seconds		240	°C
V_{IO}	Input or output voltage		–0.3 to V_{CC}+0.3	V
V_{CC}	Supply voltage	M41ST87Y	–0.3 to 7.0	V
		M41ST87W	–0.3 to 4.6	V
I_O	Output current		20	mA
P_D	Power dissipation		1	W

1. Reflow at peak temperature of 240°C (total thermal budget not to exceed 180°C between 90 to 150 seconds).

Caution: *Negative undershoots below –0.3 V are not allowed on any pin while in the battery backup mode.*

5 DC and AC parameters

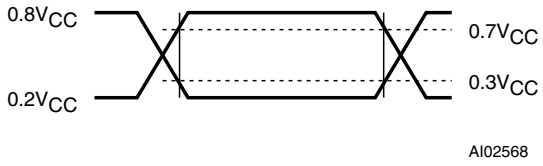
This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 15. DC and AC measurement conditions

Parameter	M41ST87Y	M41ST87W
V_{CC} supply voltage	4.5 to 5.5 V	2.7 to 3.6 V
Ambient operating temperature	–40 to 85°C	–40 to 85°C
Load capacitance (C_L)	100 pF	50 pF
Input rise and fall times	≤ 50 ns	≤ 50 ns
Input pulse voltages	0.2 to 0.8V_{CC}	0.2 to 0.8V_{CC}
Input and output timing ref. voltages	0.3 to 0.7V_{CC}	0.3 to 0.7V_{CC}

Note: Output high Z is defined as the point where data is no longer driven.

Figure 26. AC testing input/output waveforms



Note: 50 pF for M41ST87W.

Table 16. Capacitance

Symbol	Parameter[1][2]	Min	Max	Unit
C_{IN}	Input capacitance		7	pF
C_{OUT}[3]	Output capacitance		10	pF
t_{LP}	Low-pass filter input time constant (SDA and SCL)		50	ns

1. Effective capacitance measured with power supply at 5 V. Sampled only, not 100% tested.
2. At 25°C, f = 1 MHz.
3. Outputs are deselected.

Table 17. DC characteristics

Sym	Parameter	Test condition(1)	M41ST87Y			M41ST87W			Unit
			Min	Typ	Max	Min	Typ	Max	
I_{BAT}(2)	Battery current OSC ON	T_A = 25°C, V_{CC} = 0 V, V_{BAT} = 3 V		500	700		500	700	nA
	Battery current OSC OFF			50			50		nA
I_{CC1}	Supply current	f = 400 kHz			1.4			0.75	mA
I_{CC2}	Supply current (standby)	SCL, SDA = V_{CC} – 0.3 V			1			0.50	mA
I_{LI}(3)	Input leakage current	0V ≤ V_{IN} ≤ V_{CC}			±1			±1	µA
	Input leakage current (PFI)		–25	2	25	–25	2	25	nA
I_{LO}(4)	Output leakage current	0V ≤ V_{IN} ≤ V_{CC}			±1			±1	µA
I_{OUT1}(5)	V_{OUT} current (active)	V_{OUT1} > V_{CC} – 0.3 V			175			100	mA
I_{OUT2}	V_{OUT} current (battery backup)	V_{OUT2} > V_{BAT} – 0.3 V			100			100	µA
V_{IH}	Input high voltage		0.7V_{CC}		V_{CC} + 0.3	0.7V_{CC}		V_{CC} + 0.3	V
V_{IL}	Input low voltage		–0.3		0.3V_{CC}	–0.3		0.3V_{CC}	V
V_{BAT}	Battery voltage		2.5	3.0	3.5(6)	2.5	3.0	3.5(6)	V
V_{OH}(7)	Output high voltage	I_{OH} = –1.0 mA	2.4			2.4			V
	Pull-up supply voltage (open drain)	$\overline{IRQ}$/OUT, $\overline{RST}$, F_{32k}			5.5			3.6	V
V_{OHB}(8)	V_{OH} (battery backup)	I_{OUT2} = –1.0 µA(9)		2.9			2.9		V
V_{OL}	Output low voltage	I_{OL} = 3.0 mA			0.4			0.4	V
	Output low voltage (open drain)(10)	I_{OL} = 10 mA			0.4			0.4	V
V_{PFD}	Power fail deselect	THS bit = 0	4.20	4.35	4.50	2.55	2.62	2.70	V
		THS bit = 1	4.50	4.60	4.75	2.80	2.88	3.00	V
V_{PFI1}	PFI input threshold	V_{CC} = 5 V(Y) V_{CC} = 3 V(W)	1.225	1.250	1.275	1.225	1.250	1.275	V
	PFI hysteresis	PFI rising		20	70		20	70	mV
V_{PFI2}	PFI input threshold	V_{CC} = 5 V(Y) V_{CC} = 3 V(W)	1.225	1.250	1.275	1.225	1.250	1.275	V
	PFI hysteresis	PFI rising		20	70		20	70	mV
V_{SO}	Battery backup switchover			2.5			2.5		V
R_{SW}	Switch resistance on tamper pin				500			500	W

1. Valid for ambient operating temperature: T_A = –40 to 85°C; V_{CC} = 4.5 to 5.5 V or 2.7 to 3.6 V (except where noted).
2. Measured with V_{OUT} and $\overline{E}_{CON}$ open. Not including tamper detection current (see *Table 4 on page 22*).
3. $\overline{RSTIN1}$ and $\overline{RSTIN2}$ internally pulled-up to V_{CC} through 100 KΩ resistor. WDI internally pulled-down to V_{SS} through 100 KΩ resistor.

4. Outputs deselected.
5. External SRAM must match RTC supervisor chip V_{CC} specification.
6. For rechargeable backup, V_{BAT} (max) may be considered V_{CC}.
7. For $\overline{PFO}_1$ and $\overline{PFO}_2$ (if PFOD = '0'), SQW/FT (if SQWOD = '0'), and TP_{CLR} pins (CMOS).
8. Conditioned output ($\overline{E}_{CON}$) can only sustain CMOS leakage current in the battery backup mode. Higher leakage currents will reduce battery life.
9. TP_{CLR} output can source –300 µA (typ) for V_{BAT} = 2.9 V.
10. For $\overline{IRQ}$/OUT, SQW/FT (if SQWOD = '1'), $\overline{PFO}_1$ and $\overline{PFO}_2$ (if PFOD = '1'), $\overline{RST}$, SDA, and F_{32k} pins (open drain).

Figure 27. Power down/up mode AC waveforms

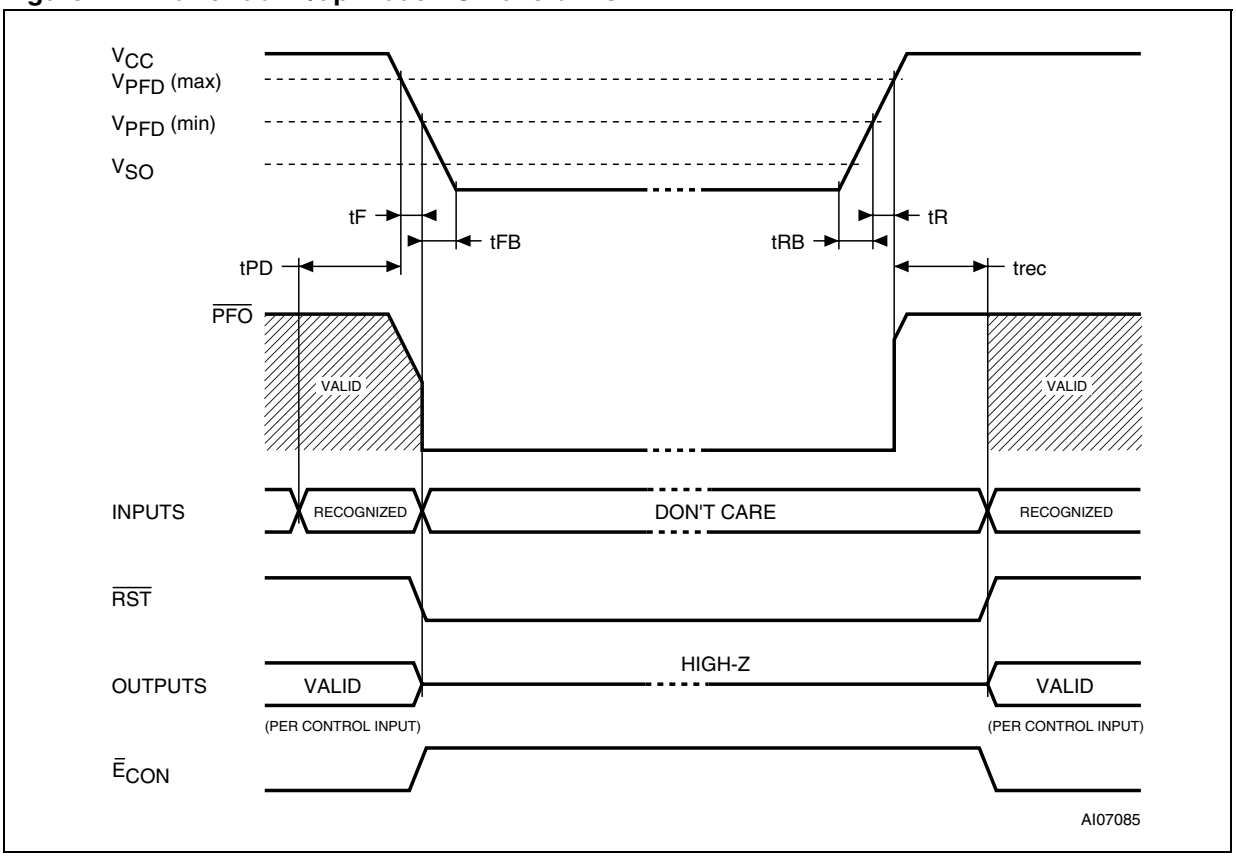


Table 18. Power down/up AC characteristics

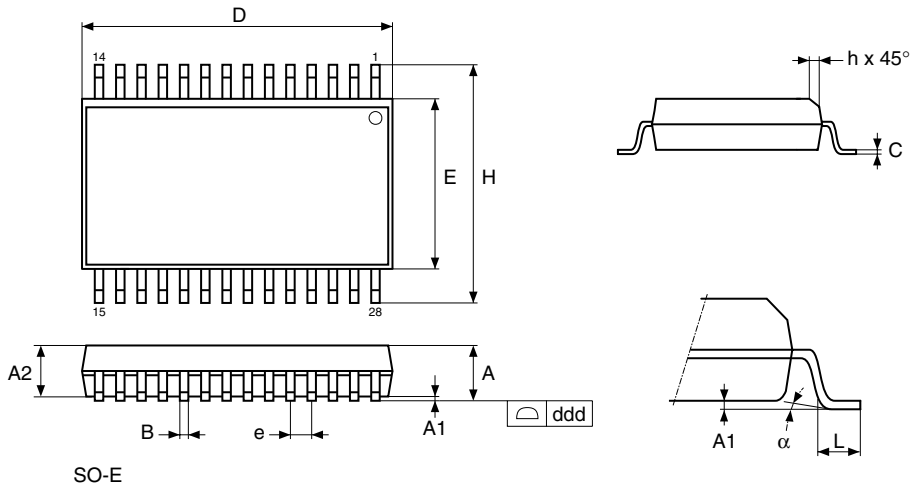
Symbol	Parameter[1]	Min	Typ	Max	Unit
t_F[2]	V_{PFD}(max) to V_{PFD}(min) V_{CC} fall time	300			µs
t_{FB}[3]	V_{PFD}(min) to V_{SS} V_{CC} fall time	10			µs
t_{PD}	$\overline{EX}$ at V_{IH} before power down	0			µs
t_{PFD}	PFI to $\overline{PFO}$ propagation delay		15	25	µs
t_R	V_{PFD}(min) to V_{PFD}(max) V_{CC} rise time	10			µs
t_{RB}	V_{SS} to V_{PFD}(min) V_{CC} rise time	1			µs
t_{rec}	Power-up deselect time	96		98[4]	ms

1. Valid for ambient operating temperature: T_A = –40 to 85°C; V_{CC} = 4.5 to 5.5 V or 2.7 to 3.6 V (except where noted).
2. V_{PFD}(max) to V_{PFD}(min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD}(min).
3. V_{PFD}(min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.
4. Programmable (see *Table 12 on page 39*)

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 28. SOX28 – 28-lead plastic small outline, 300 mils, embedded crystal outline



Note: Drawing is not to scale.

Table 19. SOX28 – 28-lead plastic small outline, 300 mils, embedded crystal, mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.44	2.69		0.096	0.106
A1		0.15	0.31		0.006	0.012
A2		2.29	2.39		0.090	0.094
B		0.41	0.51		0.016	0.020
C		0.20	0.31		0.008	0.012
D		17.91	18.01		0.705	0.709
ddd			0.10			0.004
E		7.57	7.67		0.298	0.302
e	1.27	–	–	0.050	–	–
H		10.16	10.52		0.400	0.414
L		0.51	0.81		0.020	0.032
a		0°	8°		0°	8°
N	28			28		

7 Part numbering

Table 20. Ordering information scheme

Example: M41ST 87Y MX 6

Device type

M41ST

Supply voltage and write protect voltage

87Y = V_{CC} = 4.75 to 5.5 V

THS bit = '1': 4.50 V ≤ V_{PFD} ≤ 4.75 V

V_{CC} = 4.5 to 5.5 V

THS bit = '0': 4.20 V ≤ V_{PFD} ≤ 4.50 V

87W = V_{CC} = 3.0 to 3.6 V;

THS bit = '1': 2.80 V ≤ V_{PFD} ≤ 3.00 V

V_{CC} = 2.7 to 3.6 V;

THS bit = '0': 2.55 V ≤ V_{PFD} ≤ 2.70 V

Package

MX(1)(2)= SOX28

Temperature range

6 = –40 to 85°C

Shipping method

blank = ECOPACK® package, tubes

TR = ECOPACK® package, tape & reel

1. The SOX28 package includes an embedded 32,768 Hz crystal.
2. Lead-free second level interconnect and RoHS compliant (by exemption).

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

8 Revision history

Table 21. Document revision history

Date	Revision	Changes
May-2002	1	First issue.
23-Apr-2003	2	Document promoted to Preliminary Data.
10-Jul-2003	2.1	Update tamper information (*Figure 3*, *4*, *13*, *14*, *15*; *Table 17*, *4*, *12*).
11-Sep-2003	2.2	Update electrical, charge pump, and clock information (*Table 17*; *Figure 4*, *18*, *19*).
15-Jun-2004	3	Reformatted; added Lead-free information; updated characteristics (*Figure 2*; *Table 1*, *14*, *17*, *20*).
7-Sep-2004	4	Update maximum ratings (*Table 14*).
29-Jun-2005	5	Clarify NC connections, add Inadvertent Tamper, update MX attribute (*Figure 2*, *20*; *Table 1*, *6*, *20*).
28-Mar-2006	6	Update to “Avoiding Inadvertent Tamper paragraph“ paragraph.
10-Sep-2008	7	Reformatted document and title change; updated cover page, *Figure 3*, *14*, *19*, *Section 6: Package mechanical data*.

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