

GENERAL PURPOSE PHEMT

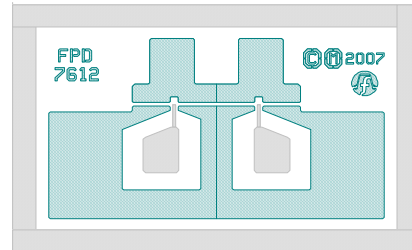
FEATURES:

- 20.5 dBm Output Power (P1dB)
- 13 dB Power Gain at 12 GHz
- 17 dB Maximum Stable Gain at 12 GHz
- 11 dB Maximum Stable Gain at 18 GHz
- 45% Power-Added Efficiency

GENERAL DESCRIPTION:

The FPD7612 is an AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (PHEMT), featuring a 0.25 μm by 200 μm Schottky barrier gate, defined by high-resolution stepper-based photolithography. The recessed gate structure minimizes parasitics to optimize performance. The epitaxial structure and processing have been optimized for reliable high-power applications.

LAYOUT:



TYPICAL APPLICATIONS:

- Narrowband and broadband high-performance amplifiers
- SATCOM uplink transmitters
- PCS/Cellular low-voltage high-efficiency output amplifiers
- Medium-haul digital radio transmitters

ELECTRICAL SPECIFICATIONS¹:

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|----------------------|---------------------------------------|-----------|----------|-----|----------------------|
| Power at 1dB Gain Compression | P1dB | VDS = 5 V; IDS = 50% IDSS | 19 | 20.5 | | dBm |
| Power Gain at P1dB | G1dB | VDS = 5 V; IDS = 50% IDSS | 11.0 | 13.0 | | dB |
| Noise Figure | N.F. min | VDS = 5 V; IDS = 50% IDSS | | 1.2 | | dB |
| Power-Added Efficiency | PAE | VDS = 5V; IDS = 50% IDSS; POUT = P1dB | | 45 | | % |
| Maximum Stable Gain (S21/S12) f = 12 GHz f = 24 GHz | MSG | VDS = 5 V; IDS = 50% IDSS | 16 9.5 | 17 11 | | dB |
| Saturated Drain-Source Current | IDSS | VDS = 1.3 V; VGS = 0 V | 45 | 60 | 75 | mA |
| Maximum Drain-Source Current | IMAX | VDS = 1.3 V; VGS \cong +1 V | | 120 | | mA |
| Transconductance | GM | VDS = 1.3 V; VGS = 0 V | | 80 | | mS |
| Gate-Source Leakage Current | IGSO | VGS = -5 V | | 1 | 10 | μA |
| Pinch-Off Voltage | VP | VDS = 1.3 V; IDS = 0.2 mA | 0.7 | 1.0 | 1.3 | V |
| Gate-Source Breakdown Voltage | VBDGS | IGS = 0.2 mA | 12.0 | 14.0 | | V |
| Gate-Drain Breakdown Voltage | VBDGD | IGD = 0.2 mA | 14.5 | 16.0 | | V |
| Thermal Resistivity (see Notes) | θ_{JC} | VDS > 3V | | 280 | | $^{\circ}\text{C/W}$ |
| Thermal Resistivity (see Notes) | θ_{JC} | VDS > 6V | | 20 | | $^{\circ}\text{C/W}$ |

Note:¹ T_{Ambient} = 22°C; RF specifications measured at f = 12 GHz using CW signal

ABSOLUTE MAXIMUM RATING¹:

| PARAMETER | SYMBOL | TEST CONDITIONS | ABSOLUTE MAXIMUM |
|---|--------|---------------------------------|------------------|
| Drain-Source Voltage | VDS | -3V < VGS < -0.5V ⁶ | 8V |
| Gate-Source Voltage | VGS | 0V < VDS < +8V | -3V |
| Drain-Source Current | IDS | For VDS < 2V | IDss |
| Gate Current | IG | Forward or reverse current | 10mA |
| RF Input Power | PIN | Under any acceptable bias state | 20dBm |
| Channel Operating Temperature | TCH | Under any acceptable bias state | 175°C |
| Storage Temperature | TSTG | Non-Operating Storage | -65°C to 150°C |
| Total Power Dissipation | PTOT | See De-Rating Note below | 0.5W |
| Gain Compression | Comp. | Under any bias conditions | 5dB |
| Simultaneous Combination of Limits ⁴ | | 2 or more Max. Limits | 80% |

Notes:

¹T_{Ambient} = 22°C unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device

²Total Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$,
where P_{DC}: DC Bias Power, P_{IN}: RF Input Power, P_{OUT}: RF Output Power

³Total Power Dissipation to be de-rated as follows above 22°C:

$$P_{TOT} = 0.5 - (0.0036W/°C) \times T_{HS}$$

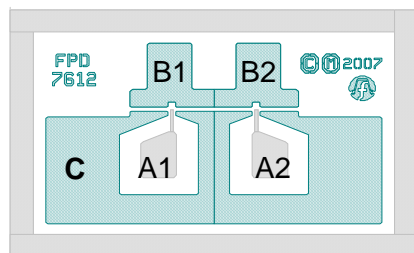
where T_{HS} = heatsink or ambient temperature above 22°C

Example: For a 85°C carrier temperature: $P_{TOT} = 0.5 - (0.0036 \times (85 - 22)) = 0.27W$

⁴Users should avoid exceeding 80% of 2 or more Limits simultaneously

⁵ Thermal Resitivity specification assumes a Au/Sn eutectic die attach onto a Au-plated copper heatsink or rib.

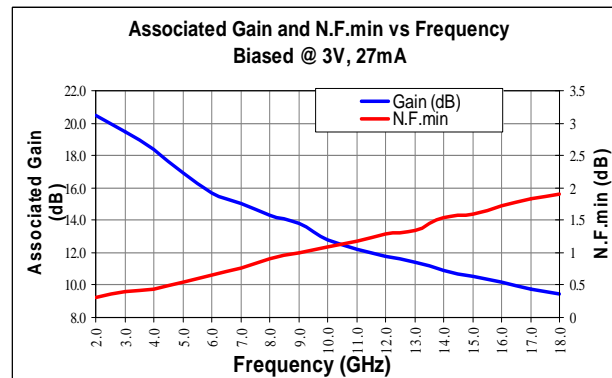
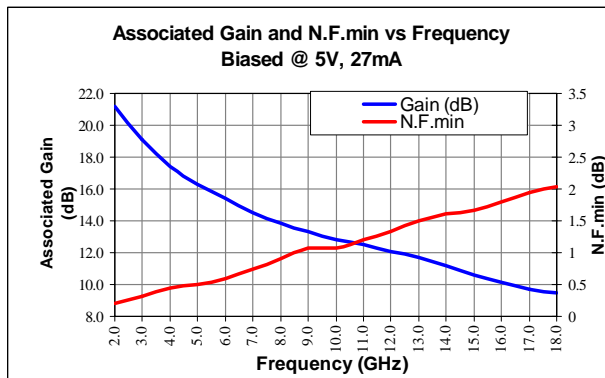
⁶ Operating at absolute maximum VD continuously is not recommended. If operation at 8V is considered then IDS must be reduced in order to keep the part within it's thermal power dissipation limits. Therefore VGS is restricted to < -0.5V.

PAD LAYOUT


| PAD | DESCRIPTION | PIN COORDINATES (µm) |
|-------|-------------|----------------------|
| A1/A2 | Gate Pads | 190/330, 120 |
| B1/B2 | Drain Pads | 200/320, 240 |
| C | Source Pad | |

Note: Co-ordinates are referenced from the bottom left hand corner of the die to the centre of bond pad opening

| DIE SIZE (µm) | DIE THICKNESS (µm) | MIN. BOND PAD OPENING (µm x µm) |
|---------------|--------------------|---------------------------------|
| 520 x 335 | 75 | 45 x 45 |

TYPICAL MEASURED PERFORMANCE :

NOISE PARAMETERS : (BIASED @ VDS=3.0V, IDS=27mA)

| Freq (GHz) | N.F.min (dB) | Rn/50 (Ohms) | Gamma Opt. | |
|---------------|-----------------|-----------------|------------|--------|
| | | | Mag. | Angle |
| 2.00 | 0.31 | 0.28 | 0.78 | 9.63 |
| 3.00 | 0.39 | 0.28 | 0.70 | 18.43 |
| 4.00 | 0.44 | 0.26 | 0.74 | 28.57 |
| 5.00 | 0.54 | 0.24 | 0.61 | 35.40 |
| 6.00 | 0.65 | 0.23 | 0.63 | 44.37 |
| 7.00 | 0.75 | 0.23 | 0.54 | 51.10 |
| 8.00 | 0.90 | 0.22 | 0.49 | 58.43 |
| 9.00 | 1.07 | 0.21 | 0.44 | 68.47 |
| 10.00 | 1.08 | 0.20 | 0.43 | 73.30 |
| 11.00 | 1.09 | 0.20 | 0.44 | 80.63 |
| 12.00 | 1.28 | 0.20 | 0.38 | 92.87 |
| 13.00 | 1.55 | 0.19 | 0.34 | 104.10 |
| 14.00 | 1.66 | 0.17 | 0.32 | 111.83 |
| 15.00 | 1.60 | 0.15 | 0.30 | 120.60 |
| 16.00 | 1.72 | 0.15 | 0.32 | 124.47 |
| 17.00 | 1.83 | 0.14 | 0.28 | 144.77 |
| 18.00 | 1.90 | 0.13 | 0.20 | 158.23 |

PREFERRED ASSEMBLY INSTRUCTIONS:

GaAs devices are fragile and should be handled with great care. Specially designed collets should be used where possible.

The recommended die attach is gold/tin eutectic solder under a nitrogen atmosphere. Stage temperature should be 280-290°C; maximum time at temperature is one minute. The recommended wire bond method is thermo-compression wedge bonding with 0.7 or 1.0 mil (0.018 or 0.025 mm) gold wire. Stage temperature should be 250-260°C.

ORDERING INFORMATION:

| PART NUMBER | DESCRIPTION |
|-------------|-------------|
| FPD7612 | Die |

HANDLING PRECAUTIONS:


To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 0 (0-250 V) as defined in JEDEC Standard No. 22-A114. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

APPLICATION NOTES & DESIGN DATA:

Application Notes and design data including S-parameters, noise parameters and device model are available on request

DISCLAIMERS:

This product is not designed for use in any space based or life sustaining/supporting equipment.