Integrated Circuit Systems, Inc.

ICS9LPR426A
Advance Information

Low Power Programmable Timing Control Hub™ for P4™ processor

Recommended Application:

Low Power CK410M Compliant Main Clock

Output Features:

- 2 - 0.7V push-pull differential CPU pairs
- 5 - 0.7V push-pull differential PCIEX pairs
- 1 - 0.7V push-pull differential SATA pair
- 1 - 0.7V push-pull differential CPU/PCIEX selectable pair
- 1 - 0.7V push-pull differential 27MHz/LCDCLK/PCIEX selectable pair
- 4 - PCI (33MHz)
- 2 - PCICLK_F, (33MHz) free-running
- 1 - USB, 48MHz
- 2 - REF, 14.318MHz

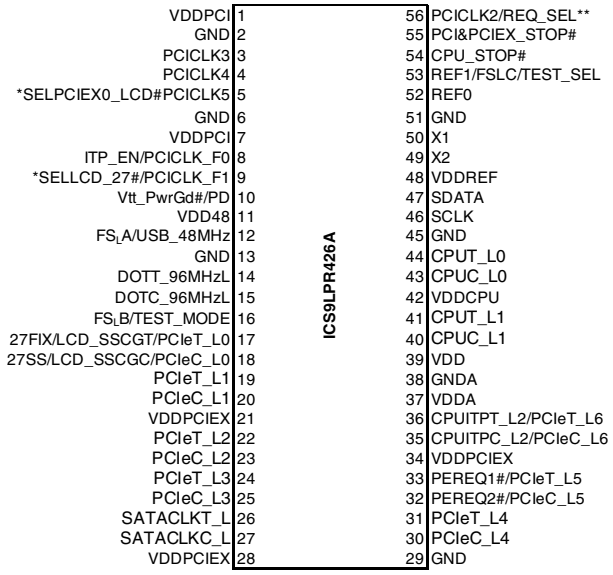
Key Specifications:

- CPU outputs cycle-cycle jitter < 85ps
- PCIEX outputs cycle-cycle jitter < 125ps
- SATA outputs cycle-cycle jitter < 125ps
- PCI outputs cycle-cycle jitter < 500ps
- +/- 100ppm frequency accuracy on CPU, PCIEX and SATA clocks
- +/- 100ppm frequency accuracy on USB clocks

Features/Benefits:

- Supports tight ppm accuracy clocks for Serial-ATA and PCIEX
- Supports programmable spread percentage and frequency
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning
- PEREQ# pins to support PCIEX power management.
- Low power differential clock outputs (No 50W resistor to GND needed)

Pin Configuration



56-TSSOP

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

Functionality Table

Bit 4	Bit 3	Bit 2 FS_LC	Bit 1 FS_LB	Bit 0 FS_LA	CPU MHz	PCIEX MHz	PCI MHz	SATA MHz
0	0	0	0	0	266.66	99.75	33.33	100.00
0	0	0	0	1	133.33	99.75	33.33	100.00
0	0	0	1	0	200.00	99.75	33.33	100.00
0	0	0	1	1	166.66	99.75	33.33	100.00
0	0	1	0	0	333.33	99.75	33.33	100.00
0	0	1	0	1	100.00	99.75	33.33	100.00
0	0	1	1	0	400.00	99.75	33.33	100.00
0	0	1	1	1	200.00	99.75	33.33	100.00
0	1	0	0	0	266.66	99.75	33.33	100.00
0	1	0	0	1	133.33	99.75	33.33	100.00
0	1	0	1	0	200.00	99.75	33.33	100.00
0	1	0	1	1	166.66	99.75	33.33	100.00
0	1	1	0	0	333.33	99.75	33.33	100.00
0	1	1	0	1	100.00	99.75	33.33	100.00
0	1	1	1	0	400.00	99.75	33.33	100.00
0	1	1	1	1	200.00	99.75	33.33	100.00
1	0	0	0	0	269.33	100.75	33.33	100.00
1	0	0	0	1	271.99	101.75	33.33	100.00
1	0	0	1	0	274.66	102.74	33.33	100.00
1	0	0	1	1	277.33	103.74	33.33	100.00
1	0	1	0	0	279.99	104.74	33.33	100.00
1	0	1	0	1	282.66	105.74	33.33	100.00
1	0	1	1	0	285.33	106.73	33.33	100.00
1	0	1	1	1	287.99	107.73	33.33	100.00
1	1	0	0	0	269.33	108.73	33.33	100.00
1	1	0	0	1	271.99	109.73	33.33	100.00
1	1	0	1	0	274.66	110.72	33.33	100.00
1	1	0	1	1	277.33	111.72	33.33	100.00
1	1	1	0	0	279.99	112.72	33.33	100.00
1	1	1	0	1	282.66	113.72	33.33	100.00
1	1	1	1	0	285.33	114.71	33.33	100.00
1	1	1	1	1	287.99	115.71	33.33	100.00

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Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
1	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
2	GND	PWR	Ground pin.
3	PCICLK3	OUT	PCI clock output.
4	PCICLK4	OUT	PCI clock output.
5	*SELPCIEX0_LCD#PCICLK5	I/O	Latched select input for LCDCLK/PCIEX output 0 = LCDCLK, 1 = PCIEX / 3.3V PCI clock output.
6	GND	PWR	Ground pin.
7	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
8	ITP_EN/PCICLK_F0	I/O	Free running PCI clock not affected by PCI_STOP#. ITP_EN: latched input to select pin functionality 1 = CPU_ITP pair 0 = SRC pair
9	*SELLCD_27#/PCICLK_F1	I/O	Free running PCI clock not affected by PCI_STOP#. SELLCD_27#: latched input to select pin functionality 1 = LCDCLK pair 0 = 27MHzSS/27MHzSS# pair
10	Vtt_PwrGd#/PD	IN	Vtt_PwrGd# is an active low input used to determine when latched inputs are ready to be sampled. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks, PLLs and the crystal oscillator are stopped.
11	VDD48	PWR	Power pin for the 48MHz output.3.3V
12	FSLA/USB_48MHz	I/O	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. / Fixed 48MHz USB clock output. 3.3V.
13	GND	PWR	Ground pin.
14	DOTT_96MHzL	OUT	True clock of low power differential pair for 96.00MHz DOT clock. No 50ohm to GND needed.
15	DOTC_96MHzL	OUT	Complement clock of low power differential pair for 96.00MHz DOT clock. No 50ohm resistor to GND needed.
16	FSLB/TEST_MODE	IN	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table.
17	27FIX/LCD_SSCGT/PCIeT_L0	OUT	27MHz Non-Spread Push-Pull output / True clock of low power LCDCLK output / True clock of low power PCIEXCLK differential pair/ selected by SELPCIEX0_LCD# and SELLCD_27#. No 50ohm resistor to GND needed for differential outputs.
18	27SS/LCD_SSCGC/PCIeC_L0	OUT	27MHz Spreading Push-Pull output / Complementary clock of LCDCLK_SS output / Complementary clock of PCIEXCLK differential pair/ selected by SELPCIEX0_LCD# and SELLCD_27#. No 50ohm resistor to GND needed for differential outputs.
19	PCIeT_L1	OUT	True clock of 0.8V differential push-pull PCI_Express pair (no 50ohm resistor to GND needed)
20	PCIeC_L1	OUT	Complement clock of 0.8V differential push-pull PCI_Express pair. (no 50ohm resistor to GND needed)
21	VDDPCIEX	PWR	Power supply for PCI Express clocks, nominal 3.3V
22	PCIeT_L2	OUT	True clock of 0.8V differential push-pull PCI_Express pair (no 50ohm resistor to GND needed)
23	PCIeC_L2	OUT	Complement clock of 0.8V differential push-pull PCI_Express pair. (no 50ohm resistor to GND needed)
24	PCIeT_L3	OUT	True clock of 0.8V differential push-pull PCI_Express pair (no 50ohm resistor to GND needed)
25	PCIeC_L3	OUT	Complement clock of 0.8V differential push-pull PCI_Express pair. (no 50ohm resistor to GND needed)
26	SATACLKT_L	OUT	True clock of 0.8V push-pull differential SATA pair. (no 50ohm resistor to GND needed)
27	SATACLKC_L	OUT	Complement clock of 0.8V push-pull differential SATA pair. (no 50ohm resistor to GND needed)
28	VDDPCIEX	PWR	Power supply for PCI Express clocks, nominal 3.3V

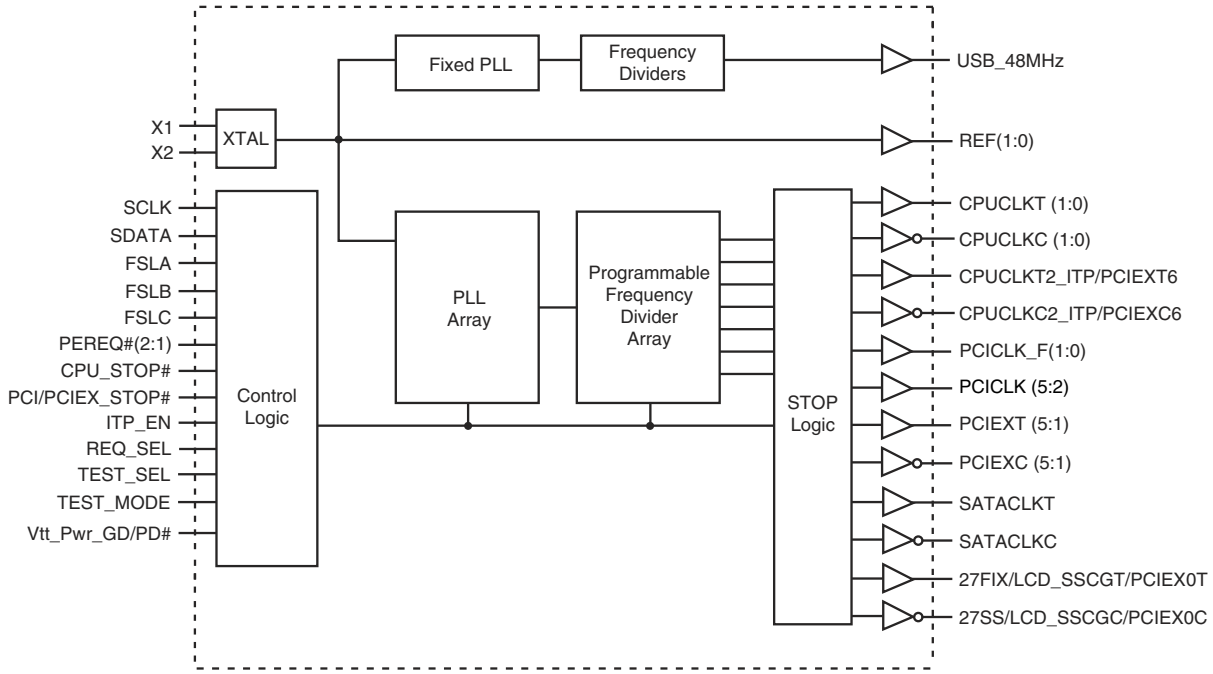
Pin Description (Continued)

PIN #	PIN NAME	TYPE	DESCRIPTION
29	GND	PWR	Ground pin.
30	PCIeC_L4	OUT	Complement clock of 0.8V differential push-pull PCI_Express pair. (no 50ohm resistor to GND needed)
31	PCIeT_L4	OUT	True clock of 0.8V differential push-pull PCI_Express pair (no 50ohm resistor to GND needed)
32	PEREQ2#/PCIeC_L5	I/O	Real-time input pin that controls PCIEXCLK outputs that are selected through the I2c. 1 = disabled, 0 = enabled. / Complement clock of differential low power PCI Express output. No 50ohm resistor to GND needed.
33	PEREQ1#/PCIeT_L5	I/O	Real-time input pin that controls PCIEXCLK outputs that are selected through the I2c. 1 = disabled, 0 = enabled. / True clock of differential low power PCI Express output. No 50ohm resistor to GND needed.
34	VDDPCIEX	PWR	Power supply for PCI Express clocks, nominal 3.3V
35	CPUITPC_L2/PCIeC_L6	OUT	Complement clock of differential pair CPU output. / Complement clock of differential PCIEX pair. These are 0.8V push pull outputs. No 50ohm resistor to GND needed.
36	CPUITPT_L2/PCIeT_L6	OUT	True clock of differential pair CPU output. / True clock of differential PCIEX pair. These are 0.8V push pull outputs. No 50ohm resistor to GND needed.
37	VDDA	PWR	3.3V power for the PLL core.
38	GNDA	PWR	Ground pin for the PLL core.
39	VDD	PWR	Power supply, nominal 3.3V
40	CPUC_L1	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs. No 50ohm resistor to GND needed.
41	CPUT_L1	OUT	True clock of differential pair 0.8V push-pull CPU outputs. No 50 ohm resistor to GND needed.
42	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
43	CPUC_L0	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs. No 50ohm resistor to GND needed.
44	CPUT_L0	OUT	True clock of differential pair 0.8V push-pull CPU outputs. No 50ohm resistor to GND needed.
45	GND	PWR	Ground pin.
46	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
47	SDATA	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
48	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
49	X2	OUT	Crystal output, Nominally 14.318MHz
50	X1	IN	Crystal input, Nominally 14.318MHz.
51	GND	PWR	Ground pin.
52	REF0	OUT	14.318 MHz reference clock.
53	REF1/FSLC/TEST_SEL	I/O	14.318 MHz reference clock./ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. /TEST_Sel: 3-level latched input to enable test mode. Refer to Test Clarification Table
54	CPU_STOP#	IN	Stops all CPU clocks, except those set to be free running clocks
55	PCI&PCIEX_STOP#	IN	Stops all PCICLKs at logic 0 level, when low. Free running PCICLKs are not effected by this input.
56	PCICLK2/REQ_SEL**	I/O	3.3V PCI clock output / Latch select input pin. 0 = PCIEXCLK, 1 = PEREQ#

General Description

ICS9LPR426A is a low power CK410M-compliant clock specification. This clock synthesizer provides a single chip solution for next generation P4 Intel processors and Intel chipsets. **ICS9LPR426A** is driven with a 14.318MHz crystal.

Block Diagram



M and N programming range

M	Minimum N	Maximum N
3	200	400
4	150	300
5	120	240
6	100	200
7	85	171
8	75	150
9	66	133
10	60	120
11	54	109
12	50	100
13	46	92

M	Minimum N	Maximum N
14	42	85
15	40	80
16	37	75
17	35	70
18	33	66
19	31	63
20	30	60
21	28	57
22	27	54
23	26	52
24	25	50

Yellow range is programming with more margin

Table 1: CPU PLL Spread Frequency Selection Table

FS4 (B0b4)	FS3 (B0b3)	FS_LC (B0b2)	FS_LB (B0b1)	FS_LA (B0b0)	CPU MHz	Spread %	
0	0	0	0	0	266.66	+/- 0.25 Center	CPU PLL Spread Depends on PCI PLL Spread
0	0	0	0	1	133.33	+/- 0.25 Center	
0	0	0	1	0	200.00	+/- 0.25 Center	
0	0	0	1	1	166.66	+/- 0.25 Center	
0	0	1	0	0	333.33	+/- 0.25 Center	
0	0	1	0	1	100.00	+/- 0.25 Center	
0	0	1	1	0	400.00	+/- 0.25 Center	
0	0	1	1	1	200.00	+/- 0.25 Center	
0	1	0	0	0	266.66	+/- 0.25 Center	
0	1	0	0	1	133.33	+/- 0.25 Center	
0	1	0	1	0	200.00	+/- 0.25 Center	
0	1	0	1	1	166.66	+/- 0.25 Center	
0	1	1	0	0	333.33	+/- 0.25 Center	
0	1	1	0	1	100.00	+/- 0.25 Center	
0	1	1	1	0	400.00	+/- 0.25 Center	
0	1	1	1	1	200.00	+/- 0.25 Center	
1	0	0	0	0	269.33	+/- 0.25 Center	
1	0	0	0	1	271.99	+/- 0.25 Center	
1	0	0	1	0	274.66	+/- 0.25 Center	
1	0	0	1	1	277.33	+/- 0.25 Center	
1	0	1	0	0	279.99	+/- 0.25 Center	
1	0	1	0	1	282.66	+/- 0.25 Center	
1	0	1	1	0	285.33	+/- 0.25 Center	
1	0	1	1	1	287.99	+/- 0.25 Center	
1	1	0	0	0	269.33	+/- 0.25 Center	
1	1	0	0	1	271.99	+/- 0.25 Center	
1	1	0	1	0	274.66	+/- 0.25 Center	
1	1	0	1	1	277.33	+/- 0.25 Center	
1	1	1	0	0	279.99	+/- 0.25 Center	
1	1	1	0	1	282.66	+/- 0.25 Center	
1	1	1	1	0	285.33	+/- 0.25 Center	
1	1	1	1	1	287.99	+/- 0.25 Center	

Table2: PCIEX PLL Spread and Frequency Selection Table

FS4 (B19b4)	FS3 (B19b3)	FS_LC (B19b2)	FS_LB (B19b1)	FS_LA (B19b0)	PCIEX MHz	Spread %	
0	0	0	0	0	99.75	+/- 0.25 Center	PCIEX PLL Spread Depends on PCI PLL Spread
0	0	0	0	1	99.75	+/- 0.25 Center	
0	0	0	1	0	99.75	+/- 0.25 Center	
0	0	0	1	1	99.75	+/- 0.25 Center	
0	0	1	0	0	99.75	+/- 0.25 Center	
0	0	1	0	1	99.75	+/- 0.25 Center	
0	0	1	1	0	99.75	+/- 0.25 Center	
0	0	1	1	1	99.75	+/- 0.25 Center	
0	1	0	0	0	99.75	+/- 0.25 Center	
0	1	0	0	1	99.75	+/- 0.25 Center	
0	1	0	1	0	99.75	+/- 0.25 Center	
0	1	0	1	1	99.75	+/- 0.25 Center	
0	1	1	0	0	99.75	+/- 0.25 Center	
0	1	1	0	1	99.75	+/- 0.25 Center	
0	1	1	1	0	99.75	+/- 0.25 Center	
0	1	1	1	1	99.75	+/- 0.25 Center	
1	0	0	0	0	100.00	+/- 0.25 Center	
1	0	0	0	1	101.75	+/- 0.25 Center	
1	0	0	1	0	102.74	+/- 0.25 Center	
1	0	0	1	1	103.74	+/- 0.25 Center	
1	0	1	0	0	104.74	+/- 0.25 Center	
1	0	1	0	1	105.74	+/- 0.25 Center	
1	0	1	1	0	106.73	+/- 0.25 Center	
1	0	1	1	1	107.73	+/- 0.25 Center	
1	1	0	0	0	108.73	+/- 0.25 Center	
1	1	0	0	1	109.73	+/- 0.25 Center	
1	1	0	1	0	110.72	+/- 0.25 Center	
1	1	0	1	1	111.72	+/- 0.25 Center	
1	1	1	0	0	112.72	+/- 0.25 Center	
1	1	1	0	1	113.72	+/- 0.25 Center	
1	1	1	1	0	114.71	+/- 0.25 Center	
1	1	1	1	1	115.71	+/- 0.25 Center	

Table3: SATA PLL Spread and Frequency Selection Table

B22b2	FS3 (B31b6)	Bit 2 (Hardwired Low = 0)	Bit 1 (Hardwired	Bit 0 (Hardwired	SATA MHz	Pin 17/18 MHz	Spread %
0	0	0	0	0	N/A*	27.00	0.5% Down
0	0	0	0	1	N/A*	27.00	0.5% Down
0	0	0	1	0	N/A*	27.00	0.5% Down
0	0	0	1	1	N/A*	27.00	0.5% Down
0	0	1	0	0	N/A*	27.00	0.5% Down
0	0	1	0	1	N/A*	27.00	0.5% Down
0	0	1	1	0	N/A*	27.00	0.5% Down
0	0	1	1	1	N/A*	27.00	0.5% Down
0	1	0	0	0	N/A*	27.00	+/- 0.3 Center
0	1	0	0	1	N/A*	27.00	+/- 0.3 Center
0	1	0	1	0	N/A*	27.00	+/- 0.3 Center
0	1	0	1	1	N/A*	27.00	+/- 0.3 Center
0	1	1	0	0	N/A*	27.00	+/- 0.3 Center
0	1	1	0	1	N/A*	27.00	+/- 0.3 Center
0	1	1	1	0	N/A*	27.00	+/- 0.3 Center
0	1	1	1	1	N/A*	27.00	+/- 0.3 Center
1	0	0	0	0	100.00	N/A*	No Spread
1	0	0	0	1	100.00	N/A*	No Spread
1	0	0	1	0	100.00	N/A*	No Spread
1	0	0	1	1	100.00	N/A*	No Spread
1	0	1	0	0	100.00	N/A*	No Spread
1	0	1	0	1	100.00	N/A*	No Spread
1	0	1	1	0	100.00	N/A*	No Spread
1	0	1	1	1	100.00	N/A*	No Spread
1	1	0	0	0	100.00	N/A*	0.5% Down
1	1	0	0	1	100.00	N/A*	0.5% Down
1	1	0	1	0	100.00	N/A*	0.5% Down
1	1	0	1	1	100.00	N/A*	0.5% Down
1	1	1	0	0	100.00	N/A*	0.5% Down
1	1	1	0	1	100.00	N/A*	0.5% Down
1	1	1	1	0	100.00	N/A*	0.5% Down
1	1	1	1	1	100.00	N/A*	0.5% Down

SELPCIEX_LCD# and SELLCD_27# definition:

SELPCIEX_LCD#	SELLCD_27#	Pin #17/18	SATA source
0	0	27MHzFixed/27MHz_SS pair	PCI PLL
0	1	LCD_SST/C pair	SATA PLL
1	0	PCIe0T/C	SATA PLL
1	1	PCIe0T/C	SATA PLL

Table4: PCI PLL Spread and Frequency Selection Table

Bit 4 (Hardwired Low = 0)	Bit 3 (Hardwired Low = 0)	Bit 2 (Hardwired Low = 0)	FS_LB (B22b1)	FS_LA (B22b0)	PCI	LCD/SATA	Spread
					MHz	MHz	%
0	0	0	0	0	33.33	100.00	+/- 0.25% Center
0	0	0	0	1	33.33	100.00	+/- 0.5% Center
0	0	0	1	0	33.33	100.00	+/- .3% Center
0	0	0	1	1	33.33	100.00	1% down
0	0	1	0	0	33.33	100.00	+/- 0.25% Center
0	0	1	0	1	33.33	100.00	+/- 0.5% Center
0	0	1	1	0	33.33	100.00	+/- .3% Center
0	0	1	1	1	33.33	100.00	1% down
0	1	0	0	0	33.33	100.00	+/- 0.25% Center
0	1	0	0	1	33.33	100.00	+/- 0.5% Center
0	1	0	1	0	33.33	100.00	+/- .3% Center
0	1	0	1	1	33.33	100.00	1% down
0	1	1	0	0	33.33	100.00	+/- 0.25% Center
0	1	1	0	1	33.33	100.00	+/- 0.5% Center
0	1	1	1	0	33.33	100.00	+/- .3% Center
0	1	1	1	1	33.33	100.00	1% down
1	0	0	0	0	33.33	100.00	+/- 0.25% Center
1	0	0	0	1	33.33	100.00	+/- 0.5% Center
1	0	0	1	0	33.33	100.00	+/- .3% Center
1	0	0	1	1	33.33	100.00	1% down
1	0	1	0	0	33.33	100.00	+/- 0.25% Center
1	0	1	0	1	33.33	100.00	+/- 0.5% Center
1	0	1	1	0	33.33	100.00	+/- .3% Center
1	0	1	1	1	33.33	100.00	1% down
1	1	0	0	0	33.33	100.00	+/- 0.25% Center
1	1	0	0	1	33.33	100.00	+/- 0.5% Center
1	1	0	1	0	33.33	100.00	+/- .3% Center
1	1	0	1	1	33.33	100.00	1% down
1	1	1	0	0	33.33	100.00	+/- 0.25% Center
1	1	1	0	1	33.33	100.00	+/- 0.5% Center
1	1	1	1	0	33.33	100.00	+/- .3% Center
1	1	1	1	1	33.33	100.00	1% down

General I²C serial interface information for the ICS9LPR426A

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
	O		
	O		O
	O		O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
		X Byte	Beginning Byte N
ACK			
			O
	O		O
	O		O
	O		
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

I2C Table: Frequency Select Register

Byte 0	Name	Control Function	Type	0	1	PWD
Bit 7	ROD	Reset on Demand	RW	Disable	Enable	0
Bit 6	SS_EN2	PCI PLL Spread Enable	RW	OFF	ON	1
Bit 5	Reserved	Reserved	RW	-	-	X
Bit 4	FS4	Freq Select Bit 4	RW	See Table 1: Frequency Selection Table		0
Bit 3	FS3	Freq Select Bit 3	RW			0
Bit 2	FSLC	Freq Select Bit 2	RW			Latch
Bit 1	FSLB	Freq Select Bit 1	RW			Latch
Bit 0	FSLA	Freq Select Bit 0	RW			Latch

I2C Table: Output Control Register

Byte 1	Name	Control Function	Type	0	1	PWD
Bit 7	Dot96Mhz	Output Control	RW	Disable	Enable	1
Bit 6	I2C RB	Select I2c readback from	RW	Shadow RAM	Active RAM	1
Bit 5	Reserved	Reserved	RW	-	-	X
Bit 4	PCIEX PLL MNEN	PCIEX PLL M/N Enable	RW	Disable	Enable	0
Bit 3	Reserved	Reserved	RW	-	-	X
Bit 2	REF0 STRENGTH	Strength Programming	RW	1X	2X	0
Bit 1	PCI/PCIEX_STOP#	Stop all PCI and PCIEX clocks	RW	Outputs Stopped	Outputs Active	1
Bit 0	CPU PLL MNEN	CPU PLL M/N Enable	RW	Disable	Enable	0

I2C Table: Output Control Register

Byte 2	Name	Control Function	Type	0	1	PWD
Bit 7	USB_48Mhz	Output Control	RW	Disable	Enable	1
Bit 6	CPUCLK2_ITP / PCIEXT/C6	Output Control	RW	Disable	Enable	1
Bit 5	SATACLKT/C	Output Control	RW	Disable	Enable	1
Bit 4	REF1	Output Control	RW	Disable	Enable	1
Bit 3	PCICLK5	Output Control	RW	Disable	Enable	1
Bit 2	PCICLK4	Output Control	RW	Disable	Enable	1
Bit 1	PCICLK3	Output Control	RW	Disable	Enable	1
Bit 0	PCICLK2	Output Control	RW	Disable	Enable	1

I2C Table: Output Control Register

Byte 3	Name	Control Function	Type	0	1	PWD
Bit 7	PCICLK1	Output Control	RW	Disable	Enable	1
Bit 6	PCICLK0	Output Control	RW	Disable	Enable	1
Bit 5	PCIEXT/C5	Output Control	RW	Disable	Enable	1
Bit 4	PCIEXT/C4	Output Control	RW	Disable	Enable	1
Bit 3	Reserved	Reserved	RW	-	-	X
Bit 2	Reserved	Reserved	RW	-	-	X
Bit 1	PCIEXT/C3	Output Control	RW	Disable	Enable	1
Bit 0	PCIEXT/C2	Output Control	RW	Disable	Enable	1

I2C Table: Output Control Register

Byte 4	Name	Control Function		0	1	PWD
Bit 7	PCIEXT/C1	Output Control	RW	Disable	Enable	1
Bit 6	REF0	Output Control	RW	Disable	Enable	1
Bit 5	CPUCLK1	Output Control	RW	Disable	Enable	1
Bit 4	CPUCLK0	Output Control	RW	Disable	Enable	1
Bit 3	SEL PCIEX_LCDCLK#	Selects PCIEX or LCD/27MHz on pins 17 and 18	R	LCDCLK	PCIEX0	latch
Bit 2	PCIEXT/C0	Output Control	RW	Disable	Enable	1
Bit 1	Reserved	Reserved	RW	-	-	X
Bit 0	Reserved	Reserved	RW	-	-	X

I2C Table: Output Control Register

Byte 5	Name	Control Function		0	1	PWD
Bit 7	PCIEXT/C4	Allow assertion of PCI_STOP# or setting of PCI_STOP control bit in I2C register to stop PCIEX clocks.	RW	Free-Running	Stoppable	0
Bit 6	Reserved		RW	-	-	X
Bit 5	Reserved		RW	-	-	X
Bit 4	SATACLK		RW	Free-Running	Stoppable	0
Bit 3	PCIEXT/C3		RW	Free-Running	Stoppable	0
Bit 2	PCIEXT/C2		RW	Free-Running	Stoppable	0
Bit 1	PCIEXT/C1		RW	Free-Running	Stoppable	0
Bit 0	PCIEXT/C0		RW	Free-Running	Stoppable	0

I2C Table: Amplitude Control Register

Byte 6	Name	Control Function	Type	0	1	PWD
Bit 7	Diff AMP	CPU Differential output Amplitude Control	RW	00 = 700mV	01 = 900mV	0
Bit 6	Diff AMP		RW	10 = 800mV	11 = 1000mV	0
Bit 5	Reserved	Reserved	RW	-	-	X
Bit 4	Reserved	Reserved	RW	-	-	X
Bit 3	Diff AMP	DOT96 Differential output Amplitude Control	RW	00 = 700mV	01 = 900mV	0
Bit 2	Diff AMP		RW	10 = 800mV	11 = 1000mV	0
Bit 1	Diff AMP	SATACLK Differential output Amplitude Control	RW	00 = 700mV	01 = 900mV	0
Bit 0	Diff AMP		RW	10 = 800mV	11 = 1000mV	0

I2C Table: Revision and Vendor ID Register

Byte 7	Name	Control Function	Type	0	1	PWD
Bit 7	RID3	Revision ID	R	-	-	0
Bit 6	RID2		R	-	-	0
Bit 5	RID1		R	-	-	0
Bit 4	RID0		R	-	-	0
Bit 3	VID3	VENDOR ID	R	-	-	0
Bit 2	VID2		R	-	-	0
Bit 1	VID1		R	001 = ICS	-	0
Bit 0	VID0		R	-	-	1

I2C Table: Byte Count Register

Byte 8	Name	Control Function	Type	0	1	PWD
Bit 7	BC7	Byte Count Programming b(7:0)	R	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes.		0
Bit 6	BC6		R			0
Bit 5	BC5		R			0
Bit 4	BC4		RW			0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			1
Bit 1	BC1		RW			1
Bit 0	BC0		RW			1

I2C Table: Watch Dog Timer Control Register

Byte 9	Name	Control Function	Type	0	1	PWD
Bit 7	HWD_EN	Watchdog Hard Alarm Enable	RW	Disable	Enable	0
Bit 6	SWD_EN	Watchdog Soft Alarm Enable	RW	Disable	Enable	0
Bit 5	WD Hard Status	WD Hard Alarm Status	R	Normal	Alarm	X
Bit 4	WD Soft Status	WD Soft Alarm Status	R	Normal	Alarm	X
Bit 3	WDTCtrl	Watch Dog Alarm Time base Control	RW	290ms Base	1160ms Base	0
Bit 2	HWD2	WD Hard Alarm Timer Bit 2	RW	These bits represent X*290ms (or 1.16S) the watchdog timer waits before it goes to alarm mode. Default is 7 X 290ms = 2s.		1
Bit 1	HWD1	WD Hard Alarm Timer Bit 1	RW			1
Bit 0	HWD0	WD Hard Alarm Timer Bit 0	RW			1

I2C Table: WD Safe Frequency Control Register

Byte 10	Name	Control Function	Type	0	1	PWD
Bit 7	SWD2	WD Soft Alarm Timer Bit 2	RW	These bits represent X*290ms (or 1.16S) the watchdog timer waits before it goes to alarm mode. Default is 7 X 290ms = 2s.		1
Bit 6	SWD1	WD Soft Alarm Timer Bit 1	RW			1
Bit 5	SWD0	WD Soft Alarm Timer Bit 0	RW			1
Bit 4	WD SF4	Watch Dog Safe Freq Programming bits	RW	Writing to these bit will configure the safe frequency as Byte10 bit (4:0).		0
Bit 3	WD SF3		RW			0
Bit 2	WD SF2		RW			0
Bit 1	WD SF1		RW			0
Bit 0	WD SF0		RW			0

I2C Table: CPU PLL Frequency Control Register

Byte 11	Name	Control Function	Type	0	1	PWD
Bit 7	N Div2	N Divider Prog bit 2	RW	The decimal representation of M and N Divider in Byte 11 and 12 will configure the CPU PLL VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 24 x Ndiv(10:0)/Mdiv(5:0)		X
Bit 6	N Div1	N Divider Prog bit 1	RW			X
Bit 5	M Div5	M Divider Programming bit (5:0)	RW			X
Bit 4	M Div4		RW			X
Bit 3	M Div3		RW			X
Bit 2	M Div2		RW			X
Bit 1	M Div1		RW			X
Bit 0	M Div0		RW			X

I2C Table: CPU PLL Frequency Control Register:

Byte 12	Name	Control Function	Type	0	1	PWD
Bit 7	N Div10	N Divider Programming Byte12 bit(7:0) and Byte11 bit(7:6)	RW	The decimal representation of M and N Divider in Byte 11 and 12 will configure the CPU PLL VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 24 x Ndiv(10:0)/Mdiv(5:0)		X
Bit 6	N Div9		RW			X
Bit 5	N Div8		RW			X
Bit 4	N Div7		RW			X
Bit 3	N Div6		RW			X
Bit 2	N Div5		RW			X
Bit 1	N Div4		RW			X
Bit 0	N Div3		RW			X

I2C Table: PCI PLL Spread Spectrum Control Register

Byte 13	Name	Control Function	Type	0	1	PWD
Bit 7	SSP7	Spread Spectrum Programming bit(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage of PCI PLL		X
Bit 6	SSP6		RW			X
Bit 5	SSP5		RW			X
Bit 4	SSP4		RW			X
Bit 3	SSP3		RW			X
Bit 2	SSP2		RW			X
Bit 1	SSP1		RW			X
Bit 0	SSP0		RW			X

I2C Table: PCI PLL Spread Spectrum Control Register

Byte 14	Name	Control Function	Type	0	1	PWD
Bit 7	SSP15	Spread Spectrum Programming bit(14:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage of PCI PLL		0
Bit 6	SSP14		RW			X
Bit 5	SSP13		RW			X
Bit 4	SSP12		RW			X
Bit 3	SSP11		RW			X
Bit 2	SSP10		RW			X
Bit 1	SSP9		RW			X
Bit 0	SSP8		RW			X

I2C Table: PCIEX PLL Frequency Control Register

Byte 15	Name	Control Function	Type	0	1	PWD
Bit 7	N Div2	N Divider Prog bit 2	RW	The decimal representation of M and N Divider in Byte 15 and 16 will configure the PCI PLL VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 24 x Ndiv(10:0)/Mdiv(5:0)		X
Bit 6	N Div1	N Divider Prog bit 1	RW			X
Bit 5	M Div5	M Divider Programming bit (5:0)	RW			X
Bit 4	M Div4		RW			X
Bit 3	M Div3		RW			X
Bit 2	M Div2		RW			X
Bit 1	M Div1		RW			X
Bit 0	M Div0		RW			X

I2C Table: PCIEX PLL Frequency Control Register:

Byte 16	Name	Control Function	Type	0	1	PWD
Bit 7	N Div10	N Divider Programming Byte16 bit(7:0) and Byte15 bit(7:6)	RW	The decimal representation of M and N Divider in Byte 15 and 16 will configure the PCI PLL VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 24 x Ndiv(10:0)/Mdiv(5:0)		X
Bit 6	N Div9		RW			X
Bit 5	N Div8		RW			X
Bit 4	N Div7		RW			X
Bit 3	N Div6		RW			X
Bit 2	N Div5		RW			X
Bit 1	N Div4		RW			X
Bit 0	N Div3		RW			X

Bytes 17,18 are reserved

I2C Table: PCIEX PLL Frequency Select Select Register

Byte 19	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved	Reserved	RW	-	-	0
Bit 6	Reserved	Reserved	RW	-	-	0
Bit 5	Reserved	Reserved	RW	-	-	0
Bit 4	FS4	Freq Select Bit 4	RW	See Table 2: PCIEX PLL Frequency Selection Table		0
Bit 3	FS3	Freq Select Bit 3	RW			0
Bit 2	FSLC	Freq Select Bit 2	RW			Latch
Bit 1	FSLB	Freq Select Bit 1	RW			Latch
Bit 0	FSLA	Freq Select Bit 0	RW			Latch

I2C Table: Output Control Register

Byte 20	Name	Control Function	Type	0	1	PWD
Bit 7	48Mhz	Strength Control	RW	1x	2x	0
Bit 6	CPU_1	Free running Control	RW	Free-Running	Stoppable	0
Bit 5	Load Control	IIC Load control	RW	Load	Do not Load	0
Bit 4	CPUCLK_2/ITP	Free-Running Controls	RW	Free-Running	Stoppable	0
Bit 3	Reserved	Reserved	RW	-	-	1
Bit 2	Reserved	Reserved	RW	-	-	1
Bit 1	CPUCLK_0	Free Running Controls	RW	Free-Running	Stoppable	0
Bit 0	RESET Sync	Reset Synchronization upon Reset (Byte 21)	RW	Disable	Enable	0

I2C Table: Synchronization Control Register

Byte 21	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved	Reserved	RW	-	-	1
Bit 6	Reserved	Reserved	RW	-	-	1
Bit 5	Reserved	Reserved	RW	-	-	1
Bit 4	Reserved	Reserved	RW	-	-	1
Bit 3	Reserved	Reserved	RW	-	-	1
Bit 2	Reserved	Reserved	RW	-	-	1
Bit 1	Reserved	Reserved	RW	-	-	1
Bit 0	Reserved	Reserved	RW	-	-	1

I2C Table: Output Control Register

Byte 22	Name	Control Function	Type	0	1	PWD
Bit 7	PCIEXT/C5	Free- Running Control	RW	Free-Running	Stoppable	0
Bit 6	PCIEXT/C6	Free- Running Control	RW	Free-Running	Stoppable	0
Bit 5	PCICLK_F1	Free- Running Control	RW	Free-Running	Stoppable	0
Bit 4	PCICLK_F0	Free- Running Control	RW	Free-Running	Stoppable	0
Bit 3	REF1	Strength Control	RW	1X	2X	0
Bit 2	Reserved	Reserved	RW	-	-	X
Bit 1	PCI PLL Freq. Select	Freq Select Bit 1	RW	See Table 4: PCI PLL Frequency Selection Table		0
Bit 0	PCI PLL Freq. Select	Freq Select Bit 0	RW			0

Bytes 23-27 are reserved

I2C Table: Programmable output divider Register

Byte 28	Name	Control Function	Type	0		1		PWD
Bit 7	Reserved	Reserved	RW	-		-		X
Bit 6	Reserved	Reserved	RW	-		-		X
Bit 5	Reserved	Reserved	RW	-		-		X
Bit 4	Reserved	Reserved	RW	-		-		X
Bit 3	CPUDiv3	CPU Divider Ratio Programming Bits for CPU PLL	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 2	CPUDiv2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 1	CPUDiv1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 0	CPUDiv0		RW	0011:/7	0111:/14	1011:/28	1111:/56	X

I2C Table: Programmable output divider Register

Byte 29	Name	Control Function	Type	0		1		PWD
Bit 7	Reserved	Reserved	RW	-		-		X
Bit 6	Reserved	Reserved	RW	-		-		X
Bit 5	Reserved	Reserved	RW	-		-		X
Bit 4	Reserved	Reserved	RW	-		-		X
Bit 3	PCIEXDiv3	PCIEX Divider Ratio Programming Bits for PCIEX PLL	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 2	PCIEXDiv2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 1	PCIEXDiv1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 0	PCIEXDiv0		RW	0011:/7	0111:/14	1011:/28	1111:/56	X

I2C Table: Programmable output divider Register

Byte 30	Name	Control Function	Type	0		1		PWD
Bit 7	Reserved	Reserved	RW	-		-		X
Bit 6	Reserved	Reserved	RW	-		-		X
Bit 5	Reserved	Reserved	RW	-		-		X
Bit 4	Reserved	Reserved	RW	-		-		X
Bit 3	PCIDiv3	PCI Divider Ratio Programming Bits	RW	0000:/N/A	0100:/N/A	1000:/N/A	1100:/N/A	X
Bit 2	PCIDiv2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 1	PCIDiv1		RW	0010:/9	0110:/18	1010:/36	1110:/72	X
Bit 0	PCIDiv0		RW	0011:/N/A	0111:/N/A	1011:/N/A	1111:/N/A	X

I2C Table: PEREQ# Control Register

Byte 31	Name	Control Function	Type	0	1	PWD
Bit 7	SELLCD_27#	Select LCD or 27MHz for pins 17/18	R	27MHz	LCDCLK	latch
Bit 6	Reserved	Reserved	RW	-	-	X
Bit 5	Reserved	Reserved	RW	-	-	X
Bit 4	Reserved	Reserved	RW	-	-	X
Bit 3	PEREQ2# Control	PCIEX6 is controlled	RW	Not Controlled	Controlled	0
Bit 2	PEREQ2# Control	PCIEX1 is controlled	RW	Not Controlled	Controlled	0
Bit 1	PEREQ1# Control	PCIEX4 is controlled	RW	Not Controlled	Controlled	0
Bit 0	PEREQ1# Control	PCIEX0 is controlled	RW	Not Controlled	Controlled	0

I2C Table: Skew programming Register

Byte 32	Name	Control Function	Type	0		1		PWD
Bit 7	CPUSkw3	CPUCLK0 Skew Control (ps)	RW	0000:0	0100:400	1000:800	1100:1200	0
Bit 6	CPUSkw2		RW	0001:100	0101:500	1001:900	1101:1300	0
Bit 5	CPUSkw1		RW	0010:200	0110:600	1010:1000	1110:1400	0
Bit 4	CPUSkw0		RW	0011:300	0111:700	1011:1100	1111:1500	0
Bit 3	CPUSkw3	CPUCLK1 Skew Control (ps)	RW	0000:0	0100:400	1000:800	1100:1200	0
Bit 2	CPUSkw2		RW	0001:100	0101:500	1001:900	1101:1300	0
Bit 1	CPUSkw1		RW	0010:200	0110:600	1010:1000	1110:1400	0
Bit 0	CPUSkw0		RW	0011:300	0111:700	1011:1100	1111:1500	0

Absolute Maximum Rating

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Core Supply Voltage	VDD_A	-			V_{DD} + 0.5V	V	1
3.3V Logic Input Supply Voltage	VDD_In	-	GND - 0.5		V_{DD} + 0.5V	V	1
Storage Temperature	Ts	-	-65		150	˚C	1
Ambient Operating Temp	Tambient	-	0		70	°C	1
Case Temperature	Tcase	-			115	°C	1
Input ESD protection HBM	ESD prot	-	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	3.3 V +/-5%	V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7		V_{DD} + 0.3	V	1
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%	V_{SS} - 0.3		0.35	V	1
Operating Supply Current	$I_{DD3.3OP}$	Full Active, C_L = Full load;		175	350	mA	1
Operating Current	$I_{DD3.3OP}$	all outputs driven		175	400	mA	1
Powerdown Current	$I_{DD3.3PD}$	all diff pairs driven		2	70	mA	1
Input Frequency	F_i	V_{DD} = 3.3 V		14.31818		MHz	2
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization	T_{STAB}	From VDD Power-Up or de-assertion of PD to 1st clock			1.8	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD		CPU output enable after PD de-assertion			300	us	1
Tfall_PD		PD fall time of			5	ns	1
Trise_PD		PD rise time of			5	ns	1
SMBus Voltage	V_{DD}		2.7		5.5	V	1
Low-level Output Voltage	V_{OL}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	I_{PULLUP}		4			mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Input frequency should be measured at the REF pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

AC Electrical Characteristics - (CPU, PCIEX, SATACLK, DOT96Mhz)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Rising Edge Slew Rate	t_{SLR}	Differential Measurement	2.5	8	V/ns	1,2
Falling Edge Slew Rate	t_{FLR}	Differential Measurement	2.5	8	V/ns	1,2
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement		20	%	1
Maximum Output Voltage	V_{HIGH}	Includes overshoot		1150	mV	1
Minimum Output Voltage	V_{LOW}	Includes undershoot	-300		mV	1
Differential Voltage Swing	V_{SWING}	Differential Measurement	300		mV	1
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	300	550	mV	1,3,4
Crossing Point Variation	$V_{XABSVAR}$	Single-ended Measurement		140	mV	1,3,5
Duty Cycle	D_{CYC}	Differential Measurement	45	55	%	1
CPU Jitter - Cycle to Cycle	$CPUJ_{C2C}$	Differential Measurement		85	ps	1
SRC Jitter - Cycle to Cycle	$SRCJ_{C2C}$	Differential Measurement		125	ps	1
DOT Jitter - Cycle to Cycle	$DOTJ_{C2C}$	Differential Measurement		250	ps	1
CPU[1:0] Skew	CPU_{SKEW10}	Differential Measurement		100	ps	1
CPU[2_ITP:0] Skew	CPU_{SKEW20}	Differential Measurement		150	ps	1
SRC Skew	SRC_{SKEW}	Differential Measurement		TBD	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

Electrical Characteristics - PCICLK/PCICLK_F

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	R_{DSP}	$V_O = V_{DD}$*(0.5)	12		55	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1		4	V/ns	1
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Group Skew	t_{skew}	V_T = 1.5 V			250	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[3] Spread Spectrum is off

Electrical Characteristics - 48MHz/USB48MHz/24_48MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Clock period	T_{period}	48.00MHz output nominal	20.8313		20.8354	ns	2
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12		55	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1		4	V/ns	1
Edge Rate	t_{slewr/f_USB}	USB48 Rising/Falling edge rate	1		2	V/ns	1
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns	1
Rise Time	t_{r_USB}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		2	ns	1
Fall Time	t_{f_USB}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Group Skew	t_{skew}	V_T = 1.5 V			250	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (Rs is used in USB48MHz test only)

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Clock period	T_{period}	14.318MHz output nominal	69.8270		69.8550	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V, V_{OH}@MAX = 3.135 V	-29		-23	mA	1
Output Low Current	I_{OL}	V_{OL} @MIN = 1.95 V, V_{OL} @MAX = 0.4 V	29		27	mA	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1		4	V/ns	1
Rise Time	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		2	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		2	ns	1
Skew	t_{sk1}	V_T = 1.5 V			500	ps	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			1000	ps	1

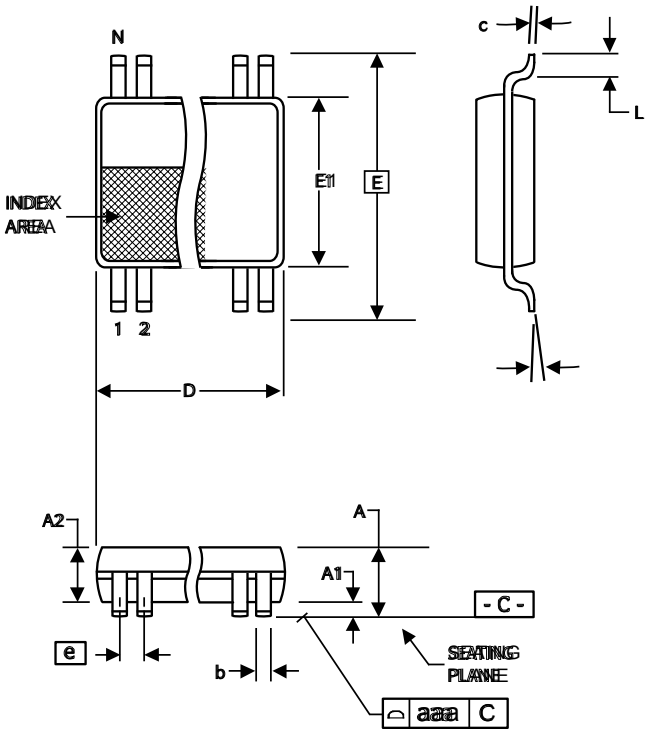
*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (Rs is used in USB48MHz test only)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

Test Clarification Table

Comments	HW		
	FSLC/ TEST_SEL HW PIN	FSLB/ TEST_MODE HW PIN	OUTPUT
	<2.0V	X	NORMAL
Power-up w/ TEST_SEL = 1 to enter test mode Cycle power to disable test mode FSLC./TEST_SEL -->3-level latched input If power-up w/ V>2.0V then use TEST_SEL If power-up w/ V<2.0V then use FSLC FSLB/TEST_MODE -->low Vth input TEST_MODE is a real time input	>2.0V	0	HI-Z
	>2.0V	1	REF/N



56-Lead 6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

ICS9LPR426AGLF-T

Example:

ICS XXXX A G LF- T

- **Designation for tape and reel packaging**
- **Lead Free, RoHS Compliant (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator**
- **Device Type**
- **Prefix**
  ICS = Standard Device

1346—10/23/07

Revision History

Rev.	Issue Date	Description	Page #
0.1	05/09/07	Initial Release	-
0.2	06/04/07	Updated SMBUS	Various
0.3	06/22/07	1. Updated Output Features. 2. Updated Block Diagram	1, 4
0.4	08/21/07	Added Test Clarification Table.	19
0.5	09/14/07	Updated Electrical Characteristics.	16
0.6	10/23/07	Added Programming Range Table	4