

# LR38617

Timing Generator IC for  
3 300 k/3 370 k-pixel CCDs

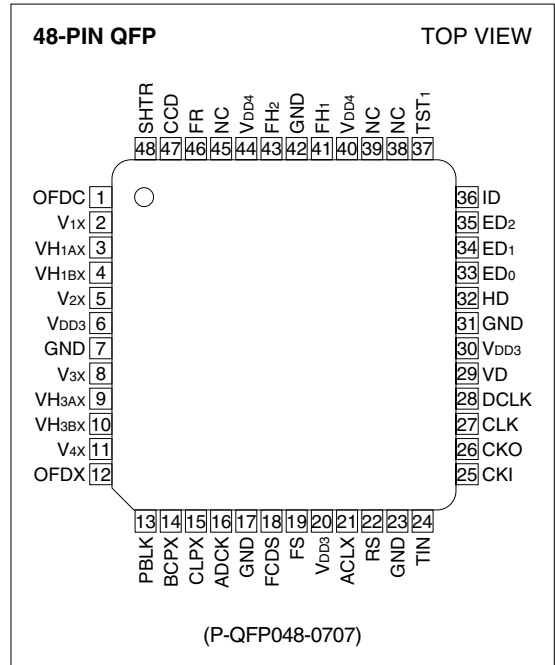
## DESCRIPTION

The LR38617 is a CMOS timing generator IC which generates timing pulses for driving 3 300 k/ 3 370 k-pixel CCD area sensors and processing pulses.

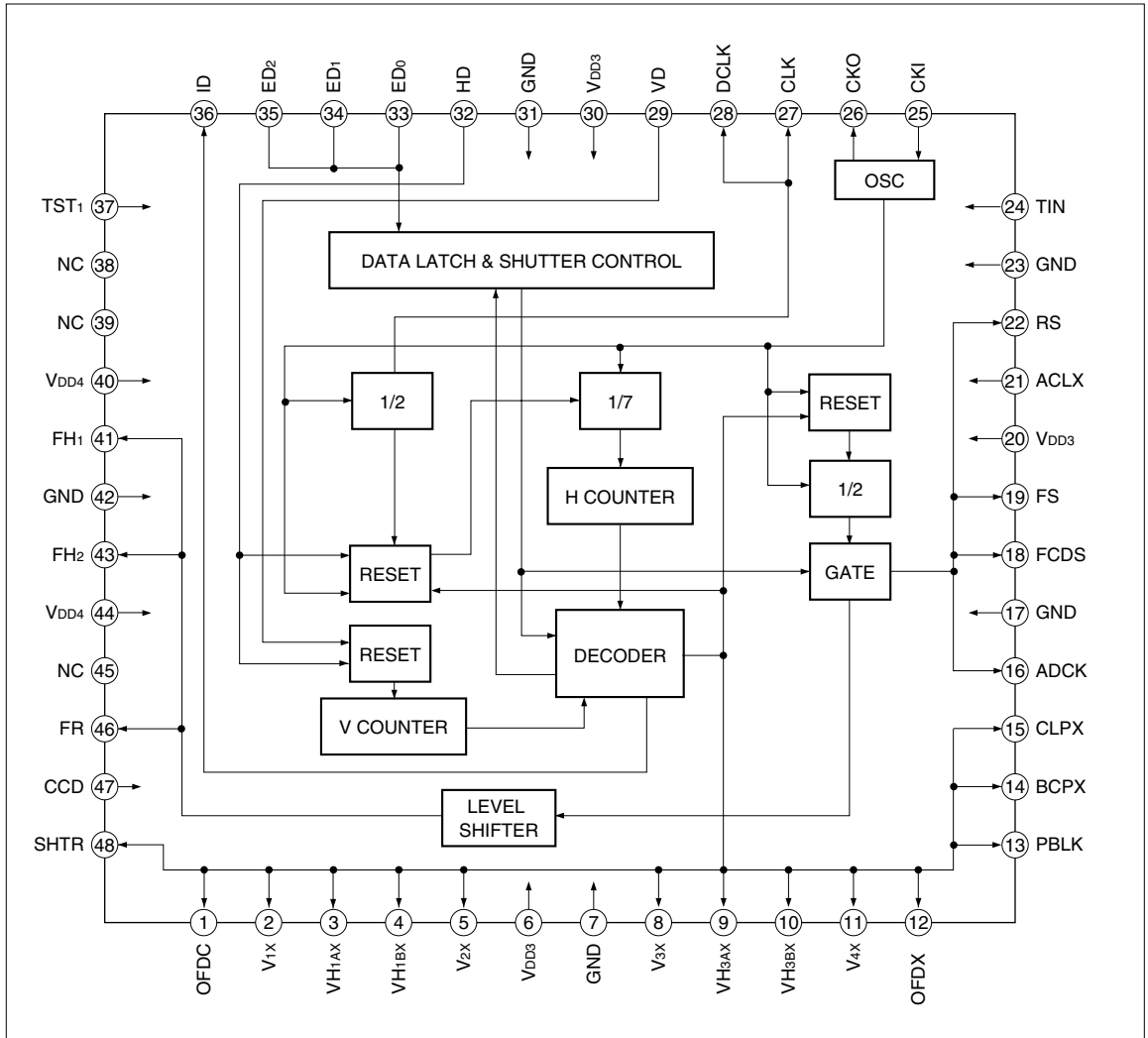
## FEATURES

- Designed for 1/1.8-type 3 300 k/3 370 k-pixel CCD area sensors
- Frequency of driving horizontal CCD : 18.00 MHz
- In monitoring mode, it can be obtained 30 fields/s.
- External shutter control function with serial data input is possible
- +3.3 V and +4.5 V power supplies
- Package :  
48-pin QFP (P-QFP048-0707) 0.5 mm pin-pitch










## PIN CONNECTIONS





















**BLOCK DIAGRAM**



## PIN DESCRIPTION

PIN NO.	SYMBOL	IO SYMBOL	POLARITY	PIN NAME	DESCRIPTION
1	OFDC	O3		Control pulse output for OFD voltage	A pulse to control OFD voltage.
2	V1X	O3		Vertical transfer pulse output 1	A vertical transfer pulse for the CCD. Connect to V1X pin of vertical driver IC.
3	VH1AX	O3		Readout pulse output 1A	A pulse that transfers the charge of the photo-diode to the vertical shift register. Connect to VH1AX pin of vertical driver IC.
4	VH1BX	O3		Readout pulse output 1B	A pulse that transfers the charge of the photo-diode to the vertical shift register. Connect to VH1BX pin of vertical driver IC.
5	V2X	O3		Vertical transfer pulse output 2	A vertical transfer pulse for the CCD. Connect to V2X pin of vertical driver IC.
6	VDD3	–	–	Power supply	Supply of +3.3 V power.
7	GND	–	–	Ground	A grounding pin.
8	V3X	O3		Vertical transfer pulse output 3	A vertical transfer pulse for the CCD. Connect to V3X pin of vertical driver IC.
9	VH3AX	O3		Readout pulse output 3A	A pulse that transfers the charge of the photo-diode to the vertical shift register. Connect to VH3AX pin of vertical driver IC.
10	VH3BX	O3		Readout pulse output 3B	A pulse that transfers the charge of the photo-diode to the vertical shift register. Connect to VH3BX pin of vertical driver IC.
11	V4X	O3		Vertical transfer pulse output 4	A vertical transfer pulse for the CCD. Connect to V4X pin of vertical driver IC.
12	OFDX	O3		OFD pulse output	A pulse that sweeps the charge of the photo-diode for the electronic shutter. Connect to OFD pin of the CCD through the vertical driver IC and DC offset circuit. Held at H level in normal mode.
13	PBLK	O3		Pre-blanking pulse output	A pulse for pre-blanking. This pulse is controlled by serial data BLKCNT. BLKCNT = H; This pulse stays low during the absence of effective pixels within the vertical blanking or during the sweepout signal. BLKCNT = L; Continuous pulse The output phase of PBLK is selected by serial data.

PIN NO.	SYMBOL	IO SYMBOL	POLARITY	PIN NAME	DESCRIPTION
14	BCPX	O3		Optical black clamp pulse output	A pulse to clamp the optical black signal. This pulse is controlled by serial data BCPCNT. BCPCNT = H; This pulse stays high during the absence of effective pixels within the vertical blanking or during the sweepout signal. BCPCNT = L; This pulse stays high during sweepout signal.
15	CLPX	O3		Clamp pulse output	A pulse to clamp the dummy outputs of the CCD signal. This pulse stays high during the sweepout period.
16	ADCK	O6MA3		AD clock output	An output pin for AD converter. The output phase of ADCK is selected by serial data in 90° steps.
17	GND	–	–	Ground	A grounding pin.
18	FCDS	O6MA3	 	CDS pulse output 1	A pulse to clamp the feed-through level for the CCD. The output phase and output polarity of FCDS are selected by serial data.
19	FS	O6MA3	 	CDS pulse output 2	A pulse to sample-hold the signal for the CCD. The output phase and output polarity of FS are selected by serial data.
20	VDD3	–	–	Power supply	Supply of +3.3 V power.
21	ACLX	ICU3	–	All clear input	An input pin for resetting all internal circuits at power-on. Connect to VDD3 through the diode and GND through the capacitor.
22	RS	O6MA3	 	S/H pulse output	A pulse to sample-hold the signal for the CDS circuit. The output phase and output polarity of RS are selected by serial data.
23	GND	–	–	Ground	A grounding pin.
24	TIN	IC3	–	Test input	A test pin. Set to L level in normal mode.
25	CKI	OSCI3	–	Clock input	An input pin for reference clock oscillation. The frequency is 36.00 MHz.
26	CKO	OSCO3	–	Clock output	An output pin for reference clock oscillation. The output is the inverse of CKI (pin 25).
27	CLK	O6MA3		Clock output	An output pin to generate HD and VD pulses. The frequency is 18.00 MHz.
28	DCLK	O6MA3		Clock output	An output pin for DSP IC. The frequency is 18.00 MHz. The output phase of DCLK is selected by serial data in 90° steps.
29	VD	IC3		Vertical reference pulse input	An input pin for reference of vertical pulse. Connect to VD pin of DSP IC.
30	VDD3	–	–	Power supply	Supply of +3.3 V power.
31	GND	–	–	Ground	A grounding pin.

PIN NO.	SYMBOL	IO SYMBOL	POLARITY	PIN NAME	DESCRIPTION
32	HD	IC3		Horizontal drive pulse input	An input pin for reference of horizontal pulse. Connect to HD pin of DSP IC.
33	ED <sub>0</sub>	ICSU3	–	Strobe pulse input	An input pin for the strobe pulse, to control the functions of LR38617. For details, see "Serial Data Control".
34	ED <sub>1</sub>	ICSU3	–	Shift register clock input	An input pin for the clock of the shift register, to control the functions of LR38617. For details, see "Serial Data Control".
35	ED <sub>2</sub>	ICSU3	–	Shift register data input	An input pin for the data of the shift register, to control the functions of LR38617. For details, see "Serial Data Control".
36	ID	O3		Line index pulse output	The pulse is used in the color separator. The signal switches between high and low at every line.
37	TST <sub>1</sub>	ICD4	–	Test pin 1	A test pin. Set open or to L level in normal mode.
38	NC	–	–	No connection	No connection.
39	NC	–	–	No connection	No connection.
40	V <sub>DD4</sub>	–	–	Power supply	Supply of +4.5 V power.
41	FH <sub>1</sub>	O6MA43		Horizontal transfer pulse output 1	A horizontal transfer pulse for the CCD. Connect to $\phi_{H1}$ pin of the CCD.
42	GND	–	–	Ground	A grounding pin.
43	FH <sub>2</sub>	O6MA43		Horizontal transfer pulse output 2	A horizontal transfer pulse for the CCD. Connect to $\phi_{H2}$ pin of the CCD.
44	V <sub>DD4</sub>	–	–	Power supply	Supply of +4.5 V power.
45	NC	–	–	No connection	No connection.
46	FR	O6MA43		Reset pulse output	A pulse to reset the charge of output circuit. The output phase of FR is selected by serial data.
47	CCD	ICU4	–	CCD selection input	An input pin to select CCD. L level : Aspect ratio 4 : 3 CCD H level or open : Aspect ratio 3 : 2 CCD
48	SHTR	O3		Trigger output	A trigger pulse for effective signal period.

IC3 : Input pin (CMOS level)

ICU3 : Input pin (CMOS level with pull-up resistor)

ICSU3 : Input pin (CMOS schmitt-trigger level with pull-up resistor)

ICU4 : Input pin (CMOS level with pull-up resistor)

ICD4 : Input pin (CMOS level with pull-down resistor)

O3 : Output pin (output high level is V<sub>DD3</sub>.)

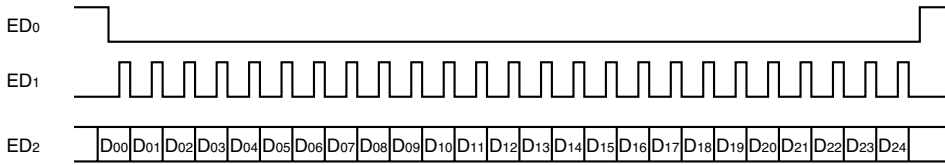
O6MA3 : Output pin (output high level is V<sub>DD3</sub>.)

O6MA43 : Output pin (output high level is V<sub>DD4</sub>.)

OSCI3 : Input pin for oscillation

OSCO3 : Output pin for oscillation

**Serial Data Control**  
**SERIAL DATA INPUT TIMING**

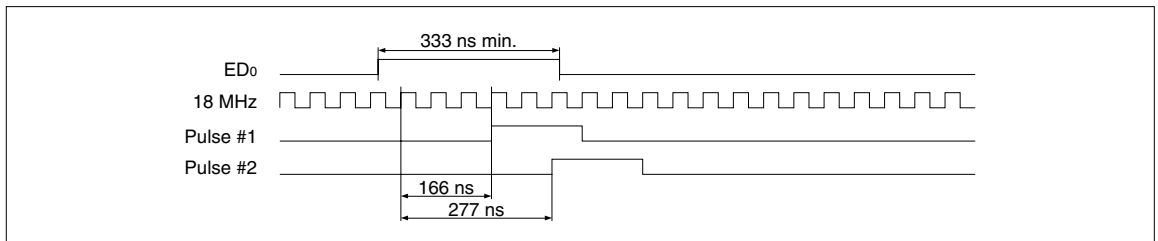


ED2 is shifted by the rising edge of ED1, and is latched by the pulse #1 which is generated after 167 to 222 ns delay from the rising edge of ED0. (See Fig. 2.)

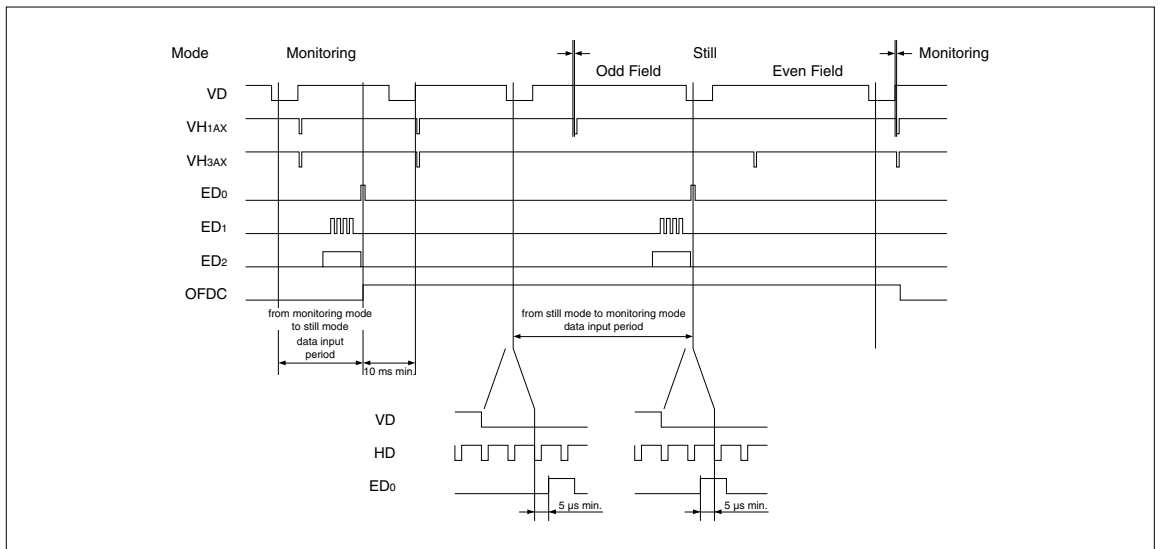
The latched serial data are divided into two types by the data of D00, and are relatched by the pulse #2 which is generated after 277 to 332 ns delay from the rising edge of ED0. (See Fig. 1.)

INMD is effective at the start of #3 horizontal line, and shutter control data are effective at the start of #6 or #234 horizontal line at CCD = L, or #12 HD horizontal line at CCD = H, and other data are effective at pulse #2.

ED0 should be at low level during data inputs of ED1 and ED2, or while ACLX is at low level.



**Fig. 1 Data Latch Timing**



**Fig. 2 Input Pulse Timing of ED0, ED1 and ED2**

## SERIAL DATA INPUTS

D00 = L

DATA	NAME	FUNCTION	DATA = L	DATA = H	AT ACLX = L
D01-D09	SDV0-SDV8	Integration time control in field period step by horizontal period.	-		All L
D10-D15	SDH0-SDH5	Integration time control in horizontal period step by 112 CLK clock period.	-		All L
D16	SDF0	Integration time control by field period.	-		All L
D17	SDF1				
D18	SDF2				
D19	SMD	Electronic shutter mode control	-		L
D20	PWSA	Power save control	Normal	Power save	L
D21	INMD	Integration mode control	Monitoring	Still	L
D22	Dummy	Dummy	Fix to L level		L
D23	BCPCNT	BCPX control	Discontinuous	Continuous	L
D24	VHCNT	VH1AX to VH3BX control	Output	Held at H level	L

D00 = H

DATA	NAME	FUNCTION	DATA = L	DATA = H	AT ACLX = L
D01	ML1	Phase control	-		All L
D02	ML2				
D03	MR1		-		All L
D04	MR2				
D05	MR3				
D06	MC1		-		All L
D07	MC2				
D08	MC3		-		All L
D09	MS1				
D10	MS2				
D11	MS3		-		All L
D12	MF1				
D13	MF2				
D14	MF3				
D15	MA1		-		All L
D16	MA2				
D17	MD1		-		All L
D18	MD2				
D19	MD3				
D20	MP1		-		All L
D21	MP2				
D22	PLCH	Polarity control of FCDS, FS and RS pulses	Negative	Positive	L
D23	BLKCNT	PBLK control	Continuous	Discontinuous	L
D24	Dummy	Dummy	Fix to L level		L

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	VDD3, VDD4	-0.3 to +6.0	V
Input voltage	VI3	-0.3 to VDD3 + 0.3	V
	VI4	-0.3 to VDD4 + 0.3	V
Output voltage	VO3	-0.3 to VDD3 + 0.3	V
	VO4	-0.3 to VDD4 + 0.3	V
Operating temperature	TOPR	-20 to +70	°C
Storage temperature	TSTG	-55 to +150	°C

## ELECTRICAL CHARACTERISTICS

### DC Characteristics

(VDD3 = 3.0 V to VDD4, VDD4 = 4.2 to 5.5 V, TOPR = -20 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	VIL3-1				0.2VDD3	V	1, 2
Input "High" voltage	VIH3-1		0.8VDD3			V	
Input "Low" voltage	VIL3-2	Schmitt-buffer	0.2VDD3			V	3
Input "High" voltage	VIH3-2				0.75VDD3	V	
Hysteresis voltage	VT+ - VT-			0.08VDD3			
Input "Low" voltage	VIL4				0.2VDD4	V	4
Input "High" voltage	VIH4		0.8VDD4			V	
Input "Low" current	IIL3-1	VI = 0 V			1.0	μA	1
Input "High" current	IIH3-1	VI = VDD3			1.0	μA	
Input "Low" current	IIL3-2	VI = 0 V	2.0		60	μA	2, 3
Input "High" current	IIH3-2	VI = VDD3			2.0	μA	
Input "Low" current	IIL4-1	VI = 0 V			2.0	μA	4
Input "High" current	IIH4-1	VI = VDD4	4.0		60	μA	
Input "Low" current	IIL4-2	VI = 0 V	4.0		60	μA	5
Input "High" current	IIH4-2	VI = VDD4			2.0	μA	
Output "Low" voltage	VOL3-1	IOL = 2 mA			0.4	V	6
Output "High" voltage	VOH3-1	IOH = -1 mA	VDD3 - 0.5			V	
Output "Low" voltage	VOL3-2	IOL = 3 mA			0.4	V	7
Output "High" voltage	VOH3-2	IOH = -3 mA	VDD3 - 0.5			V	
Output "Low" voltage	VOL4	IOL = 10 mA			0.4	V	8
Output "High" voltage	VOH4	IOH = -10 mA	VDD4 - 0.5			V	

### NOTES :

1. Applied to inputs (IC3, OSCI3).
2. Applied to input (ICU3).
3. Applied to input (ICSU3).
4. Applied to input (ICD4).
5. Applied to input (ICU4).
6. Applied to output (O3).
7. Applied to outputs (OSCO3, O6MA3). (Output (OSCO3) measures on condition that input (OSCI3) level is 0 V or VDD3.)
8. Applied to output (O6MA43).

PACKAGE OUTLINES

48 QFP (P-QFP048-0707)

(Unit : mm)

