# 2.5V LVDS 1:6 CLOCK BUFFER TERABUFFER™ II

IDT5T9306

## FEATURES:

- **Guaranteed Low Skew < 25ps (max)**
- **Very low duty cycle distortion < 125ps (max)**
- **High speed propagation delay < 1.75ns (max)**
- **Additive phase jitter, RMS 0.159ps (typical) @ 125MHz**
- **Up to 1GHz operation**
- **Selectable inputs**
- **Hot insertable and over-voltage tolerant inputs**
- **3.3V / 2.5V LVTTL, HSTL, eHSTL, LVEPECL (2.5V), LVPECL (3.3V), CML, or LVDS input interface**
- **Selectable differential inputs to six LVDS outputs**
- **Power-down mode**
- **2.5V $V_{DD}$**
- **Available in VFQFPN package**

## APPLICATIONS:

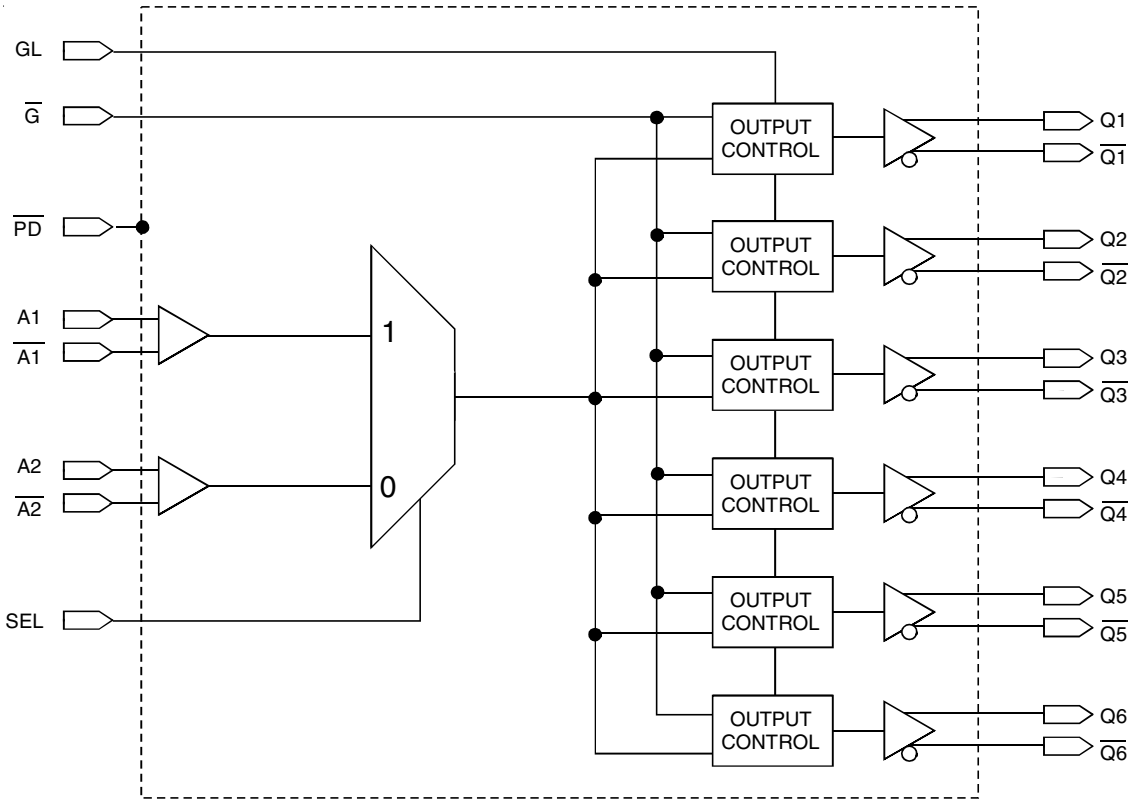
- **Clock distribution**

## DESCRIPTION:

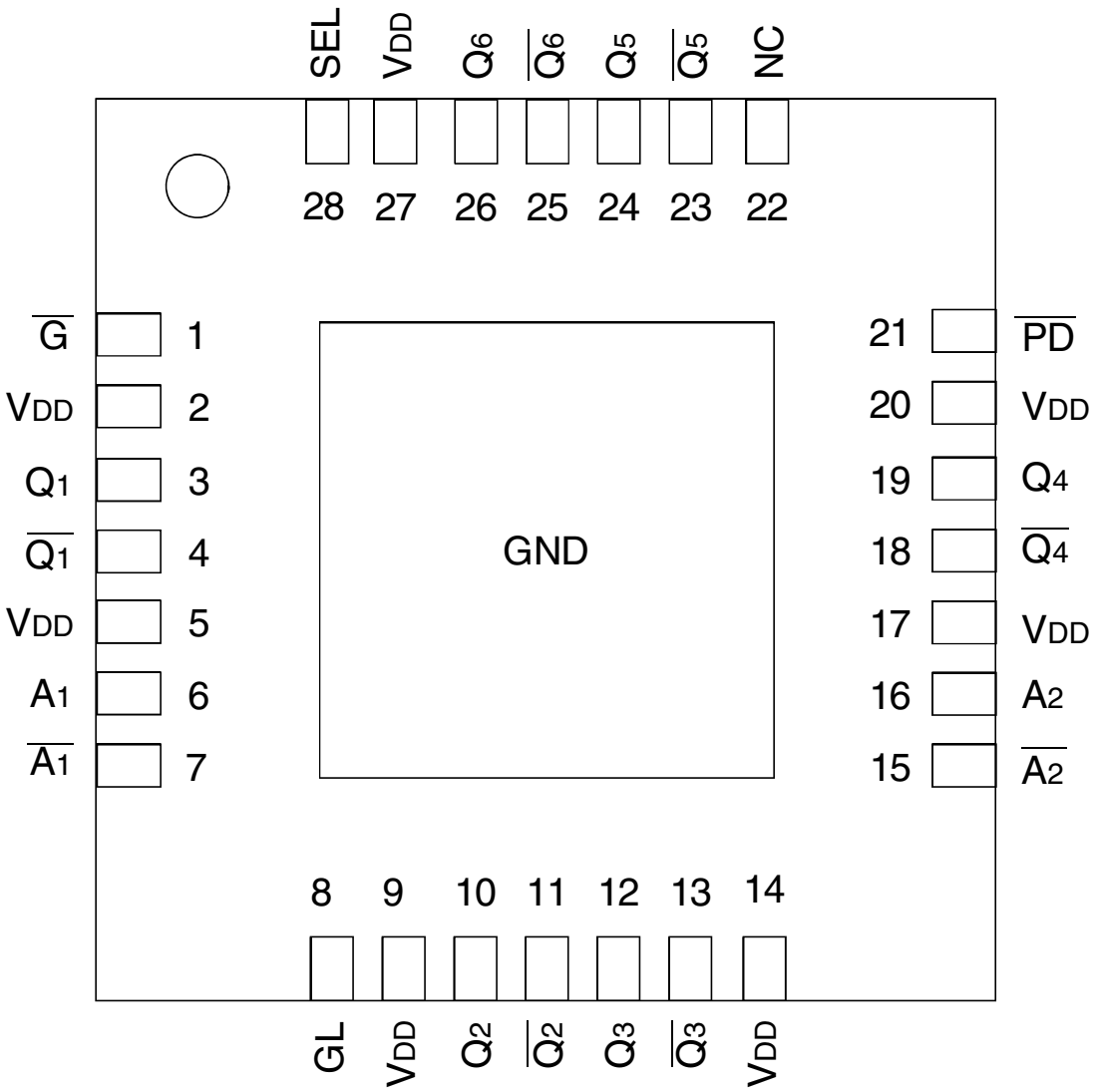
The IDT5T9306 2.5V differential clock buffer is a user-selectable differential input to six LVDS outputs. The fanout from a differential input to six LVDS outputs reduces loading on the preceding driver and provides an efficient clock distribution network. The IDT5T9306 can act as a translator from a differential HSTL, eHSTL, LVEPECL (2.5V), LVPECL (3.3V), CML, or LVDS input to LVDS outputs. A single-ended 3.3V / 2.5V LVTTL input can also be used to translate to LVDS outputs. The redundant input capability allows for an asynchronous change-over from a primary clock source to a secondary clock source. Selectable reference inputs are controlled by SEL.

The IDT5T9306 outputs can be asynchronously enabled/disabled. When disabled, the outputs will drive to the value selected by the GL pin. Multiple power and grounds reduce noise.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION




**VFQFPN**
**TOP VIEW**

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Description | Max | Unit |
|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | –0.5 to +3.6 | V |
| $V_I$ | Input Voltage | –0.5 to +3.6 | V |
| $V_O$ | Output Voltage(2) | –0.5 to $V_{DD}$ +0.5 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | ° C |
| $T_J$ | Junction Temperature | 150 | ° C |

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Not to exceed 3.6V.

## CAPACITANCE(1) ($T_A$ = +25°C, F = 1.0MHz)

| Symbol | Parameter | Min | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | — | — | 3 | pF |

**NOTE:**
1. This parameter is measured at characterization but not tested

## RECOMMENDED OPERATING RANGE

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_A$ | Ambient Operating Temperature | –40 | +25 | +85 | ° C |
| $V_{DD}$ | Internal Power Supply Voltage | 2.3 | 2.5 | 2.7 | V |

## PIN DESCRIPTION

| Symbol | I/O | Type | Description |
|---|---|---|---|
| $A_{[1:2]}$ | I | Adjustable(1,4) | Clock input. $A_{[1:2]}$ is the "true" side of the differential clock input. |
| $\overline{A}_{[1:2]}$ | I | Adjustable(1,4) | Complementary clock inputs. $\overline{A}_{[1:2]}$ is the complementary side of $A_{[1:2]}$. For LVTTL single-ended operation, $\overline{A}_{[1:2]}$ should be set to the desired toggle voltage for $A_{[1:2]}$:<br>3.3V LVTTL $V_{REF}$ = 1650mV<br>2.5V LVTTL $V_{REF}$ = 1250mV |
| $\overline{G}$ | I | LVTTL | Gate control for differential outputs $Q_1$ and $\overline{Q}_1$ through $Q_6$ and $\overline{Q}_6$. When $\overline{G}$ is LOW, the differential outputs are active. When $\overline{G}$ is HIGH, the differential outputs are asynchronously driven to the level designated by GL(2). |
| GL | I | LVTTL | Specifies output disable level. If HIGH, "true" outputs disable HIGH and "complementary" outputs disable LOW. If LOW, "true" outputs disable LOW and "complementary" outputs disable HIGH. |
| Qn | O | LVDS | Clock outputs |
| $\overline{Q}$n | O | LVDS | Complementary clock outputs |
| SEL | I | LVTTL | Reference clock select. When LOW, selects $A_2$ and $\overline{A}_2$. When HIGH, selects $A_1$ and $\overline{A}_1$. |
| $\overline{PD}$ | I | LVTTL | Power-down control. Shuts off entire chip. If LOW, the device goes into low power mode. Inputs and outputs are disabled. Both "true" and "complementary" outputs will pull to $V_{DD}$. Set HIGH for normal operation.(3) |
| $V_{DD}$ | | PWR | Power supply for the device core and inputs |
| GND | | PWR | Power supply return for all power |
| NC | | | No connect; recommended to connect to GND |

**NOTES:**
1. Inputs are capable of translating the following interface standards:
   Single-ended 3.3V and 2.5V LVTTL levels
   Differential HSTL and eHSTL levels
   Differential LVEPECL (2.5V) and LVPECL (3.3V) levels
   Differential LVDS levels
   Differential CML levels
2. Because the gate controls are asynchronous, runt pulses are possible. It is the user's responsibility to either time the gate control signals to minimize the possibility of runt pulses or be able to tolerate them in down stream circuitry.
3. It is recommended that the outputs be disabled before entering power-down mode. It is also recommended that the outputs remain disabled until the device completes power-up after asserting $\overline{PD}$.
4. The user must take precautions with any differential input interface standard being used in order to prevent instability when there is no input signal.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR LVTTL(1)

| Symbol | Parameter | Test Conditions | Min. | Typ.(2) | Max | Unit |
|---|---|---|---|---|---|---|
| **Input Characteristics** | | | | | | |
| $I_{IH}$ | Input HIGH Current | $V_{DD}$ = 2.7V | — | — | ±5 | µA |
| $I_{IL}$ | Input LOW Current | $V_{DD}$ = 2.7V | — | — | ±5 | |
| $V_{IK}$ | Clamp Diode Voltage | $V_{DD}$ = 2.3V, $I_{IN}$ = -18mA | — | - 0.7 | - 1.2 | V |
| $V_{IN}$ | DC Input Voltage | | - 0.3 | — | +3.6 | V |
| $V_{IH}$ | DC Input HIGH | | 1.7 | — | — | V |
| $V_{IL}$ | DC Input LOW | | — | — | 0.7 | V |
| $V_{THI}$ | DC Input Threshold Crossing Voltage | | — | $V_{DD}$ /2 | — | V |
| $V_{REF}$ | Single-Ended Reference Voltage(3) | 3.3V LVTTL | — | 1.65 | — | V |
| | | 2.5V LVTTL | — | 1.25 | — | |

**NOTES:**

1. See RECOMMENDED OPERATING RANGE table.
2. Typical values are at $V_{DD}$ = 2.5V, +25°C ambient.
3. For $A_{[1:2]}$ single-ended operation, $A_{[1:2]}$ is tied to a DC reference voltage.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR DIFFERENTIAL INPUTS(1)

| Symbol | Parameter | Test Conditions | Min. | Typ.(2) | Max | Unit |
|---|---|---|---|---|---|---|
| **Input Characteristics** | | | | | | |
| $I_{IH}$ | Input HIGH Current | $V_{DD}$ = 2.7V | — | — | ±5 | µA |
| $I_{IL}$ | Input LOW Current | $V_{DD}$ = 2.7V | — | — | ±5 | |
| $V_{IK}$ | Clamp Diode Voltage | $V_{DD}$ = 2.3V, $I_{IN}$ = -18mA | — | - 0.7 | - 1.2 | V |
| $V_{IN}$ | DC Input Voltage | | - 0.3 | — | +3.6 | V |
| $V_{DIF}$ | DC Differential Voltage(3) | | 0.1 | — | — | V |
| $V_{CM}$ | DC Common Mode Input Voltage(4) | | 0.05 | — | $V_{DD}$ | V |

**NOTES:**

1. See RECOMMENDED OPERATING RANGE table.
2. Typical values are at $V_{DD}$ = 2.5V, +25°C ambient.
3. $V_{DIF}$ specifies the minimum input differential voltage ($V_{TR}$ - $V_{CP}$) required for switching where $V_{TR}$ is the "true" input level and $V_{CP}$ is the "complement" input level. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
4. $V_{CM}$ specifies the maximum allowable range of ($V_{TR}$ + $V_{CP}$) /2.

## DC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING RANGE FOR LVDS(1)

| Symbol | Parameter | Test Conditions | Min. | Typ.(2) | Max | Unit |
|---|---|---|---|---|---|---|
| **Output Characteristics** | | | | | | |
| $V_{OT}(+)$ | Differential Output Voltage for the True Binary State | | 247 | — | 454 | mV |
| $V_{OT}(-)$ | Differential Output Voltage for the False Binary State | | 247 | — | 454 | mV |
| $\Delta V_{OT}$ | Change in $V_{OT}$ Between Complementary Output States | | — | — | 50 | mV |
| $V_{OS}$ | Output Common Mode Voltage (Offset Voltage) | | 1.125 | 1.2 | 1.375 | V |
| $\Delta V_{OS}$ | Change in $V_{OS}$ Between Complementary Output States | | — | — | 50 | mV |
| $I_{OS}$ | Outputs Short Circuit Current | $V_{OUT}$ + and $V_{OUT}$ - = 0V | — | 12 | 24 | mA |
| $I_{OSD}$ | Differential Outputs Short Circuit Current | $V_{OUT}$ + = $V_{OUT}$ - | — | 6 | 12 | mA |

**NOTES:**

1. See RECOMMENDED OPERATING RANGE table.
2. Typical values are at $V_{DD}$ = 2.5V, $T_A$ = +25°C ambient.

## DIFFERENTIAL INPUT AC TEST CONDITIONS FOR HSTL

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| $V_{DIF}$ | Input Signal Swing(1) | 1 | V |
| $V_X$ | Differential Input Signal Crossing Point(2) | 750 | mV |
| $D_H$ | Duty Cycle | 50 | % |
| $V_{THI}$ | Input Timing Measurement Reference Level(3) | Crossing Point | V |
| $t_R$, $t_F$ | Input Signal Edge Rate(4) | 2 | V/ns |

**NOTES:**

1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the $V_{DIF}$ (AC) specification under actual use conditions.
2. A 750mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the $V_X$ specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

## DIFFERENTIAL INPUT AC TEST CONDITIONS FOR eHSTL

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| $V_{DIF}$ | Input Signal Swing(1) | 1 | V |
| $V_X$ | Differential Input Signal Crossing Point(2) | 900 | mV |
| $D_H$ | Duty Cycle | 50 | % |
| $V_{THI}$ | Input Timing Measurement Reference Level(3) | Crossing Point | V |
| $t_R$, $t_F$ | Input Signal Edge Rate(4) | 2 | V/ns |

**NOTES:**

1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the $V_{DIF}$ (AC) specification under actual use conditions.
2. A 900mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the $V_X$ specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

## DIFFERENTIAL INPUT AC TEST CONDITIONS FOR LVEPECL (2.5V) AND LVPECL (3.3V)

| Symbol | Parameter | | Value | Units |
|---|---|---|---|---|
| $V_{DIF}$ | Input Signal Swing(1) | | 732 | mV |
| $V_X$ | Differential Input Signal Crossing Point(2) | LVEPECL | 1082 | mV |
| | | LVPECL | 1880 | |
| $D_H$ | Duty Cycle | | 50 | % |
| $V_{THI}$ | Input Timing Measurement Reference Level(3) | | Crossing Point | V |
| $t_R$, $t_F$ | Input Signal Edge Rate(4) | | 2 | V/ns |

**NOTES:**

1. The 732mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the $V_{DIF}$ (AC) specification under actual use conditions.
2. 1082mV LVEPECL (2.5V) and 1880mV LVPECL (3.3V) crossing point levels are specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the $V_X$ specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

## DIFFERENTIAL INPUT AC TEST CONDITIONS FOR LVDS

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| $V_{DIF}$ | Input Signal Swing[1] | 400 | mV |
| $V_X$ | Differential Input Signal Crossing Point[2] | 1.2 | V |
| $D_H$ | Duty Cycle | 50 | % |
| $V_{THI}$ | Input Timing Measurement Reference Level[3] | Crossing Point | V |
| $t_R$, $t_F$ | Input Signal Edge Rate[4] | 2 | V/ns |

**NOTES:**

1. The 400mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the $V_{DIF}$ (AC) specification under actual use conditions.
2. A 1.2V crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the $V_X$ specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

## AC DIFFERENTIAL INPUT SPECIFICATIONS(1)

| Symbol | Parameter | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|
| $V_{DIF}$ | AC Differential Voltage[2] | 0.1 | — | 3.6 | V |
| $V_{IX}$ | Differential Input Crosspoint Voltage | 0.05 | — | $V_{DD}$ | V |
| $V_{CM}$ | Common Mode Input Voltage Range[3] | 0.05 | — | $V_{DD}$ | V |
| $V_{IN}$ | Input Voltage | - 0.3 | | +3.6 | V |

**NOTES:**

1. The output will not change state until the inputs have crossed and the minimum differential voltage range defined by $V_{DIF}$ has been met or exceeded.
2. $V_{DIF}$ specifies the minimum input voltage ($V_{TR}$ - $V_{CP}$) required for switching where $V_{TR}$ is the "true" input level and $V_{CP}$ is the "complement" input level. The AC differential voltage must be achieved to guarantee switching to a new state.
3. $V_{CM}$ specifies the maximum allowable range of ($V_{TR}$ + $V_{CP}$) /2.

## POWER SUPPLY CHARACTERISTICS FOR LVDS OUTPUTS(1)

| Symbol | Parameter | Test Conditions | Typ. | Max | Unit |
|---|---|---|---|---|---|
| $I_{DDQ}$ | Quiescent $V_{DD}$ Power Supply Current | $V_{DD}$ = Max., All Input Clocks = LOW[2] Outputs enabled | — | 240 | mA |
| $I_{TOT}$ | Total Power $V_{DD}$ Supply Current | $V_{DD}$ = 2.7V., $F_{REFERENCE\ CLOCK}$ = 1GHz | — | 250 | mA |
| $I_{PD}$ | Total Power Down Supply Current | PD = LOW | — | 5 | mA |

**NOTES:**

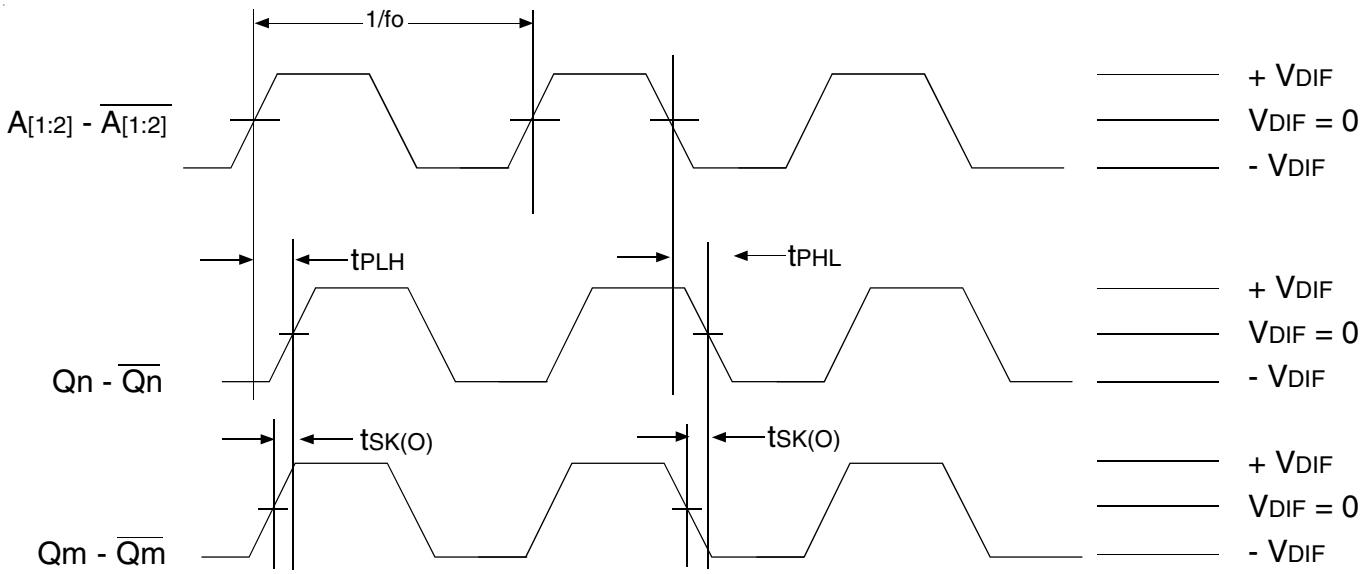
1. These power consumption characteristics are for all the valid input interfaces and cover the worst case conditions.
2. The true input is held LOW and the complementary input is held HIGH.

## AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE(1,5)

| Symbol | Parameter | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|
| **Skew Parameters** | | | | | |
| $t_{SK(O)}$ | Same Device Output Pin-to-Pin Skew(2) | — | — | 25 | ps |
| $t_{SK(P)}$ | Pulse Skew(3) | — | — | 125 | ps |
| $t_{SK(PP)}$ | Part-to-Part Skew(4) | — | — | 300 | ps |
| **Propagation Delay** | | | | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay A, A Crosspoint to Qn, Qn Crosspoint | — | 1.25 | 1.75 | ns |
| $f_O$ | Frequency Range(6) | — | — | 1 | GHz |
| **Output Gate Enable/Disable Delay** | | | | | |
| $t_{PGE}$ | Output Gate Enable Crossing $V_{THI}$ to Qn/Qn Crosspoint | — | — | 3.5 | ns |
| $t_{PGD}$ | Output Gate Disable Crossing $V_{THI}$ to Qn/Qn Crosspoint Driven to GL Designated Level | — | — | 3.5 | ns |
| **Power Down Timing** | | | | | |
| $t_{PWRDN}$ | PD Crossing $V_{THI}$ to Qn = $V_{DD}$, Qn = $V_{DD}$ | — | — | 100 | µS |
| $t_{PWRUP}$ | Output Gate Disable Crossing $V_{THI}$ to Qn/Qn Driven to GL Designated Level | — | — | 100 | µS |
| **RMS Additive Phase Jitter** | | | | | |
| $t_{JIT}$ | RMS Additive Phase Jitter @ 25MHz (12kHz – 10MHz Integration Range) | | 0.541 | | ps |
| | RMS Additive Phase Jitter @ 125MHz (12kHz – 20MHz Integration Range) | | 0.159 | | ps |
| | RMS Additive Phase Jitter @ 156.25MHz (12kHz – 20MHz Integration Range) | | 0.185 | | ps |

**NOTES:**
1. AC propagation measurements should not be taken within the first 100 cycles of startup.
2. Skew measured between crosspoints of all differential output pairs under identical input and output interfaces, transitions and load conditions on any one device.
3. Skew measured is the difference between propagation delay times $t_{PHL}$ and $t_{PLH}$ of any differential output pair under identical input and output interfaces, transitions and load conditions on any one device.
4. Skew measured is the magnitude of the difference in propagation times between any single differential output pair of two devices, given identical transitions and load conditions at identical $V_{DD}$ levels and temperature.
5. All parameters are tested with a 50% input duty cycle.
6. Guaranteed by design but not production tested.

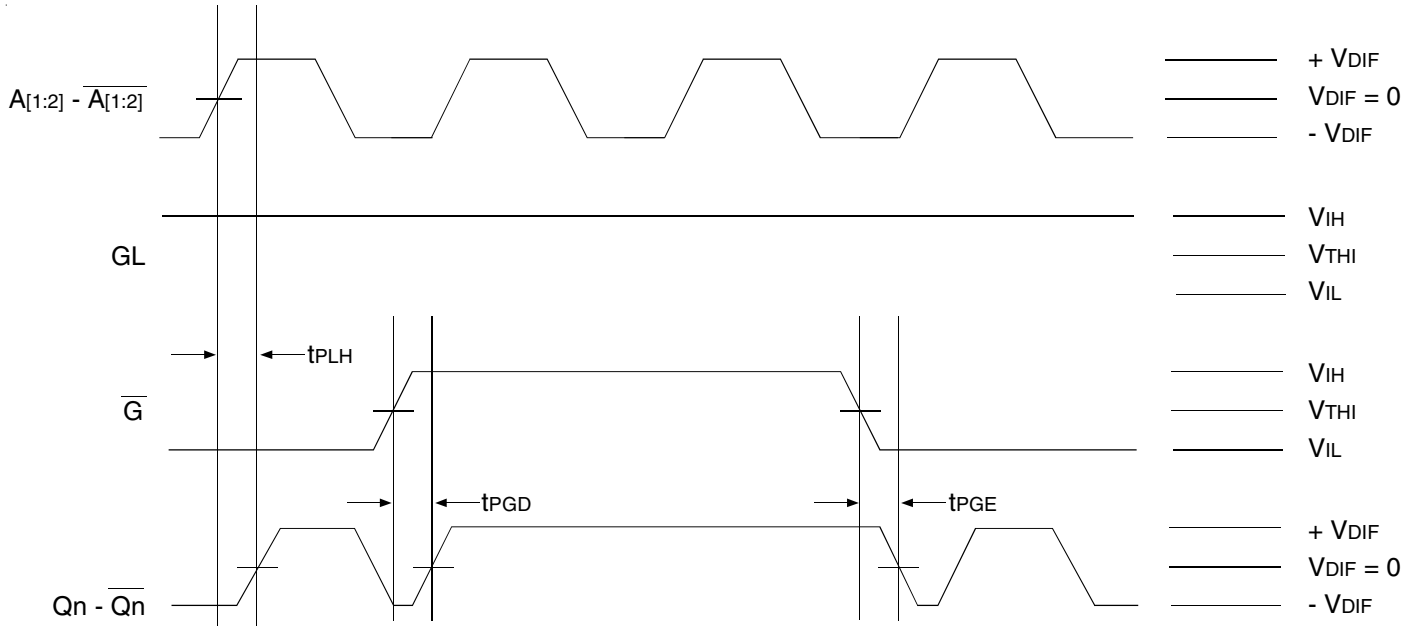
# DIFFERENTIAL AC TIMING WAVEFORMS




***Output Propagation and Skew Waveforms***

**NOTES:**

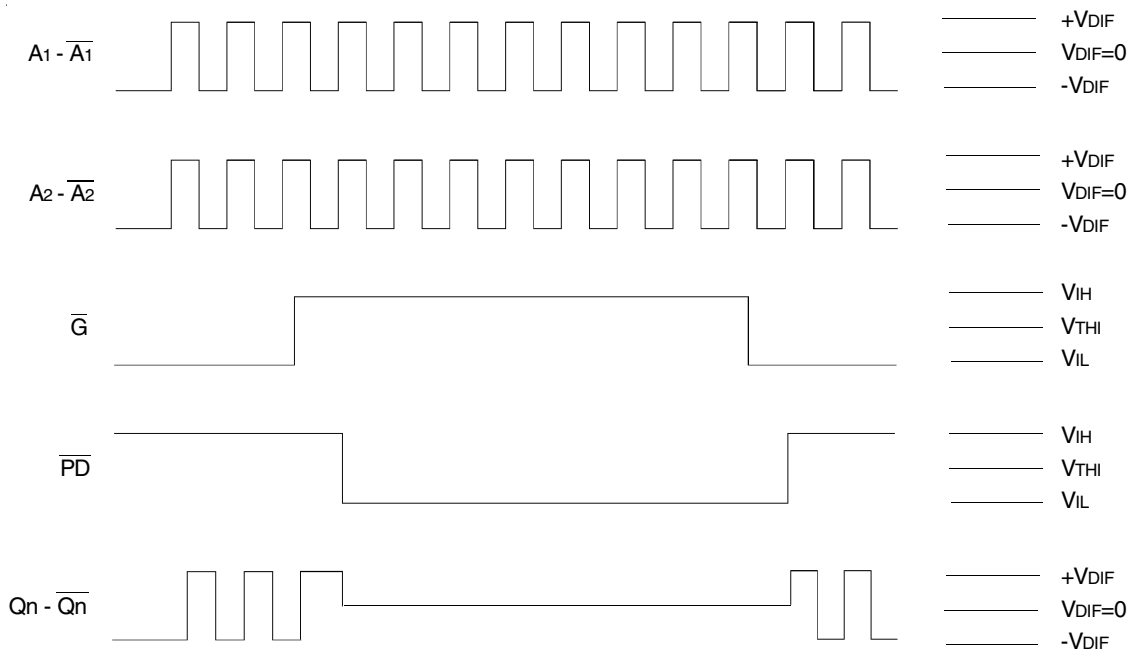
1. Pulse skew is calculated using the following expression:
   $t_{SK(P)} = | t_{PHL} - t_{PLH} |$
   Note that the $t_{PHL}$ and $t_{PLH}$ shown above are not valid measurements for this calculation because they are not taken from the same pulse.
2. AC propagation measurements should not be taken within the first 100 cycles of startup.




***Differential Gate Disable/Enable Showing Runt Pulse Generation***

**NOTE:**

1. As shown, it is possible to generate runt pulses on gate disable and enable of the outputs. It is the user's responsibility to time the G signal to avoid this problem.

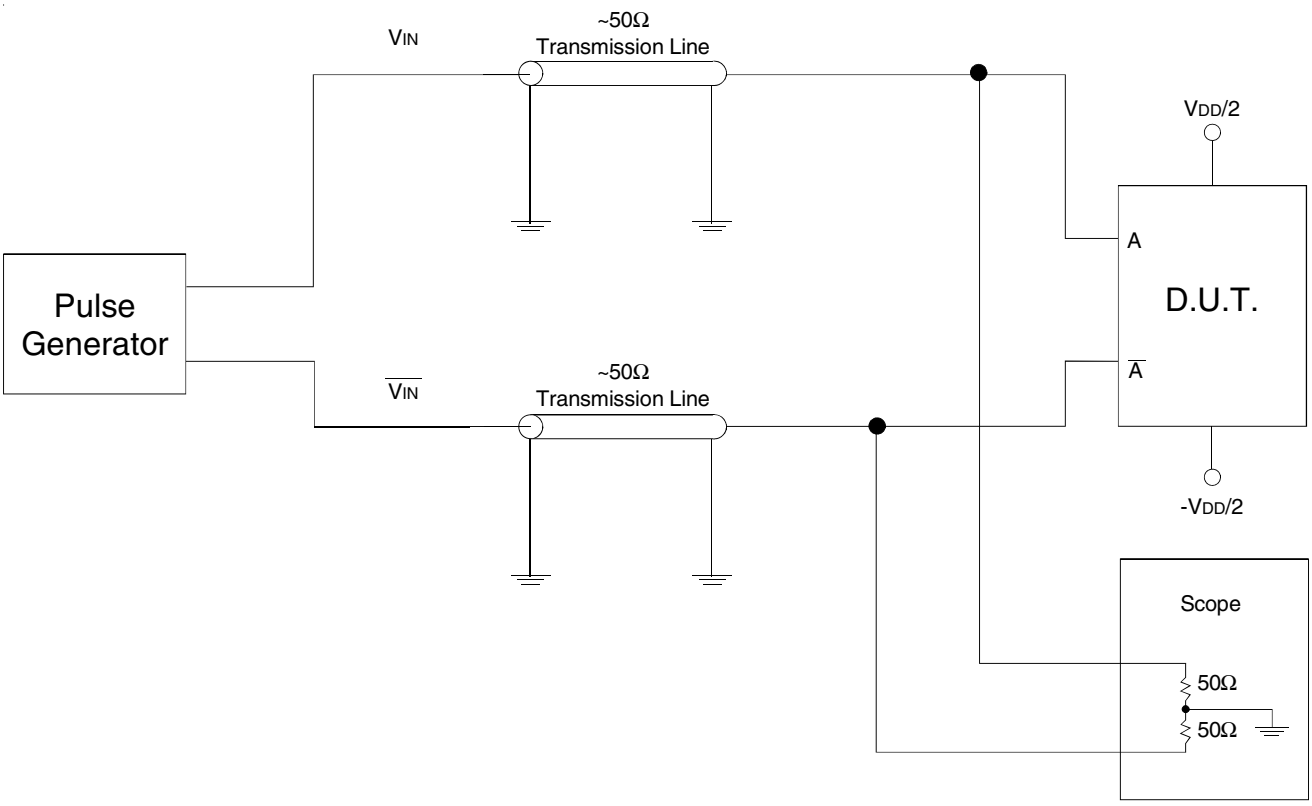



***Power Down Timing***

**NOTES:**

1. It is recommended that outputs be disabled before entering power-down mode. It is also recommended that the outputs remain disabled until the device completes power-up after asserting PD.
2. The POWER DOWN TIMING diagram assumes that GL is HIGH.
3. It should be noted that during power-down mode, the outputs are both pulled to VDD. In the POWER DOWN TIMING diagram this is shown when Qn-Qn goes to VDIF = 0.

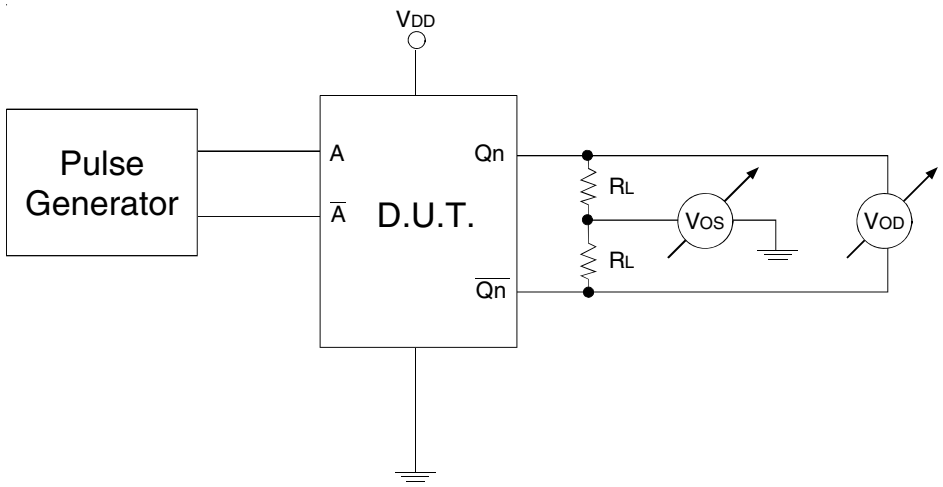
# TEST CIRCUITS AND CONDITIONS



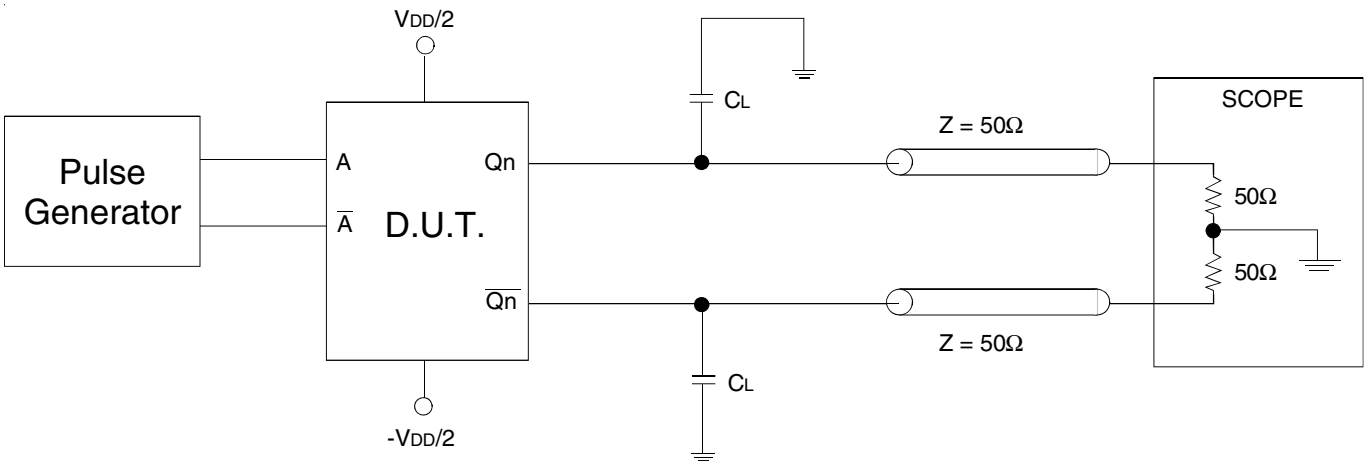

***Test Circuit for Differential Input***

## DIFFERENTIAL INPUT TEST CONDITIONS

| Symbol | $V_{DD}$ = 2.5V ± 0.2V | Unit |
|---|---|---|
| $V_{THI}$ | Crossing of A and A | V |




***Test Circuit for DC Outputs and Power Down Tests***




***Test Circuit for Propagation, Skew, and Gate Enable/Disable Timing***

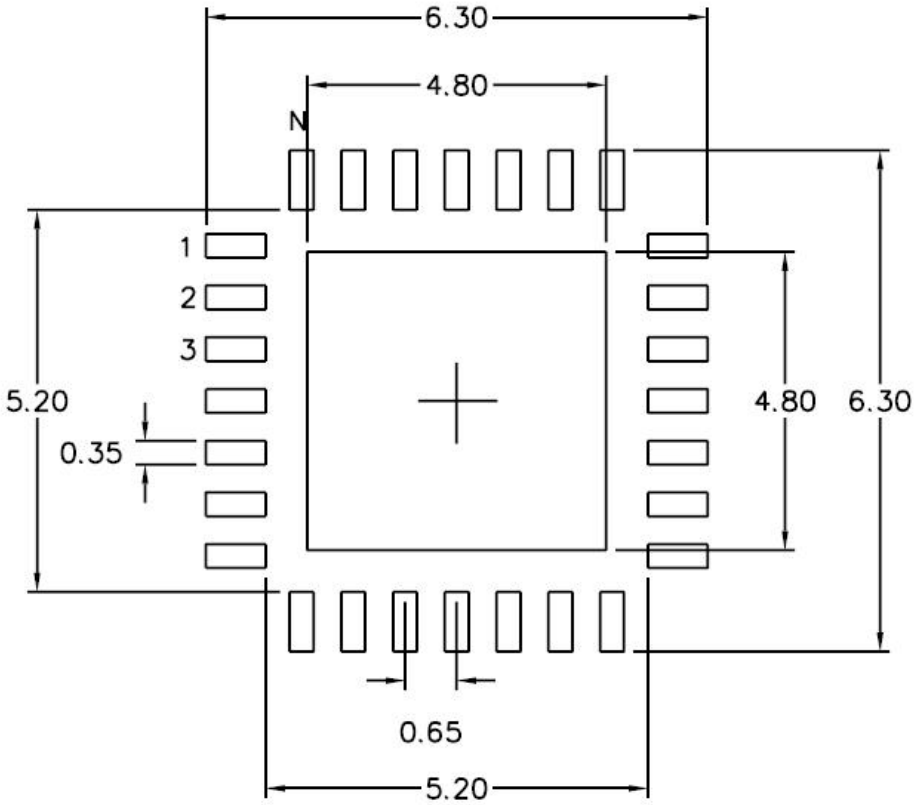
## LVDS OUTPUT TEST CONDITION

| Symbol | VDD = 2.5V ± 0.2V | Unit |
|---|---|---|
| CL | 0(1) | pF |
| | 8(1,2) | |
| RL | 50 | Ω |

**NOTES:**

1. Specifications only apply to "Normal Operations" test condition. The TIA/EIA specification load is for reference only.
2. The scope inputs are assumed to have a 2pF load to ground. TIA/EIA - 644 specifies 5pF between the output pair. With CL = 8pF, this gives the test circuit appropriate 5pF equivalent load.

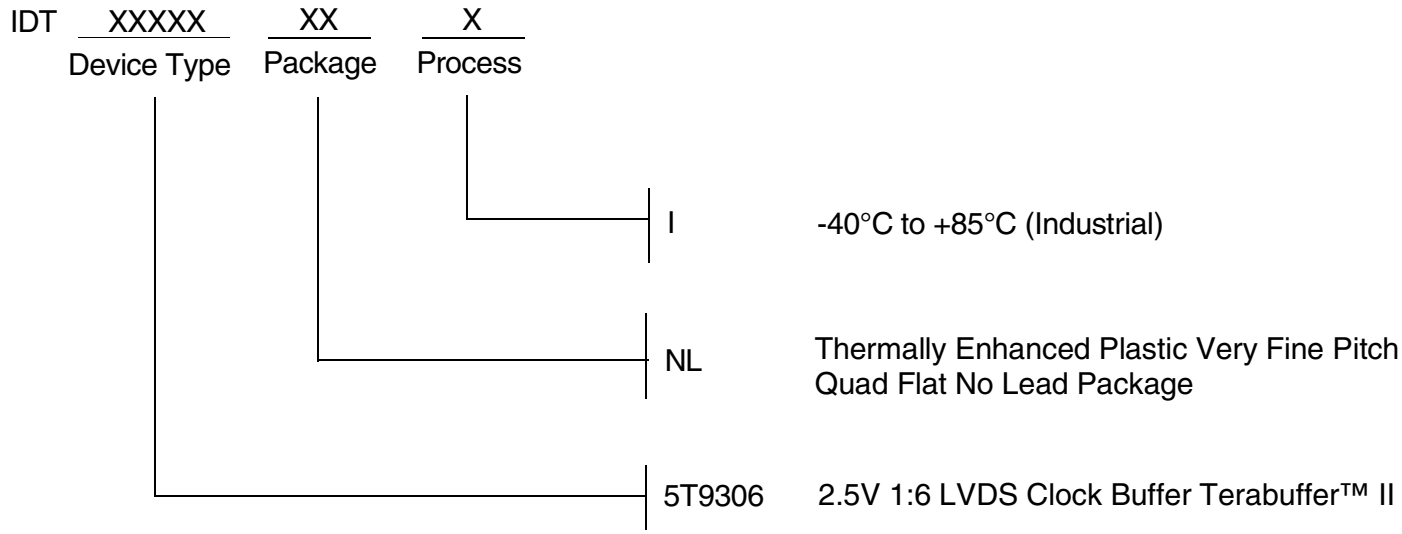
## RECOMMENDED LANDING PATTERN




*NL 28 pin*

**NOTE:** All dimensions are in millimeters.

## ORDERING INFORMATION

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