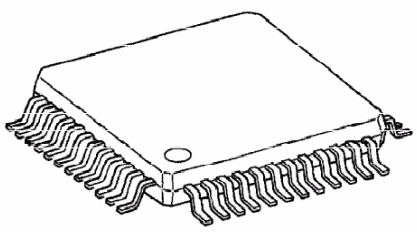
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA1375FG

Single Conversion Tuner for Digital TV / CATV

The TA1375FG is a tuner IC for for Digital TV and CATV applications that integrates a PLL block and mixer, oscillator, IF amplifier and IF GCA on a single chip.
This oscillator and PLL circuits are low phase noise.
The control data of the PLL block conforms to I²C-bus formats.
Small flat package : LQFP48(0.5mm pitch)



LQFP48-P-0707-0.5

Weight: 0.17g (typ.)

Features

- Vcc: 5V（typ.）
- Two-band mixer
- Three-band oscillator
- Low phase noise oscillator circuit
- Built-In IF GCA circuit
- IF output driver
- GCA block: Gain changeover switch (3dB shift possible)
- Direct 2 modulus type frequency synthesizer
- I²C bus format control
- 33V high voltage tuning amplifier built-in
- Four-bit bandswitch drive transistor
- Frequency step : 50kHz, 62.5kHz, 142.86kHz, 166.67kHz (when a 4MHz crystal is used.)
- Four-programmable chip address
- Power-on reset circuit
- Package: Pb-free

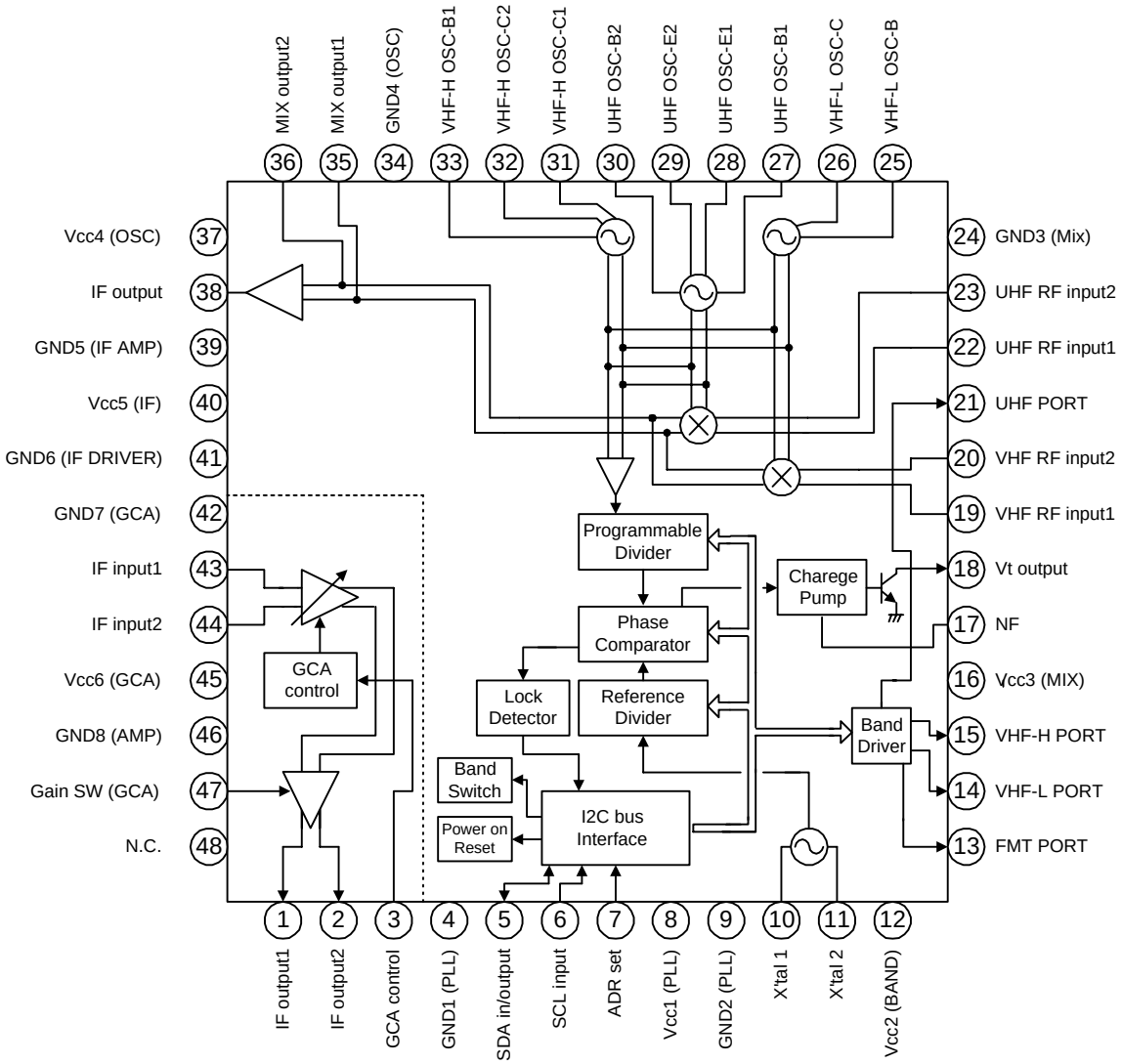
Power on reset status

- Frequency step : [62.5kHz]
- Charge pump current: [Low]
- Counter data: ALL [0]
- Band driver: [OFF]
- Tuning amplifier: [OFF] (charge pump is sink mode)
- Local oscillator and mixer: ALL [OFF]

note1: These devices are easy to be damaged by high voltage or electric fields. In regards to this, please handle with care.

note2: Install the product correctly. Otherwise, it may result in break down, damage and/or degration to the product or equipment.

Block Diagram



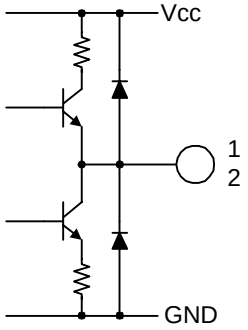
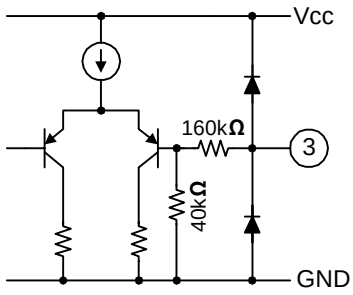
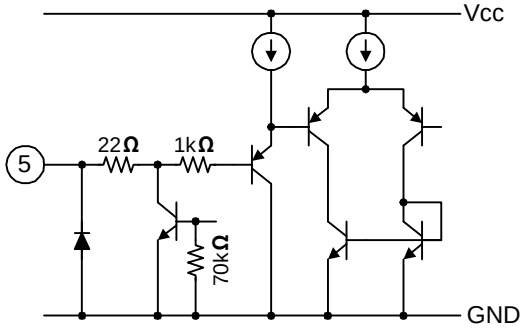
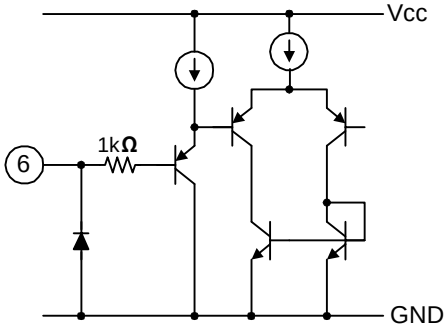
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purpose.

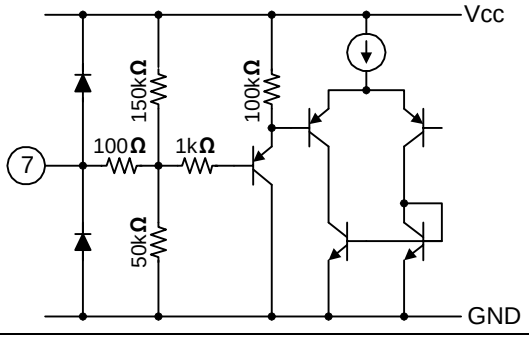
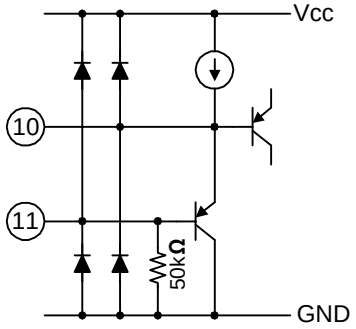
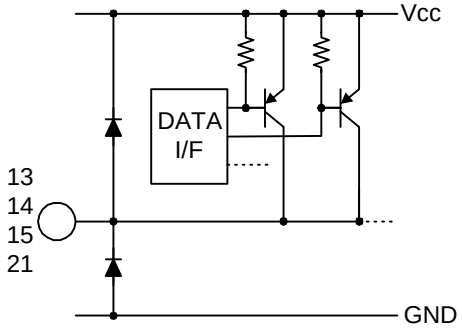
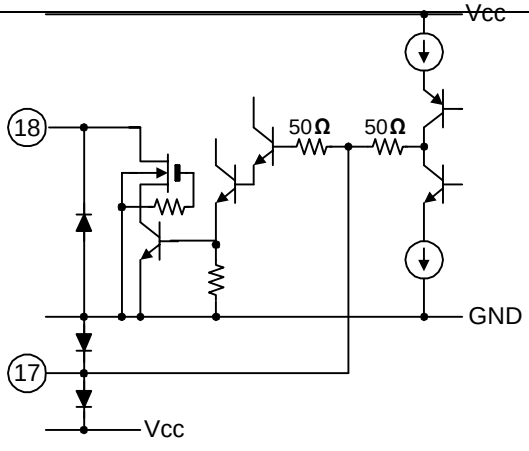
Terminal Name

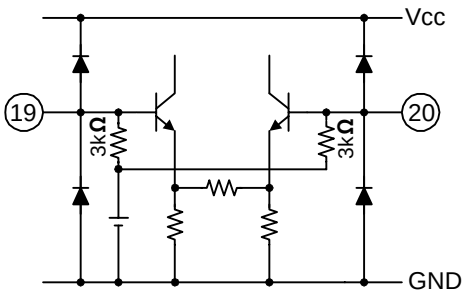
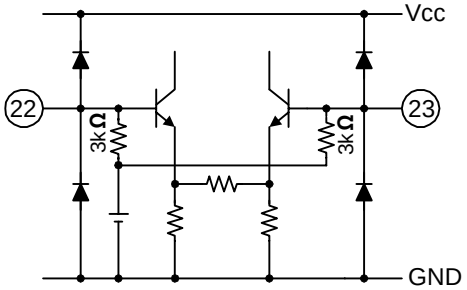
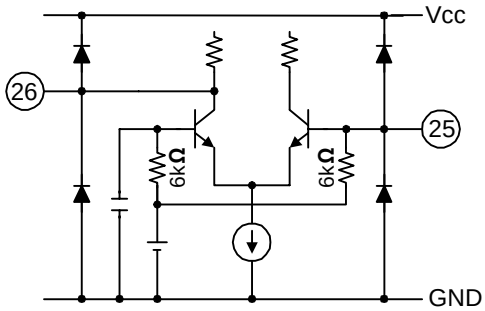
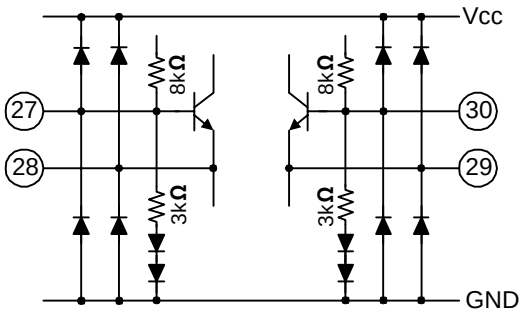
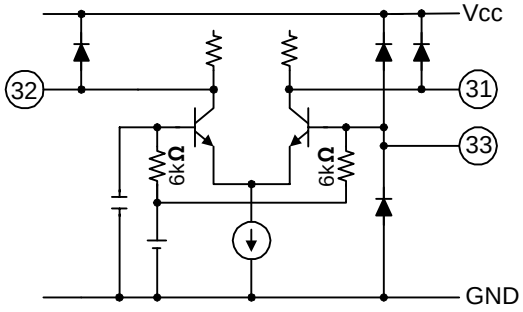
Pin No.	Pin name
1	IF output 1
2	IF output 2
3	GCA control terminal
4	GND 1 (PLL)
5	SDA In/out
6	SCL In
7	ADR set (address setting)
8	Vcc 1 (PLL)
9	GND 2 (PLL)
10	Crystal 1
11	Crystal 2
12	Vcc 2 (BAND)
13	FMT port (NPN-Tr)
14	VHF-L port (NPN-Tr)
15	VHF-H port (NPN-Tr)
16	Vcc 3 (MIX)
17	NF
18	Vt output
19	VHF RF Input 1
20	VHF RF Input 2
21	UHF port (NPN-Tr)
22	UHF RF Input 1
23	UHF RF Input 2
24	GND 3 (MIX)
25	VHF-L OSC-base
26	VHF-L OSC-collector
27	UHF OSC-base1
28	UHF OSC-emitter1
29	UHF OSC-emitter2
30	UHF OSC-base2
31	VHF-H OSC-collector1
32	VHF-H OSC-collector2
33	VHF-H OSC-base1
34	GND 4 (OSC)
35	MIX output 1
36	MIX output 2
37	Vcc 4 (OSC)
38	IF out
39	GND 5 (IF AMP)
40	Vcc 5 (IF)
41	GND 6 (IF DRIVER)
42	GND 7 (GCA)
43	IF Input 1
44	IF Input 2
45	Vcc 6 (GCA)
46	GND 8 (AMP)
47	Gain SW（GCA） （Open: typical / GND:＋3dB gain up）
48	N.C. （This pin does not connect the Inside circuit.）

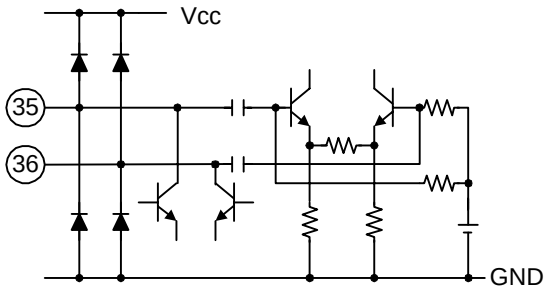
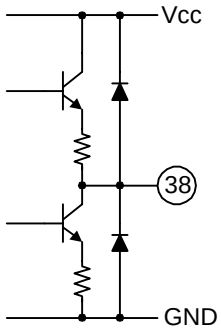
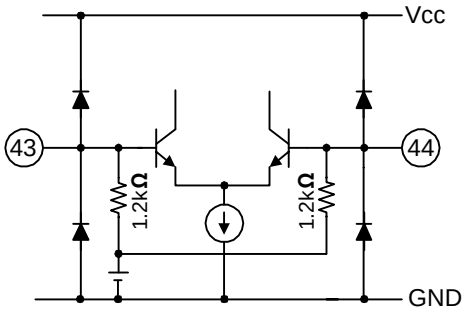
Terminal Function

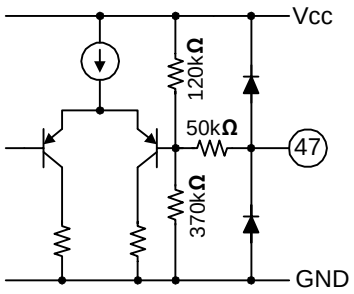
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purpose.

Pin No.	Pin Name.	Function	Interface
1 2	IF output	IF output pin for the GCA block. Symmetrical output type.	
3	GCA control	Gain control pin of GCA block. The gain of GCA block Is controllable by the voltage given to this pin.	
4	GND1	This Is the ground pin for the PLL circuit.	—
5	SDA	Serial data Input and output pin	
6	SCL	Serial clock Input pin	

Pin No.	Pin Name.	Function	Interface
7	ADR set	Address setting pin The address of the PLL block Is set up using the voltage applied to this pin.	
8	Vcc1	This Is power supply for the PLL circuit.	—
9	GND2	This Is the ground pin for the PLL circuit.	—
10 11	Crystal	Crystal oscillator input pins. A 4MHz crystal is used.	
12	Vcc2	This Is power supply for the Band circuit.	—
13 14 15 21	Band driver Output port	The output port of the band block can be set up using the control data. Bear in mind that drive current differs according to each band drive port.	
16	Vcc3	This Is power supply for the Mixer circuit.	—
17	NF	Be sure to connect a resistance (of about 33kΩ) between pin18 and the 33V external power supply for tuning. To prevent abnormal oscillation, connect between pin18 and GND a capacity element that does not affect a PLL.	
18	Vt output		

Pin No.	Pin Name.	Function	Interface
19 20	VHF RF input	RF signal Input pin for the VHF band. It can be symmetrical Input, asymmetrical Input by grounding of one pin with a capacity element.	
22 23	UHF RF input	RF signal Input pin for the UHF band. It can be symmetrical Input, asymmetrical Input by grounding of one pin with a capacity element.	
24	GND3	This Is the ground pin for the Mixer circuit.	—
25 26	VHF-L band Local oscillator	Local oscillator for the VHF-L band The oscillator type Is symmetrical amplifier.	
27 28 29 30	UHF band Local oscillator	Local oscillator for the UHF band The oscillator type Is balanced clap.	
31 32 33	VHF-H band Local oscillator	Local oscillator for the VHF-H band The oscillator type Is symmetrical amplifier.	

Pin No.	Pin Name.	Function	Interface
34	GND4	This Is the ground pin for the Local oscillator circuit.	—
35 36	Mixer ouytput	Mixer output pins A tank circuit Is connected between the pins for tuning. Since these are open collector outputs, be sure to connect with a power supply through a load. (resistance, coil).	
37	Vcc4	This Is power supply for the Local oscillator circuit.	—
38	IF output (MOP)	IF output pin for the MOP block Asymmetrical output type.	
39	GND5	This Is the ground pin for the IF amplifier circuit.	—
40	Vcc5	This Is power supply for the IF circuit.	—
41	GND6	This Is the ground pin for the IF output circuit.	—
42	GND7	This Is the ground pin for the GCA circuit.	—
43 44	IF Input	IF input pin for the GCA block. Symmetrical Input type.	

Pin No.	Pin Name.	Function	Interface
45	Vcc6	This Is power supply for the GCA circuit.	—
46	GND8	This Is the ground pin for the GCA output circuit.	—
47	Gain SW (GCA)	It Is the voltage gain changeover SW. It changes by setting this pin to Open or GND. When based on an open state, about 3dB voltage gain can be increased by setting a pin to GND.	
48	N.C.	This pin does not connect the Inside circuit.	—

Maximum Ratings

CHARACTERISTIC	PIN No	SYMBOL	RATING	UNIT
Vcc	8	Vcc1	6	V
	12	Vcc2	6	
	16	Vcc3	6	
	37	Vcc4	6	
	40	Vcc5	6	
	45	Vcc6	6	
Tuning Amplifier Voltage Applied	18	VBT	38	V
Input Terminal Voltage	—	VIN	GND-0.3～Vcc+0.3	V
Power Dissipation	—	PD	1190 (note4)	mW
Operating Temperature	—	Topr	-20～85	℃
Storage Temperature	—	Tstg	-55～150	℃

note3: The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant. If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause break down, damage and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions. Before using, creating and/or producing designs, refer to and comply with the precautions and conditions set forth in this documents.

note4: 50 × 50 × 1.6mm, Cu36% board used. When using the device at above Ta=25℃, decrease the power dissipation by 9.6mW for each Increase of 1℃

Operating Supply Voltage

Pin No.	SYMBOL	MIN.	TYP.	MAX.	UNIT
8	Vcc1 (PLL)	4.5	5.0	5.25	V
12	Vcc2 (BAND)	4.5	5.0	5.25	
16	Vcc3 (MIX)	4.5	5.0	5.25	
37	Vcc4 (OSC)	4.5	5.0	5.25	
40	Vcc5 (IF)	4.5	5.0	5.25	
45	Vcc6 (GCA)	4.5	5.0	5.25	

Electric Characteristics

(Unless otherwise specified,Vcc1 = Vcc2 = Vcc3 = Vcc4 = Vcc5 = Vcc6 = 5V, Ta = 25℃)

CHARACTERISTICS	SYMBOL	TEST CIRC-UIT	BAND	TEST CONDITION (note5,6,7)	MIN.	TYP.	MAX.	UNIT
Power Supply and current Icc1+Icc2+Icc3+Icc4+Icc5+Icc6(total)	Icc (total)	1	VHF-L	Bus data :B1 : ON(IBD=0mA)	73	88	108	mA
			VHF-H	Bus data :B2 : ON(IBD=0mA)	73	88	108	
			UHF	Bus data :B3 or B4 : ON(IBD=0mA)	76	91	111	
Down Converter Block								
Conversion Gain (see1)	CG	3	VHF-L	RF=90MHz -30dBmWin	19.0	21.5	24.0	dB
			VHF-H	RF=465MHz -30dBmWin	20.5	23.0	25.5	
			UHF	RF=471MHz -30dBmWin	22.0	24.5	27.0	
			UHF	RF=855MHz -30dBmWin	21.5	24.0	26.5	
IF Output Power Level (see2)	Ifp	3	VHF-L	RF=90MHz	9	10	—	dBmW
			VHF-H	RF=465MHz	9	10	—	
			UHF	RF=471MHz	9	10	—	
			UHF	RF=855MHz	9	10	—	
Conversion Gain Shift (see3)	CGs	3	VHF-L	RF=90MHz –30dBmWin	—	—	±0.5	dB
			VHF-H	RF=465MHz -30dBmWin	—	—	±0.5	
			UHF	RF=471MHz -30dBmWin	—	—	±1.0	
			UHF	RF=855MHz -30dBmWin	—	—	±1.0	
Gain Control Amplifier Block (Pin47 = Open)								
Maximum Voltage Gain	VGmax	3	—	VGCA=3V, RF=-60dBmW	45.0	47.0	49.0	dB
Typical Voltage Gain	VGtyp	3	—	VGCA=1.7V, RF=-37.5dBmW	21.5	23.5	25.5	
Minimum Voltage Gain	VGmin	3	—	VGCA=0.5V, RF=-15dBmW	-5.0	-3.0	-1.0	
Gain Variable Range	GR	3	—	VGCA=0.5～3V	46	50	54	dB
Gain Control Sensitivity	Sgain	3	—	VGCA=1.7V	27	30	33	dB/V
Linearity	LGCA	3	—	VGCA=1.1～2.3V	—	—	±1	dB
Maximum Output Signal Amplitude	Vomax	3	—	—	1.5	—	—	Vp-p
Flow Into Current of PIN3	Cont-I	3	—	Pin3 (apply voltage=0～Vcc6)	—	—	50	uA
PLL Block								
Band Port Drive Current	IBD-FMT	1	—	Pin13 (FMT port)	—	—	5	mA
	IBD-VHF		—	Pin14,15 (VHF port)	—	—	20	
	IBD-UHF		—	Pin21 (UHF port)	—	—	15	
Band Port Drive Maximum Current	IBDmax	1	—	Maximum drive current / 2 port ON	—	—	25	mA
Band Port Drive Voltage Drop	VBDsat	1	—	With each port at maximum current drive. 1 port ON	—	0.15	0.2	V
Tuning Amplifier Output Voltage (Close Loop)	Vt out	3	—	Isink = 3mA	0.3	—	33	V
Tuning Amplifier Maximum Current	Ivt	3	—	VBT = 33V	—	—	3	mA
Crystal Negative Resistance	XtR	1	—	—	1.2	1.5	—	kΩ
Ratio Setting Range	N	-	—	15-bits counter	1024	—	32767	Ratio
Logic Input Low Voltage	VBsL	1	—	Pin5,6	-0.3	—	1.1	V
Logic Input High Voltage	VBsH	1	—	Pin5,6	2.0	—	Vcc2 +0.3	V
Logic Input Current (Low)	I BsL	1	—	Pin5,6	-20	—	10	uA
Logic Input Current (High)	I BsH	1	—	Pin5,6	-10	—	20	uA
Charge Pump Output Current	Ichg	1	—	CP = 0	±115	±145	±175	uA
			—	CP = 1	±165	±210	±255	
ACK Output Voltage	VACK	1	—	Isink = 3mA	—	—	0.4	V

note5: IF output frequency=43.75MHz、note6: IF output load=75Ω、note7: VGCA=voltage value applied to Pin3

Reference Data (Unless otherwise specified,Vcc1=Vcc2=Vcc3=Vcc4=Vcc5=Vcc6=5V, Ta = 25℃)

(The data is a reference value and is not guaranteed.)

CHARACTERISTICS	SYMBOL	TEST CIRCUIT	BAND	TEST CONDITION (note5,6,7)	MIN.	TYP.	MAX.	UNIT
Down Converter Block								
Noise Figure (MO) (see4)	NF	3, 4	VHF-L	RF=90MHz	—	13.5	15.0	dB
			VHF-H	RF=465MHz	—	11.0	12.5	
			UHF	RF=471MHz	—	11.5	13.0	
			UHF	RF=855MHz	—	11.0	12.5	
OSC Frequency Shift (The PLL is not operating) (see5)	△fB	3	VHF-L	OSC=133.75MHz	—	—	±200	kHz
			VHF-H	OSC=508.75MHz	—	—	±500	
			UHF	OSC=514.75MHz	—	—	±500	
			UHF	OSC=898.75MHz	—	—	±500	
Switch On Drift (The PLL is not operating) (see6)	△fs	3	VHF-L	OSC=133.75MHz	—	—	±500	kHz
			VHF-H	OSC=508.75MHz	—	—	±1000	
			UHF	OSC=514.75MHz	—	—	±500	
			UHF	OSC=898.75MHz	—	—	±1000	
1% Cross Modulation (see7)	CM	3, 5	VHF-L	fd=90MHz	86	89	—	dBuV
			VHF-H	fd=465MHz	82	85	—	
			UHF	fd=471MHz	83	86	—	
			UHF	fd=855MHz	79	82	—	
3rd Inter Modulation (MO) (see8)	IM3-MO	3, 5	VHF-L	fd=90MHz	62	65	—	dB
			VHF-H	fd=465MHz	59	62	—	
			UHF	fd=471MHz	57	60	—	
			UHF	fd=855MHz	55	58	—	
Phase Noise (1kHz offset) (see9) freq-step=62.5kHz CP=Hi mode	PN1k	3	VHF-L	OSC=133.75MHz	—	-75	-68	dBc/Hz
			VHF-L	OSC=238.75MHz	—	-65	-58	
			VHF-H	OSC=244.75MHz	—	-72	-64	
			VHF-H	OSC=508.75MHz	—	-62	-58	
			UHF	OSC=514.75MHz	—	-65	-58	
			UHF	OSC=898.75MHz	—	-64	-58	
Phase Noise (10kHz offset) (see10) freq-step=62.5kHz CP=Hi mode	PN10k	3	VHF-L	OSC=133.75MHz	—	-89	-86	dBc/Hz
			VHF-L	OSC=238.75MHz	—	-89	-86	
			VHF-H	OSC=244.75MHz	—	-90	-86	
			VHF-H	OSC=508.75MHz	—	-88	-86	
			UHF	OSC=514.75MHz	—	-89	-86	
			UHF	OSC=898.75MHz	—	-90	-86	
Gain Control Amplifier Block (Pin47 = Open)								
Noise Figure (GCA)	Nfgca	3, 6	—	GR=0dB, DSB	—	4.7	6.2	dB
			—	GR=10dB, DSB	—	5.2	6.7	
			—	GR=20dB, DSB	—	7.0	8.0	
			—	GR=30dB, DSB	—	12.0	13.0	
			—	GR=40dB, DSB	—	20.5	21.5	
3rd Inter Modulation (GCA)	IM3-GCA	3, 7	—	f1=43.75MHz, f2=44.75MHz VGCA=3V(MAX Gain) V-out=0.5Vpp / tone	42	50	—	dB
			—	f1=43.75MHz, f2=44.75MHz VGCA=1.25V(Gain=10dB) V-out=0.5Vpp / tone	42	50	—	dB
PLL Block								
RF Input Maximum Level without Lock out	RF-in	3	—	Pin19,20,22,23	—	—	120	dBuV
Crystal External Input Minimum Level	Xoextl-l	2	—	4MHz signal input	300	—	—	mVp-p
Crystal External Input Maximum Level	Xoextl-h	2	—	4MHz signal input	—	—	1000	mVp-p
Crystal External Input Frequency	Xoextf	2	—	It is necessary D/U>10dB.	—	4	—	MHz

note5: IF output frequency=43.75MHz、note6: IF output load=75Ω、note7: VGCA=voltage value applied to Pin3

I²C Bus Line Characteristic

CHARACTERISTICS	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
SCL Clock Frequency	fscl	–	0	-	400	kHz
Bus Free Time between a STOP and a Start Condition	tBUF		1.3	-	-	us
Hold Time (Repeated) START Condition	tHD;STA		0.6	-	-	us
Low Period of the SCL Clock	tLOW		1.3	-	-	us
High Period of the SCL Clock	tHIGH		0.6	-	-	us
Set-up Time for a Repeated START Condition	tSU;STA		0.6	-	-	us
Data Hold Time	tHD;DAT		0	-	0.9	us
Data Set-up Time	tSU;DAT		100	-	-	ns
Rise Time of both SDA and SCL Signal	tR		-	-	300	ns
Fall Time of both SDA and SCL Signals	tF		-	-	300	ns
Set up Time for STOP Condition	tsU;STO		0.6	-	-	us

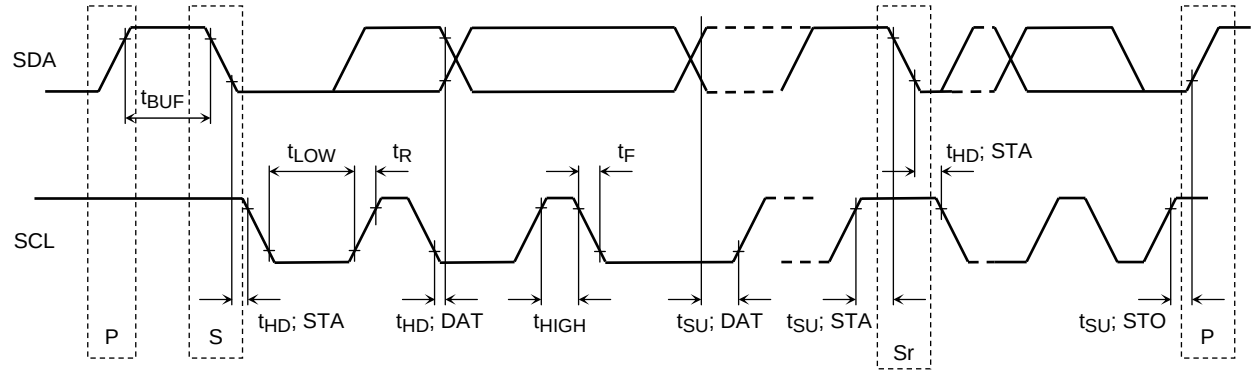


Figure.1 I²C-bus data timing chart (Rising edge timing)

Timing charts may be simplified for explanatory purposes.

Test Circuit

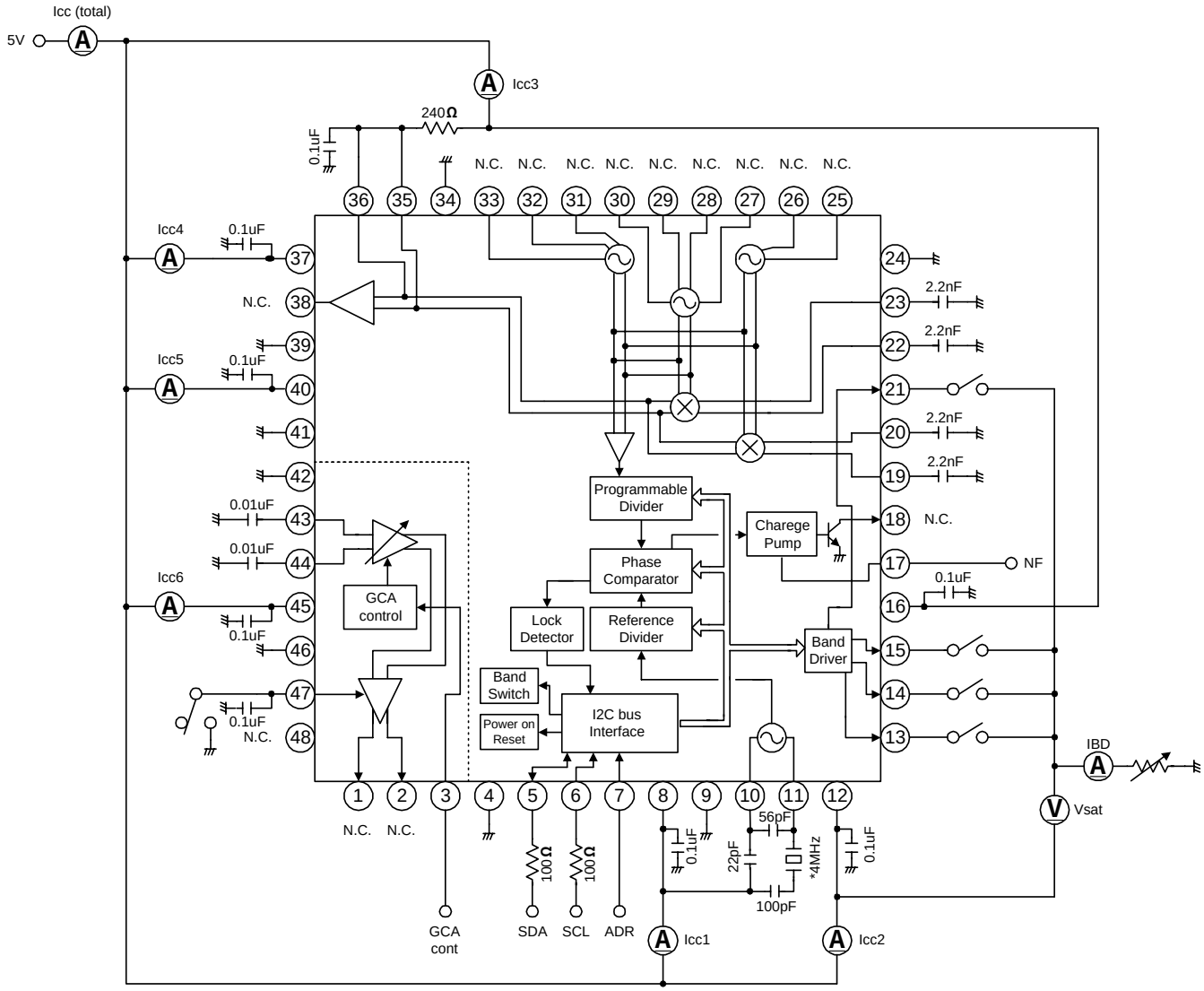


Figure.2 Test Circuit 1

note8: Components in the test circuits are only used to obtain and confirm the device characteristics. These components and circuits do not warrant to prevent the application equipment from malfunction or failure.

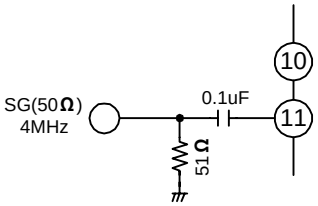


Figure.3 Test Circuit 2 (Crystal External Input)

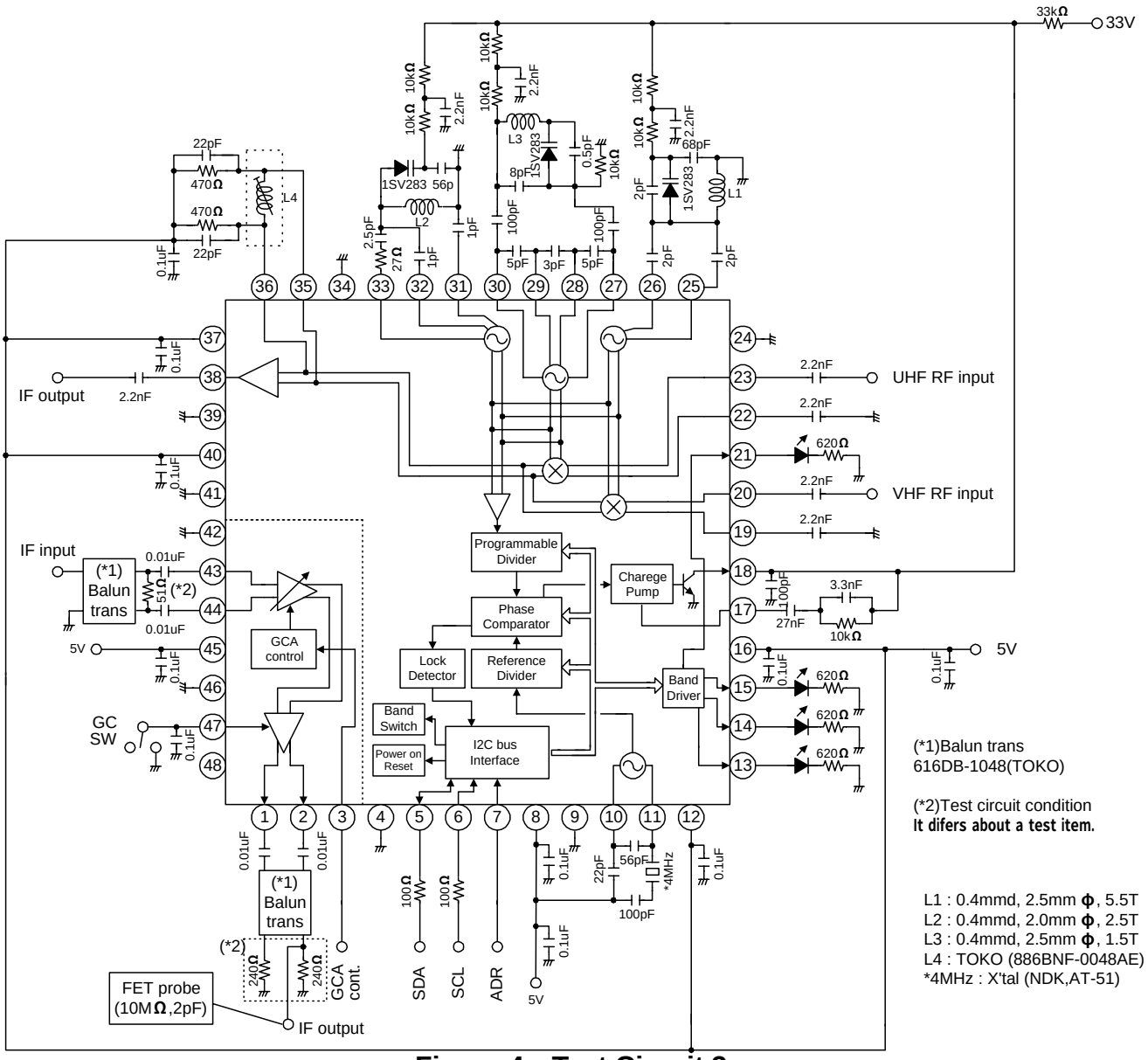
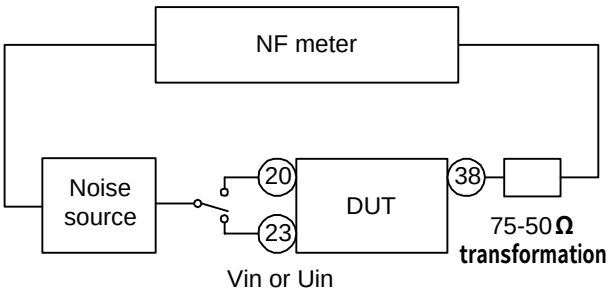


Figure.4 Test Circuit 3

note8: Components in the test circuits are only used to obtain and confirm the device characteristics. These components and circuits do not warrant to prevent the application equipment from malfunction or failure.



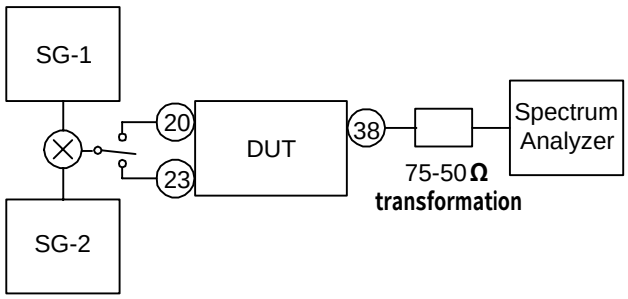


Figure.5 Test Circuit 4 (MOP Block : NF) **Figure.6 Test Circuit 5 (MOP Block : IM3 / CM)**

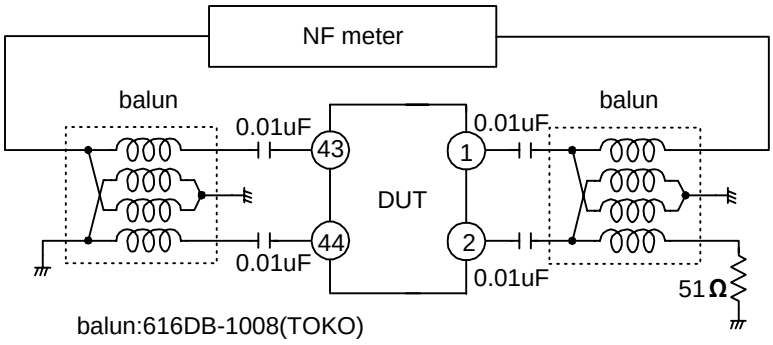


Figure.7　Test Circuit 6 (GCA Block : NF)

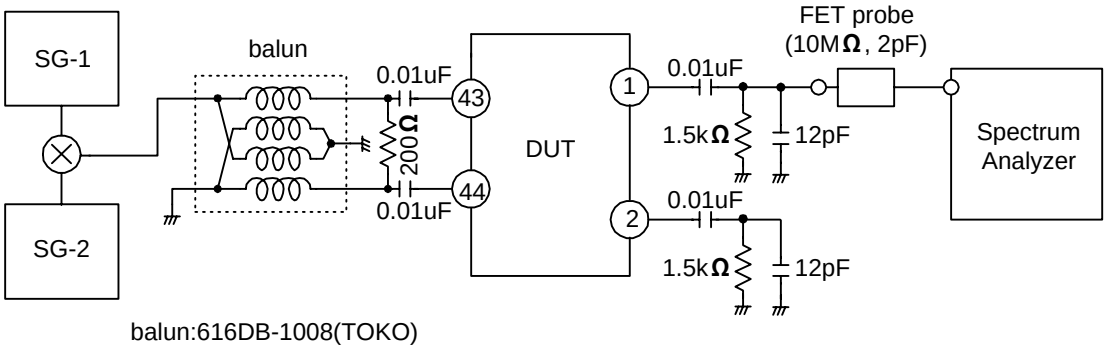


Figure.8　Test Circuit 7 (GCA Block : IM3)

MOP Block Test Conditions

(see1) Conversion Gain
RF Input level = -30dBmW (untuned)

(see2) IF Output Power Level
Measure IF output level when It is maximum level.

(see3) Conversion Gain Shift
The conversion gain shift Is defined as a change In conversion gain when supply voltage varies from Vcc=5V to 4.5V or From Vcc=5V to 5.25V.

(see4) Noise Figure (MO)
Noise figure meter used. Direct reading.

(see5) OSC Frequency Shift (The PLL is not operating)
The frequency shift Is defined as a change In oscillator frequency when supply voltage varies from Vcc=5V to 4.5V or From Vcc=5V to 5.25V.

(see6) Switch ON Drift (The PLL is not operating)
Measure frequency change from 2 seconds after switching on to 3 minutes.

(see7) 1% Cross Modulation
- fd = fp : (fd Input level = -30dBmW)
- fud = fp ±12MHz, 100kHz AM30%

Input two signals, and Increase the fud Input level.
Measure the fud Input level when the suppression level reaches 56.5dB.

(see8) 3rd Internal Modulation (MO)
- fd = fp : (fd Input level = -30dBmW)
- fud = fp ±1MHz : (fud Input level = -30dBmW)

Input two signals, measure the suppression level.

(see9) Phase Noise (1kHz offset)
Measure the phase noise at 1kHz offset. (PLL setting; frequency step = 62.5kHz / charge pump current = High mode)
RF Input level = -30dBmW

(see10) Phase Noise (10kHz offset)
Measure the phase noise at 10kHz offset. (PLL setting; frequency step = 62.5kHz / charge pump current = High mode)
RF Input level = -30dBmW

Description of PLL Block Operation

- I²C bus control -

The TA1375FG conforms to the I²C-bus format.
The I²C-bus mode enables two-way bus communications with Write Mode, which receives data, and Read Mode, which sends data.
Write Mode and Rear Mode are set using the last bit (R/W bit) of the address byte. If the last address bit is set to [0], Write Mode is selected; if it is set to [1], Read Mode is selected.
Address can be set using the hardware bits and four programmable address are available.
With this setting, multiple frequency synthesizers can be used in the same I²C-bus.
The address for the hardware bit setting can be selected by applying voltage to the address setting pin (ADR:pin7).An address is selected according to the set bits.

If the correct address bytes are received, the serial data (SDA) line is "Low" during acknowledgment; when Write Mode is set, the serial data (SDA) line is "Low" during the next acknowledgment if the data byte is programmed.

This IC incorporates a built-in power-on reset circuit for which a detection voltage of approximately 1.4 V has been set. When the Vcc is supplied, a delay or stoppage in a power supply voltage close to this detection voltage may cause the power-on reset circuit to malfunction, in which case there is a risk that some data may not be received even after the recommended voltage has been restored.

A) Write Mode (Setting Command)

When Write Mode is set so that the different types of information may be received, byte1 is used to specify the address data; byte2 and byte3, the frequency data; byte4, function setting data such as the divider ratio setting; and byte 5, the output port data (bandswitch data).
Data are latched and transferred at the end of byte 3,byte 4 and byte 5.
Byte 2 and byte 3 are latched and transferred is done with a two bytes set (byte 2 + byte 3).
Once a correct address is received and acknowledged, the data type is determined by whether the first bit of the next byte is set to [0] or [1]. [0] indicates frequency data, while [1] indicates function setting or output data.
Until the I²C-bus STOP CONDITION is detected, the additional data can be input without transmitting the address data again. (For example: Frequency sweep is possible with additional frequency data.)
If data transmission is aborted, data programmed before the abort are valid.

[[BYTE 1]]

Hardware bit setting of byte1 is possible using the address data.
The hardware bit is set with the voltage applied to the address-setting pin (ADR:pin7).

[[BYTE 2 , BYTE 3]]

Byte 2 , byte 3 are stored in the 15-bit shift register with counter data for the frequency setting, and control the 15-bit programmable counter ratio.
The program frequency can be calculated in the following formula :

$fosc = fr \times N$

fosc : Program frequency
fr : Phase comparator reference frequency (Step frequency)
N : Counter total divider ratio

fr is calculated using the crystal oscillator and the reference frequency divider ratio set in byte 4 (control byte).
(fr = crystal oscillator frequency / reference divider ratio)
The reference frequency divider ratio can be set to 1/64 , 1/80, 1/24 and 1/28.
When using a 4MHz crystal oscillator, fr=62.5kHz , 50.0kHz , 166.67kHz and 142.86kHz.
The step frequency are 62.5kHz , 50.0kHz , 166.67kHz and 142.86kHz.

[[BYTE 4]]

Byte4 is a control byte used to set the different function. Bit 2 (CP) and controls the output current of the charge-pump circuit. When bit 2 is set to [0] : the output current is set to $\pm$145uA ; when it is set to [1], it is $\pm$210uA.
Bit 3 (T2), bit 4 (T1) and bit 5 (T0) are used to set the phase comparator reference signal output and counter divider output in test mode. (For details of test mode, see the test mode setting table.)
Bit 6 (Rsa) and bit 7 (Rsb) are used to set the crystal reference frequency divider ratio.(For details of the crystal reference frequency divider ratio, see the table for crystal reference frequency divider ratios.)
Bit 8 (OS) is used to set the charge-pump driver amplifier output setting. When bit 8 is set to [0] the output is ON (the normal setting used); when it is set to [1] the output is OFF (charge pump is sink mode).

[[BYTE 5]]

Byte 5 is used to set the test mode and control the output ports (VHF-L, VHF-H, UHF and FMT).
When an output port is set to [0], it is OFF; when it is set to [1], it is ON.
As setting the band switch data, It can be control change of VHF or UHF, band switch driver.

No.	Band SW Data (setting data)				Mixer		Oscillator			Band Drive Port			
-	B4	B3	B2	B1	VHF	UHF	VL	VH	U	VL	VH	U	FMT
1	0	0	0	0	×	×	×	×	×	×	×	×	×
2	0	0	0	1	○	×	○	×	×	○	×	×	×
3	0	0	1	0	○	×	×	○	×	×	○	×	×
4	0	1	0	0	×	○	×	×	○	×	×	○	×
5	1	0	0	0	×	○	×	×	○	×	×	○	×
6	0	1	0	1	○	×	○	×	×	○	×	×	○
7	1	0	0	1	○	×	○	×	×	○	×	×	○

○: Operation
×: Not operation

When It Is setting the band sw data excepts from No.1 to No.7, this Is not operating mixer, oscillator and band switch driver.

Please give the following currents to band switch driver respectively as the maximum value. If the band switch driver operates 2-port 'ON'(when setting data Is No.6 and No.7) , total band driver curent Is below 25mA.

VHF-L band switch driver (pin14) output current; 20mA(maximum)
VHF-H band switch driver (pin15) output current; 20mA(maximum)
UHF band switch driver (pin21) output current; 15mA(maximum)
VHF-L and FMT band switch driver (pin13 and 14) output total current; 25mA(maximum)

B) Read Mode (Status Request)

When Read Mode is set, power-on reset operation status and phase comparator lock detector output status are output to the master device.
Bit 1 (POR) indicates the power-on reset operation status. When the power supply of Vcc1 stops, this bit is set to [1]. The conditions for reset to [0] are that voltage supplied to Vcc1 is 3V or higher, that transmission is requested in Read Mode, and that the status is output. (When Vcc1 is turned on, bit1 is also set to [1].)
Bit 2 (FL) indicates the phase comparator lock status. When this is locked, [1] is output; when it is unlocked, [0] is output.

DATA FORMAT

A) WRITE MODE

		MSB							LSB	
1	Address Byte	1	1	0	0	0	MA1	MA0	R/W=0	ACK
2	Divider Byte 1	0	N14	N13	N12	N11	N10	N9	N8	ACK
3	Divider Byte 2	N7	N6	N5	N4	N3	N2	N1	N0	ACK(L)
4	Control Byte	1	CP	T2	T1	T0	Rsa	Rsb	OS	ACK(L)
5	Band SW Byte	×	×	×	×	B4	B3	B2	B1	ACK(L)

× :DON'T CARE
ACK :Acknowledged
(L) :Latch and transfer timing

B) READ MODE

		MSB							LSB	
1	Address Byte	1	1	0	0	0	MA1	MA0	R/W=1	ACK
2	Status Byte	POR	FL	1	1	1	1	1	1	-

ACK :Acknowledged

DATA SPECIFICATIONS

●MA1,MA0 : programmable hardware address bits

MA1	MA0	ADDRESS PIN APPLIED VOLTAGE
0	0	0 to 0.1Vcc1
0	1	OPEN or 0.2Vcc1 to 0.3Vcc1
1	0	0.4Vcc1 to 0.6Vcc1
1	1	0.9Vcc1 to Vcc1

●N14 – N0 : programmable counter data

● CP : charge pump output current setting
[0] : ± 145uA(typ.)
[1] : ± 210uA(typ)

●T2,T1,T0 : test mode setting bits

CHARACTERISTIC		T2	T1	T0	NOTE
Normal operation		0	0	×	-
Charge-pump	OFF	0	1	×	Charge pump is OFF (check output : NF)
	SINK	1	1	0	Only charge pump sink current is ON (check output : NF)
	SOURCE	1	1	1	Only charge pump source current is ON (check output : NF)
Reference signal output		1	0	0	Reference signal output (check output : pin21)
1/2 counter divider output		1	0	1	1/2 counter output (check output : pin15)

note9: Testing of the counter driver output requires the input of programmable counter data.

●Rsa,Rsb : Reference frequency divider ratio select bit.

Rsa	Rsb	DIVIDER RATIO	STEP FREQUENCY
0	0	1/80	50.0kHz
0	1	1/28	142.86kHz
1	0	1/24	166.67kHz
1	1	1/64	62.5kHz

●OS : tuning amplifier control bit
[0] : tuning amplifier ON (normal operation)
[1] : tuning amplifier OFF (charge pump is sink mode)

●POR : power on reset flag
[0] : normal operation
[1] : reset operation

●FL : lock detect flag
[0] : unlocked
[1] : locked

●× : don't care

-EXAMPLE OF BUS DATA TRANSMITTER-

S : Start
ADR : Address Byte
DIV1 : Divider Byte 1 (frequency data)
DIV2 : Divider Byte 2 (frequency data)
CONT : Control Byte
BAND : Band SW Byte
A : Acknowledge
P : Stop

[1] Transmitter - 1

S	ADR	A	DIV1	A	DIV2	A	CONT	A	BAND	A	P

[2] Transmitter - 2

S	ADR	A	CONT	A	BAND	A	DIV1	A	DIV2	A	P

[3] Transmitter – 3 (This can be applies if control data and bandswitch data have already been programmed.)

S	ADR	A	DIV1	A	DIV2	A	P

[4] Transmitter – 4 (This can be applies if frequency data have already been programmed.)

S	ADR	A	CONT	A	BAND	A	P

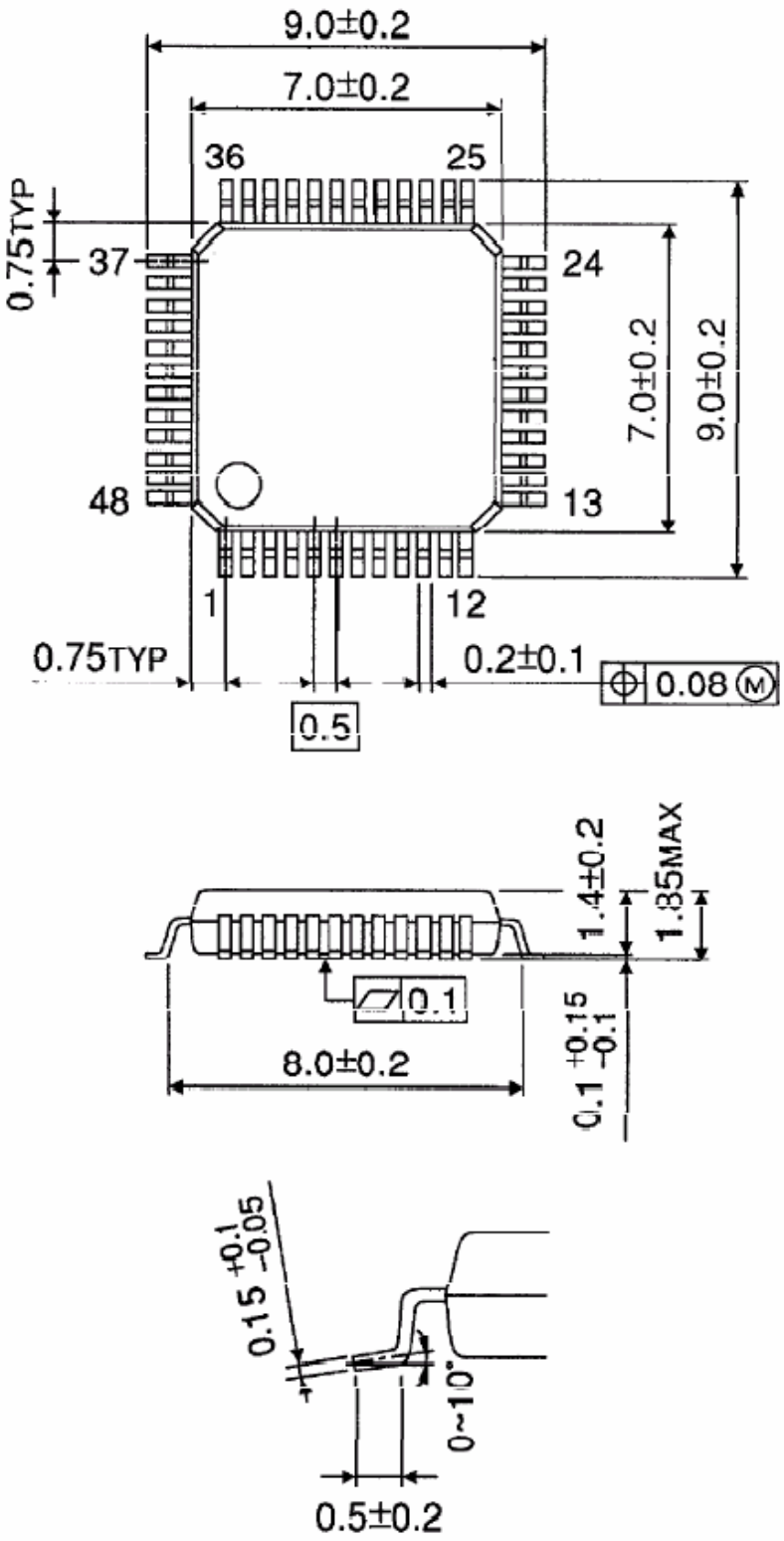
[5] Transmitter – 5 (This can be applies if frequency data and bandswitch data have already been programmed.)

S	ADR	A	CONT	A	P

Until the I²C-bus STOP Condition is detected, it is possible to input the additional data without transmitting the address data again. (For example: Frequency sweep is possible with additional frequency data.)
If data transmission is aborted, data programmed before the abort are valid.

OUTLINE DRAWING

LQFP48-P-0707-0.50 Unit : mm



Weight: 0.17g (typ.)

HANDLING PRECAUTIONS

1. The device should not be inserted into or removed from the test apparatus while the voltage is being applied; otherwise breakdown or deterioration in performance of the device may result.
   Also, avoid any abrupt increasing or decreasing of the voltage.
   Overshoot or chattering of the power supply may cause the IC to be degraded.
   To avoid this problem, equip the power supply line with filters.

2. The peripheral circuits described in this datasheet are given only as system examples for evaluating the performance of the device. Toshiba neither recommend the configuration or related values of the peripheral circuits nor intend to manufacture such application systems in large quantities.
   Please note that the high-frequency characteristics of the device may vary depending on the external components, mounting method and other factors relating to the application design. Therefore it is the responsibility of users incorporating the device into their designs to evaluate the characteristics of application circuits.
   Toshiba only guarantee the quality and characteristics of the device as described in this datasheet and do not assume any responsibility for the customer's application design.

3. In order better to understand the quality and reliability of Toshiba semiconductor products and to incorporate them into designs in an appropriate manner, please refer to the latest Semiconductor Reliability Handbook (Integrated Circuits) published by Toshiba Semiconductor Company.

   The handbook can also be viewed online at " http://www.semicon.toshiba.co.jp/ "

Solderability

Regarding solderability, the following conditions have been confirmed.

(1) Use of Sn-63Pb solder bath
- Solder bath temperature = 230°C
- Dipping time = 5 seconds
- The number Number of times = once
- Use of R-type flux

(2) Use of Sn-3.0Ag-0.5Cu solder bath
- Solder bath temperature = 245°C
- Dipping time = 5 seconds
- Number of times = once
- Use of R-type flux

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