TOSHIBA Transistor Silicon NPN / PNP Epitaxial Type (PCT Process)

TPCP8901

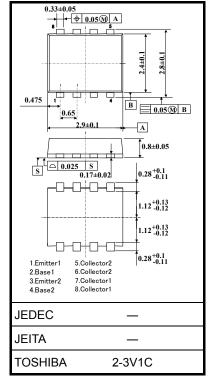
Portable Equipment Applications Switching Applications

- Small footprint due to small and thin package
- High DC current gain : PNP
 $h_{FE} = 200$ to 500 ($I_C = -0.1$ A)

 :NPN
 $h_{FE} = 400$ to 1000 ($I_C = 0.1$ A)
- Low collector-emitter saturation : PNP VCE (sat) = -0.20 V (max)
 - : NPN V_{CE} (sat) = 0.17 V (max)
- High-speed switching : PNP $t_f = 70 \text{ ns} (typ.)$
 - : NPN $t_f = 85 \text{ ns (typ.)}$

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating		Unit	
		Symbol	PNP	NPN	Onit	
Collector-base voltage		V _{CBO}	-50	100	V	
Collector-emitter voltage		V _{CEO}	-50	50	V	
Emitter-base voltage		V _{EBO}	-7	7	V	
Collector current	DC (Note 1)	Ι _C	-0.8	1.0	А	
	Pulse (Note 1)	I _{CP}	-5.0	5.0	A	
Base current		Ι _Β	-100	100	mA	
Collector power dissipation (t = 10s)	Single-device operation		1.48			
	Single-device value at dual operation	P _C (Note 2)	0.8	30	W	
Collector power dissipation (DC)	Single-device operation		0.83		W	
	Single-device value at dual operation	P _C (Note 2)				
Junction temperature		Tj	150		°C	
Storage temperature range		T _{stg}	–55 to 150		°C	



Weight: 0.017 g (typ.)

Note 1: Please use devices on condition that the junction temperature is below 150°C. Icp= \pm 5A (@ t \leq 100 μ s)

Note 2: Mounted on FR4 board (glass epoxy, 1.6 mm thick, Cu area: 645 mm²)

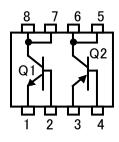
Note 3: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Unit: mm

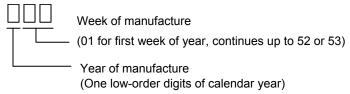
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Figure 1. Circuit configuration (top view)



Note 4: \bullet on lower left on the marking indicates Pin 1.

※ Weekly code: (Three digits)



Electrical Characteristics (Ta = 25°C)

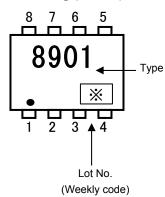
PNP

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Collector cut-off current		I _{CBO}	$V_{CB}=-50~V,~I_{E}=0$	_		-100	nA
Emitter cut-off current		I _{EBO}	$V_{EB} = -7 \text{ V}, \text{ I}_{C} = 0$	_	_	-100	nA
Collector-emitter breakdown voltage		V (BR) CEO	$I_{C} = -10 \text{ mA}, I_{B} = 0$	-50	_	_	V
DC current gain		h _{FE} (1)	$V_{CE} = -2 V, I_C = -0.1 A$	200	_	500	
		h _{FE} (2)	$V_{CE} = -2 \text{ V}, \text{ I}_{C} = -0.3 \text{ A}$	125	_	_	
Collector-emitter saturation voltage		V _{CE (sat)}	$I_{C} = -0.3 \text{ A}, I_{B} = -0.01 \text{ A}$	_	_	-0.20	V
Base-emitter saturation voltage		V _{BE (sat)}	$I_{C} = -0.3 \text{ A}, I_{B} = -0.01 \text{ A}$	_	_	-1.10	V
Collector output capacitance		C _{ob}	$V_{CB} = -10 \text{ V}, I_E = 0, f = 1 \text{MHz}$	_	8	_	pF
Switching time	Rise time	tr	See Figure 3 circuit diagram $V_{CC} \simeq -30 \text{ V}, \text{ R}_L = 100 \Omega$ $-I_{B1} = I_{B2} = -10 \text{ mA}$	_	60	_	ns
	Storage time	t _{stg}		_	280	_	
	Fall time	t _f		_	70	_	

NPN

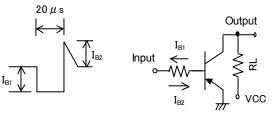
Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Collector cut-off current		I _{CBO}	$V_{CB} = 100 \text{ V}, \text{ I}_{E} = 0$			100	nA
Emitter cut-off current		I _{EBO}	$V_{EB}=7~V,~I_C=0$	_	_	100	nA
Collector-emitter bre	eakdown voltage	V (BR) CEO	$I_{C} = 10 \text{ mA}, I_{B} = 0$	50	_	_	V
DC current gain		h _{FE} (1)	$V_{CE} = 2 V, I_C = 0.1 A$	400	_	1000	
		h _{FE} (2)	$V_{CE} = 2 V, I_C = 0.3 A$	200	_	_	
Collector-emitter saturation voltage		V _{CE (sat)}	$I_C = 300 \text{ mA}, I_B = 6 \text{ mA}$	_	_	0.17	V
Base-emitter saturat	tion voltage	V _{BE (sat)}	$I_C = 300 \text{ mA}, I_B = 6 \text{ mA}$	_	_	1.10	V
Collector output cap	acitance	C _{ob}	$V_{CB} = 10 \text{ V}, I_E = 0, f = 1 \text{MHz}$	_	5	_	pF
Switching time	Rise time	tr	See Figure 4 circuit diagram $V_{CC} \simeq 30 \text{ V}, \text{ R}_L = 100 \Omega$ $I_{B1} = -I_{B2} = 10 \text{ mA}$	_	35	_	ns
	Storage time	t _{stg}			680	_	
	Fall time	t _f			85	_	

Figure 2. Marking (Note 4)



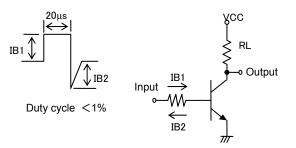
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Figure 3. Switching Time Test Circuit & Timing Chart



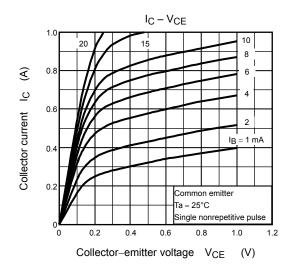
Duty cycle <1%

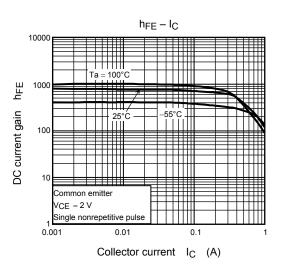
Figure 4. Switching Time Test Circuit & Timing Chart

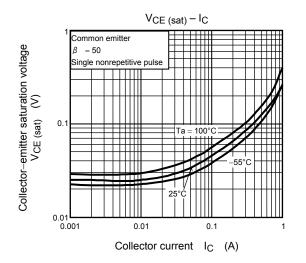


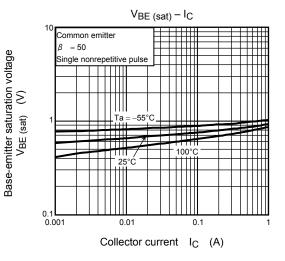
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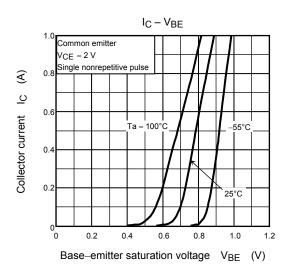
NPN



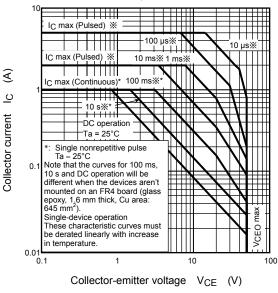






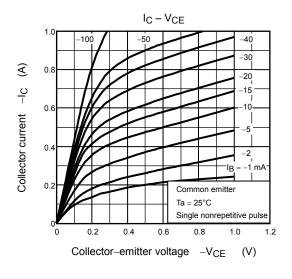


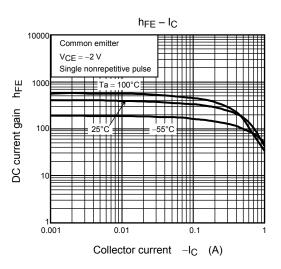
Safe Operation Area

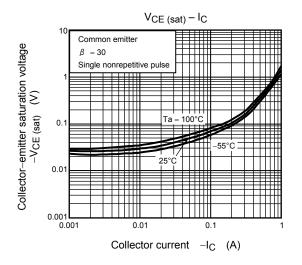


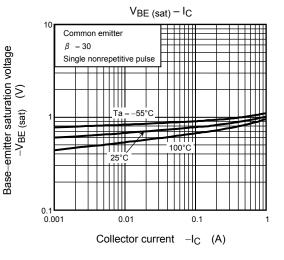
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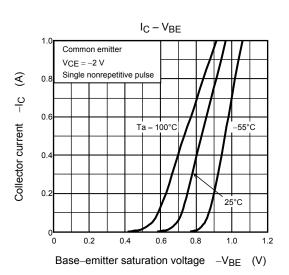
PNP



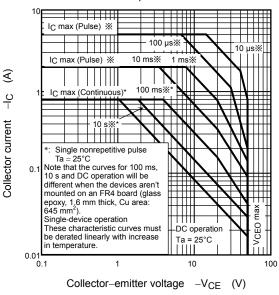






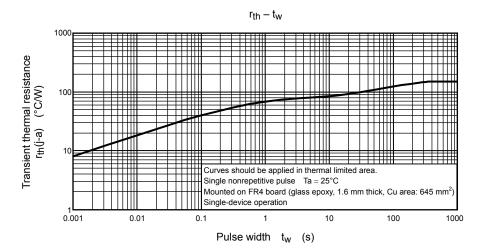


Safe operation area



TOSHIBA

Common



Permissible Power Dissipation for Simultaneous Operation 1.0 DC operation Permissible power dissipation for Q2 $$P_{\rm C}$$ (W) Ta = 25°C Mounted on an FR4 board glass epoxy 0.8 1.6 mm thick, Cu area: 645 mm²) 0.6 0.4 0.2 0 L 0 0.2 0.6 0.4 0.8 1.0 Permissible power dissipation for Q1 Pc (W) Collector power dissipation at the single-device

Collector power dissipation at the single-device value at dual operation is 0.48W.

operation is 0.83W.

Collector power dissipation at the dual operation is set to $0.96 \ensuremath{W}.$

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20070701-EN

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