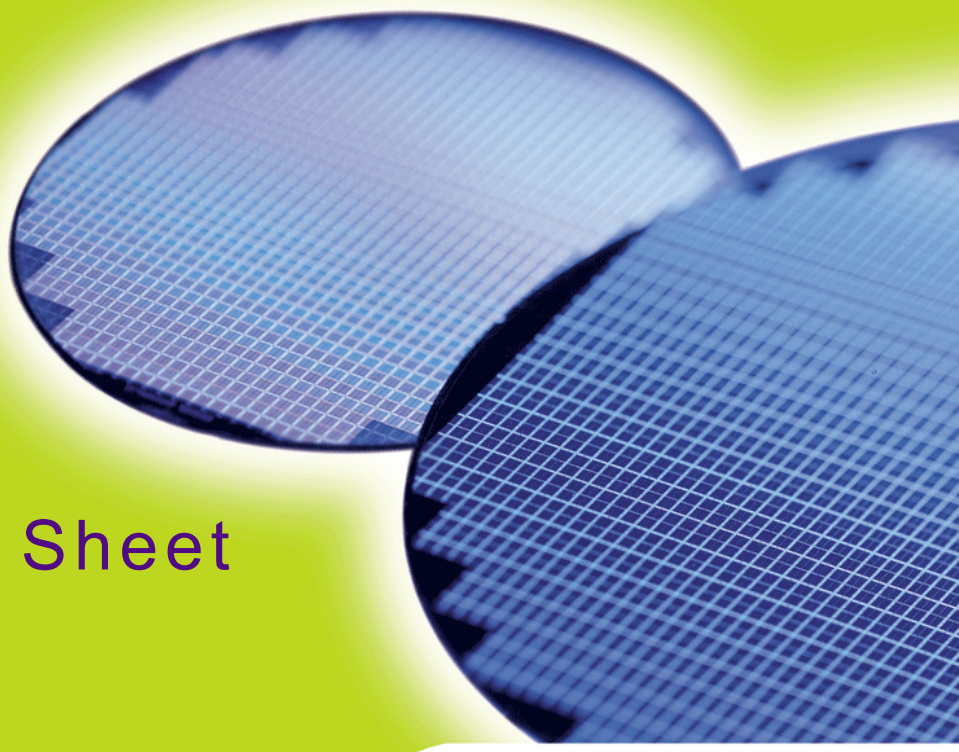
August 2007

HYB18L512320BF-7.5
HYE18L512320BF-7.5

DRAMs for Mobile Applications
512-Mbit SDR Mobile-RAM



Internet Data Sheet

Rev.1.22

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HY[B/E]18L512320BF-7.5 Internet Data Sheet	
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all	Editorial change.
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1 Overview

1.1 Features

- 4 banks × 4 Mbit × 32 organization (dual-die)
- Fully synchronous to positive clock edge
- Four internal banks for concurrent operation
- Programmable CAS latency: 2, 3
- Programmable burst length: 1, 2, 4, 8 or full page
- Programmable wrap sequence: sequential or interleaved
- Programmable drive strength: full, 1/2, 1/4 and 1/8
- Auto refresh and self refresh modes
- Refresh cycles:
  - 8192 refresh cycles / 64 ms
- Auto precharge
- Commercial (-0°C to +70°C) and Extended (-25°C to +85°C) operating temperature range
- Package:
  - Dual-Die 90-ball PG-TFBGA package (13.0 × 8.0 × 1.2 mm)
- RoHS Compliant Products[1)]

Power Saving Features

- Low supply voltages: V_{DD} = 1.70 V to 1.95 V, V_{DDQ} = 1.70 V to 1.95 V
- Optimized self refresh (I_{DD6}) and standby currents (I_{DD2} / I_{DD3})
- Programmable Partial Array Self Refresh (PASR)
- Temperature Compensated Self-Refresh (TCSR), controlled by on-chip temperature sensor
- Power-Down and Deep Power Down modes

TABLE 1
Performance

Part Number Speed Code		- 7.5	Unit
Speed Grade		133	MHz
Access Time (t_{ACmax})	CL = 2 or 3	6.5	ns
Clock Cycle Time (t_{CKmin})	CL = 3	7.5	ns
	CL = 2	9.5	ns

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

TABLE 2
Memory Addressing Scheme

Item	Addresses
Banks	BA0, BA1
Rows	A0 - A12
Columns	A0 - A8

green Product

TABLE 3
Ordering Information

Type[1)]	Package	Description
Standard Temperature Range		
HYB18L512320BF-7.5	PG-TFBGA-90-3	133 MHz 4 Banks × 4 Mbit × 32 LP-SDRAM
Extended Temperature Range		
HYE18L512320BF-7.5	PG-TFBGA-90-3	133 MHz 4 Banks × 4 Mbit × 32 LP-SDRAM

1) HY[B/E]: Designator for memory products (HYB: Standard temp range, HYE: extended temp. range)
18L: 1.8 V Mobile-RAM
512: 512 MBit density
32: 32 bit interface width
B: die revision
F: green product
-7.5: speed grade(s): min. clock cycle time

1.2 Pin Configuration

FIGURE 1
Standard Ballout 256-Mbit Mobile-RAM (Top View x32)

1	2	3		7	8	9
DQ26	DQ24	V_{SS}	A	V_{DD}	DQ23	DQ21
DQ28	V_{DDQ}	V_{SSQ}	B	V_{DDQ}	V_{SSQ}	DQ19
V_{SSQ}	DQ27	DQ25	C	DQ22	DQ20	V_{DDQ}
V_{SSQ}	DQ29	DQ30	D	DQ17	DQ18	V_{DDQ}
V_{DDQ}	DQ31	NC	E	NC	DQ16	V_{SSQ}
V_{SS}	DQM3	A3	F	A2	DQM2	V_{DD}
A4	A5	A6	G	A10/AP	A0	A1
A7	A8	A12	H	NC	BA1	A11
CLK	CKE	A9	J	BA0	$\overline{CS}$	$\overline{RAS}$
DQM1	NC	NC	K	$\overline{CAS}$	$\overline{WE}$	DQM0
V_{DDQ}	DQ8	V_{SS}	L	V_{DD}	DQ7	V_{SSQ}
V_{SSQ}	DQ10	DQ9	M	DQ6	DQ5	V_{DDQ}
V_{SSQ}	DQ12	DQ14	N	DQ1	DQ3	V_{DDQ}
DQ11	V_{DDQ}	V_{SSQ}	P	V_{DDQ}	V_{SSQ}	DQ4
DQ13	DQ15	V_{SS}	R	V_{DD}	DQ0	DQ2

1.3 Description

The HY[B/E]18L512320BF is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM.

The HY[B/E]18L512320BF achieves high speed data transfer rates by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to the system clock. Read and write accesses are burst-oriented; accesses start at a selected location and continue for a programmed number of locations (1, 2, 4, 8 or full page) in a programmed sequence.

The device operation is fully synchronous: all inputs are registered at the positive edge of CLK.

The HY[B/E]18L512320BF is especially designed for mobile applications. It operates from a 1.8 V power supply. Power consumption in self refresh mode is drastically reduced by an On-Chip Temperature Sensor (OCTS); it can further be reduced by using the programmable Partial Array Self Refresh (PASR).

A conventional data-retaining Power Down (PD) mode is available as well as a non-data-retaining Deep Power Down (DPD) mode.

The HY[B/E]18L512320BF is housed in a 90-ball PG-VFBGA (x32) package. It is available in Standard (-0 °C to +70 °C) and Extended (-25 °C to +85 °C) temperature ranges.

1.4 Pin Definition and Description

TABLE 4
Pin Description

Ball	Type	Detailed Function
CLK	Input	**Clock:** all inputs are sampled on the positive edge of CLK.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals, device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), ACTIVE POWER-DOWN (row active in any bank) or SUSPEND (access in progress). CKE is synchronous for POWER-DOWN entry and exit and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit. Input buffers, excluding CLK and CKE are disabled during power-down. Input buffers, excluding CKE are disabled during SELF REFRESH.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external bank selection on systems with multiple memory banks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DQ0 - DQ31	I/O	**Data Inputs/Output:** Bi-directional data bus (32 bit)
DQM0 - DQM3	Input	**Input/Output Mask:** input mask signal for WRITE cycles and output enable for READ cycles. For WRITEs, DQM acts as a data mask when HIGH. For READs, DQM acts as an output enable and places the output buffers in High-Z state when HIGH (two clocks latency). DQM0 corresponds to the data on DQ0 - DQ7; DQM1 to the data on DQ8 - DQ15; DQM2 to the data on DQ16 - DQ23; DQM3 to the data on DQ24 - DQ31.
BA0, BA1	Input	**Bank Address Inputs:** BA0 and BA1 define to which bank an ACTIVATE, READ, WRITE or PRECHARGE command is being applied. BA0, BA1 also determine which mode register is to be loaded during a MODE REGISTER SET command (MRS or EMRS).
A0 - A12	Input	**Address Inputs:** defines the row address during an ACTIVE command cycle. A0 - A8 define the column address during a READ or WRITE command cycle. In addition, A10 (= AP) controls Auto Precharge operation at the end of the burst read or write cycle. During a PRECHARGE command, A10 (= AP) in conjunction with BA0, BA1 controls which bank(s) are to be precharged: if A10 is HIGH, all four banks will be precharged regardless of the state of BA0 and BA1; if A10 is LOW, BA0, BA1 define the bank to be precharged. During MODE REGISTER SET commands, the address inputs hold the op-code to be loaded.
V_{DDQ}	Supply	**I/O Power Supply:** Isolated power for DQ output buffers for improved noise immunity: V_{DDQ} = 1.70 V to 1.95 V
V_{SSQ}	Supply	**I/O Ground**
V_{DD}	Supply	**Power Supply:** Power for the core logic and input buffers, V_{DD} = 1.70 V to 1.95 V
V_{SS}	Supply	**Ground**
N.C.	–	**No Connect**

2 Functional Description

The 512-Mbit Mobile-RAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM.

READ and WRITE accesses to the Mobile-RAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the banks, A0 - A12 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the Mobile-RAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command description and device operation.

2.1 Register Definition

2.1.1 Mode Register

The Mode Register is used to define the specific mode of operation of the Mobile-RAM. This definition includes the selection of a burst length (bits A0-A2), a burst type (bit A3), a CAS latency (bits A4-A6), and a write burst mode (bit A9). The Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power.

The Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements results in unspecified operation.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

MRMode Register Definition(BA[1:0] = 00_B)

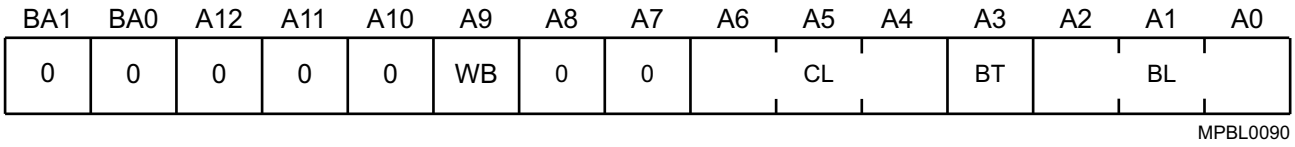


TABLE 5
Mode Register Definition (BA[1:0] = 00_B)

Field	Bits	Type	Description
WB	9	w	**Write Burst Mode** 0 Burst Write 1 Single Write
CL	[6:4]	w	**CAS Latency** 010 2 011 3 *Note: All other bit combinations are RESERVED.*

Field	Bits	Type	Description
BT	3	w	**Burst Type** 0 Sequential 1 Interleaved
BL	[2:0]	w	**Burst Length** 000 1 001 2 010 4 011 8 111 full page (Sequential burst type only) *Note: All other bit combinations are RESERVED.*

2.2 Extended Mode Register

The Extended Mode Register controls additional low power features of the device. These include the Partial Array Self Refresh (PASR, bits A0-A2)), the Temperature Compensated Self Refresh (TCSR, bits A3-A4)) and the drive strength selection for the DQs (bits A5-A6). The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 1) and will retain the stored information until it is programmed again or the device loses power.

The Extended Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements result in unspecified operation.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

EMR
Extended Mode Register(BA[1:0] = 10_B)

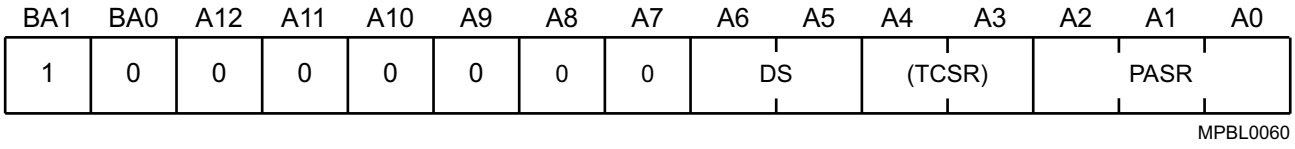


TABLE 6
Extended Mode Register Definition (BA[1:0] = 10_B)

Field	Bits	Type	Description
DS	[6:5]	w	**Selectable Drive Strength** 00_B **DS** Full Drive Strength 01_B **DS** Half Drive Strength *Note: All other bit combinations are RESERVED.*
TCSR	[4:3]	w	**Temperature Compensated Self Refresh** XX Superseded by on-chip temperature sensor (see text)
PASR	[2:0]	w	**Partial Array Self Refresh** 000_B **PASR** all banks (default) 001_B **PASR** 1/2 array (BA1 = 0) 010_B **PASR** 1/4 array (BA1 = BA0 = 0) 101_B **PASR** 1/8 array (BA1 = BA0 = RA12 = 0) 110_B **PASR** 1/16 array (BA1 = BA0 = RA12 = RA11 = 0) *Note: All other bit combinations are RESERVED.*

2.3 Function Truth Tables

TABLE 7
Current State Bank n - Command to Bank n

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command / Action	Notes
Any	H	X	X	X	DESELECT (NOP / continue previous operation)	1)2)3)4)5)6)
	L	H	H	H	NO OPERATION (NOP / continue previous operation)	1)2)3)4)5)6)
Idle	L	L	H	H	ACTIVE (select and activate row)	1)2)3)4)5)6)
	L	L	L	H	AUTO REFRESH	1)2)3)4)5)6)7)
	L	L	L	L	MODE REGISTER SET	1)2)3)4)5)6)7)
	L	L	H	L	PRECHARGE	1)2)3)4)5)6)8)
Row Active	L	H	L	H	READ (select column and start READ burst)	1)2)3)4)5)6)9)
	L	H	L	L	WRITE (select column and start WRITE burst)	1)2)3)4)5)6)9)
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	1)2)3)4)5)6)10)
Read (Auto-Precharge Disabled)	L	H	L	H	READ (select column and start new READ burst)	1)2)3)4)5)6)9)
	L	H	L	L	WRITE (select column and start new WRITE burst)	1)2)3)4)5)6)9)
	L	L	H	L	PRECHARGE (truncate READ burst, start precharge)	1)2)3)4)5)6)10)
	L	H	H	L	BURST TERMINATE	1)2)3)4)5)6)11)
Write (Auto-Precharge Disabled)	L	H	L	H	READ (select column and start READ burst)	1)2)3)4)5)6)9)
	L	H	L	L	WRITE (select column and start WRITE burst)	1)2)3)4)5)6)9)
	L	L	H	L	PRECHARGE (truncate WRITE burst, start precharge)	1)2)3)4)5)6)10)
	L	H	H	L	BURST TERMINATE	1)2)3)4)5)6)11)

1) This table applies when CKEn-1 was HIGH and CKEn is HIGH and after t_{RC} has been met (if the previous state was self refresh).
2) This table is bank-specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3) Current state definitions:Idle:The bank has been precharged, and t_{RP} has been met.Row Active:A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.Read:A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.Write:A WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4) The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and according to **Table 8**.Precharging:Starts with registration of a PRECHARGE command and ends when t_{RP} is met. Once t_{RP} is met, the bank is in the “idle” state.Row Activating:Starts with registration of an ACTIVE command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank is in the “row active” state.Read with AP Enabled:Starts with registration of a READ command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.Write with AP Enabled:Starts with registration of a WRITE command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.
5) The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states. Refreshing:Starts with registration of an AUTO REFRESH command and ends when t_{RC} is met. Once t_{RC} ismet, the SDRAM is in the “all banks idle” state.Accessing MR:Starts with registration of a MODE REGISTER SET command and ends when t_{MRD} has beenmet. Once t_{MRD} is met, the SDRAM is in the “all banks idle” state.Precharging All:Starts with registration of a PRECHARGE ALL command and ends when t_{RP} is met. Once t_{RP} is met, all banks are in the idle state.
6) All states and sequences not shown are illegal or reserved.
7) Not bank-specific; requires that all banks are idle and no bursts are in progress.
8) Same as NOP command in that state.
9) READs or WRITEs listed in the Command/Action column include READs or WRITEs with Auto Precharge enabled and READs or WRITEs with Auto Precharge disabled.

10) May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
11) Not bank-specific; BURST TERMINATE affects the most recent READ or WRITE burst, regardless of bank.

TABLE 8
Current State Bank n - Command to Bank m (different bank)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command / Action	Notes
Any	H	X	X	X	DESELECT (NOP / continue previous operation)	1)2)3)4)5)6)
	L	H	H	H	NO OPERATION (NOP / continue previous operation)	1)2)3)4)5)6)
Idle	X	X	X	X	Any command otherwise allowed to bank n	1)2)3)4)5)6)
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	1)2)3)4)5)6)
	L	H	L	H	READ (select column and start READ burst)	1)2)3)4)5)6)7)
	L	H	L	L	WRITE (select column and start WRITE burst)	1)2)3)4)5)6)7)
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	1)2)3)4)5)6)
Read (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	1)2)3)4)5)6)
	L	H	L	H	READ (select column and start READ burst)	1)2)3)4)5)6)7)
	L	H	L	L	WRITE (select column and start WRITE burst)	1)2)3)4)5)6)7)8)
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	1)2)3)4)5)6)
Write (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	1)2)3)4)5)6)
	L	H	L	H	READ (select column and start READ burst)	1)2)3)4)5)6)7)
	L	H	L	L	WRITE (select column and start WRITE burst)	1)2)3)4)5)6)7)
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	1)2)3)4)5)6)
Read(with Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	1)2)3)4)5)6)
	L	H	L	H	READ (select column and start READ burst)	1)2)3)4)5)6)7)9)
	L	H	L	L	WRITE (select column and start WRITE burst)	1)2)3)4)5)6)7)8)9)
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	1)2)3)4)5)6)
Write(with Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	1)2)3)4)5)6)
	L	H	L	H	READ (select column and start READ burst)	1)2)3)4)5)6)7)9)
	L	H	L	L	WRITE (select column and start WRITE burst)	1)2)3)4)5)6)7)9)
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	1)2)3)4)5)6)

1) This table applies when CKEn-1 was HIGH and CKEn is HIGH and after t_{RC} has been met (if the previous state was Self Refresh).
2) This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3) Current state definitions:Idle:The bank has been precharged, and t_{RP} has been met.Row Active:A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.Read:A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated orbeen terminated.Write:A WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.Read with AP Enabled:Starts with registration of a READ command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.Write with AP Enabled:Starts with registration of a WRITE command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.
4) AUTO REFRESH, SELF REFRESH and MODE REGISTER SET commands may only be issued when all banks are idle.
5) A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6) All states and sequences not shown are illegal or reserved.
7) READs or WRITEs listed in the Command/Action column include READs or WRITEs with Auto Precharge enabled and READs or WRITEs with Auto Precharge disabled.
8) Requires appropriate DQM masking.

9) Concurrent Auto Precharge: bank n will start precharging when its burst has been interrupted by a READ or WRITE command to bank m.

TABLE 9
Truth Table - CKE

CKEn-1	CKEn	Current State	Command	Action	Notes
L	L	Power Down	X	Maintain Power Down	1)2)3)4)
		Self Refresh	X	Maintain Self Refresh	1)2)3)4)
		Clock Suspend	X	Maintain Clock Suspend	1)2)3)4)
		Deep Power Down	X	Maintain Deep Power Down	1)2)3)4)
L	H	Power Down	DESELECT or NOP	Exit Power Down	1)2)3)4)
		Self Refresh	DESELECT or NOP	Exit Self Refresh	1)2)3)4)5)
		Clock Suspend	X	Exit Clock Suspend	1)2)3)4)
		Deep Power Down	X	Exit Deep Power Down	1)2)3)4)6)
H	L	All Banks Idle	DESELECT or NOP	Enter Precharge Power Down	1)2)3)4)
		Bank(s) Active	DESELECT or NOP	Enter Active Power Down	1)2)3)4)
		All Banks Idle	AUTO REFRESH	Enter Self Refresh	1)2)3)4)
		Read / Write burst	(valid)	Enter Clock Suspend	1)2)3)4)
H	H	See **Table 7** and **Table 8**			1)2)3)4)

1) CKEn is the logic state of CKE at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.
2) Current state is the state immediately prior to clock edge n.
3) COMMAND n is the command registered at clock edge n; ACTION n is a result of COMMAND n.
4) All states and sequences not shown are illegal or reserved.
5) DESELECT or NOP commands should be issued on any clock edges occurring during t_{RC} period.
6) Exit from DEEP POWER DOWN requires the same command sequence as for power-up initialization.

3 Electrical Characteristics

3.1 Operating Conditions

TABLE 10
Absolute Maximum Ratings

Parameter		Symbol	Values		Unit
			Min.	Max.	
Power Supply Voltage		V_{DD}	-0.3	2.7	V
Power Supply Voltage for Output Buffer		V_{DDQ}	-0.3	2.7	V
Input Voltage		V_{IN}	-0.3	V_{DDQ} + 0.3	V
Output Voltage		V_{OUT}	-0.3	V_{DDQ} + 0.3	V
Operation Case Temperature	Commercial	T_C	0	+70	°C
	Extended		-25	+85	°C
Storage Temperature		T_{STG}	-55	+150	°C
Power Dissipation		P_D	–	1.0	W
Short Circuit Output Current		I_{OUT}	–	50	mA

Attention: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

TABLE 11
Pin Capacitances

Parameter	Symbol	Values		Unit	Notes[1)2)]
		Min.	Max.		
Input capacitance: CLK	C_{I1}	3.0	6.0	pF	
Input capacitance: all other input	C_{I2}	3.0	6.0	pF	
Input/Output capacitance: DQ	C_{IO}	3.0	5.0	pF	

1) These values are not subject to production test but verified by device characterization.
2) Input capacitance is measured according to JEP147 with V_{DD}, V_{DDQ} applied and all other pins (except the pin under test) floating. DQ's should be in high impedance state.

TABLE 12
Electrical Characteristics

Parameter	Symbol	Values		Unit	Notes[1)]
		Min.	Max.		
Power Supply Voltage	V_{DD}	1.70	1.95	V	–
Power Supply Voltage for DQ Output Buffer	V_{DDQ}	1.70	1.95	V	–
Input high voltage	V_{IH}	0.8 × V_{DDQ}	V_{DDQ} + 0.3	V	2)
Input low voltage	V_{IL}	-0.3	0.3	V	2)
Output high voltage	V_{OH}	V_{DDQ} - 0.2	–	V	–
Output low voltage	V_{OL}	–	0.2	V	–
Input leakage current	I_{IL}	-1.0	1.0	µA	–
Output leakage current	I_{OL}	-1.5	1.5	µA	–

1) 0 °C ≤ T_C ≤ 70 °C (comm.); -25 °C ≤ T_C ≤ 85 °C (ext.); All voltages referenced to V_{SS}. V_{SS} and V_{SSQ} must be at same potential.
2) V_{IH} may overshoot to V_{DD} + 0.8 V for pulse width < 4 ns; V_{IL} may undershoot to -0.8 V for pulse width < 4 ns.Pulse width measured at 50% with amplitude measured between peak voltage and DC reference level.

3.2 AC Characteristics

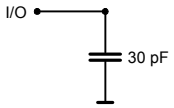
TABLE 13
AC Characteristics

Parameter		Symbol	- 7.5		Unit	Notes[1)2)3)4)]
			Min.	Max.		
Clock cycle time	CL = 2	t_{CK}	9.5	—	ns	—
	CL = 3		7.5	—	ns	
Clock frequency	CL = 2	f_{CK}	—	105	MHz	—
	CL = 3		—	133	MHz	
Access time from CLK		t_{AC}	—	6.5	ns	5)6)
Clock high-level width		t_{CH}	2.5	—	ns	—
Clock low-level width		t_{CL}	2.5	—	ns	—
Address, data and command input setup time		t_{IS}	1.5	—	ns	7)
Address, data and command input hold time		t_{IH}	0.8	—	ns	7)
MODE REGISTER SET command period		t_{MRD}	2	—	t_{CK}	—
DQ low-impedance time from CLK		t_{LZ}	1.0	—	ns	—
DQ high-impedance time from CLK		t_{HZ}	3.0	7.0	ns	—
Data out hold time		t_{OH}	2.5	—	ns	5)6)
DQM to DQ High-Z delay (READ Commands)		t_{DQZ}	—	2	t_{CK}	—
DQM write mask latency		t_{DQW}	0	—	t_{CK}	—
ACTIVE to ACTIVE command period		t_{RC}	67	—	ns	8)
ACTIVE to READ or WRITE delay		t_{RCD}	19	—	ns	8)

Parameter	Symbol	- 7.5		Unit	Notes[1)2)3)4)]
		Min.	Max.		
ACTIVE bank A to ACTIVE bank B delay	t_{RRD}	15	—	ns	8)
ACTIVE to PRECHARGE command period	t_{RAS}	45	100k	ns	8)
WRITE recovery time	t_{WR}	14	—	ns	9)
PRECHARGE command period	t_{RP}	19	—	ns	8)
Refresh period (8192 rows)	t_{REF}	—	64	ms	—
Self refresh exit time	t_{SREX}	1	—	t_{CK}	—

1) 0 °C ≤ T_C ≤ 70 °C (comm.); -25 °C ≤ T_C ≤ 85 °C (ext.); V_{DD} = V_{DDQ} = 1.70 V to 1.95 V;
2) All parameters assumes proper device initialization.
3) AC timing tests measured at 0.9 V.
4) The transition time t_T is measured between V_{IH} and V_{IL}; all AC characteristics assume t_T = 1 ns.
5) Specified t_{AC} and t_{OH} parameters are measured with a 30 pF capacity load only as shown in **Figure 2**.
6) If t_T(CLK) > 1 ns, a value of (t_T/2 - 0.5) ns has to be added to this parameter.
7) If t_T > 1 ns, a value of (t_T - 1) ns has to be added to this parameter.
8) These parameter account for the number of clock cycles and depend on the operating frequency, as follows: no. of clock cycles = specified delay / clock period; round up to next integer.
9) The write recovery time of t_{WR} = 14 ns allows the use of one clock cycle for the write recovery time when f_{CK} ≤ 72 MHz. With f_{CK} > 72 MHz two clock cycles for t_{WR} are mandatory. Infineon Technologies recommends to use two clock cycles for the write recovery time in all applications.

FIGURE 2
Measurement with Reference Load



3.3 Operating Currents

TABLE 14
Maximum Operating Currents

Parameter & Test Conditions	Symbol		Unit	Notes[1]
		- 7.5		
Operating current: one bank: active / read / precharge, BL = 1, $t_{RC} = t_{RCmin}$	I_{DD1}	120	mA	2)3)
Precharge power-down standby current: all banks idle, $\overline{CS} \geq V_{IHmin}$, CKE ≤ V_{ILmax}, inputs changing once every two clock cycles	I_{DD2P}	1.2	mA	2)
Precharge power-down standby current with clock stop: all banks idle, $\overline{CS} \geq V_{IHmin}$, CKE ≤ V_{ILmax}, all inputs stable	I_{DD2PS}	1.0	mA	–
Precharge non power-down standby current: all banks idle, $\overline{CS} \geq V_{IHmin}$, CKE ≥ V_{IHmin}, inputs changing once every two clock cycles	I_{DD2N}	26	mA	2)
Precharge non power-down standby current with clock stop: all banks idle, $\overline{CS} \geq V_{IHmin}$, CKE ≥ V_{IHmin}, all inputs stable	I_{DD2NS}	2.0	mA	–
Active power-down standby current: one bank active, $\overline{CS} \geq V_{IHmin}$, CKE ≤ V_{ILmax}, inputs changing once every two clock cycles	I_{DD3P}	2.0	mA	2)
Active power-down standby current with clock stop: one bank active, $\overline{CS} \geq V_{IHmin}$, CKE ≤ V_{ILmax}, all inputs stable	I_{DD3PS}	1.5	mA	–
Active non power-down standby current: one bank active, $\overline{CS} \geq V_{IHmin}$, CKE ≥ V_{IHmin}, inputs changing once every two clock cycles	I_{DD3N}	30	mA	2)
Active non power-down standby current with clock stop: one bank active, $\overline{CS} \geq V_{IHmin}$, CKE ≥ V_{IHmin}, all inputs stable	I_{DD3NS}	3.0	mA	–
Operating burst read current: all banks active; continuous burst read, inputs changing once every two clock cycles	I_{DD4}	90	mA	2)3)
Auto-Refresh current: $t_{RC} = t_{RCmin}$, “burst refresh”, inputs changing once every two clock cycles	I_{DD5}	180	mA	2)
Self Refresh current:self refresh mode, $\overline{CS} \geq V_{IHmin}$, CKE ≤ V_{ILmax}, all inputs stable	I_{DD6}	See **Table 15**		–
Deep Power Down current	I_{DD7}	50	µA	–

1) 0 °C ≤ T_C ≤ 70 °C (comm.); -25 °C ≤ T_C ≤ 85 °C (ext.); $V_{DD} = V_{DDQ}$ = 1.70 V to 1.95 V;Recommended Operating Conditions unless otherwise noted

2) These values are measured with t_{CK} = 7.5 ns

3) All parameters are measured with no output loads.

TABLE 15
Self Refresh Currents

Parameter & Test Conditions	Max. Temperature	Symbol	Values		Units	Notes[1)2)]
			Typ.	Max.		
Self Refresh Current: Self refresh mode, full array activation(PASR = 000)	85 °C	I_{DD6}	1020	1200	µA	–
	70 °C		680	–		
	45 °C		450	–		
	25 °C		410	–		
Self Refresh Current: Self refresh mode, half array activation(PASR = 001)	85 °C		800	940		
	70 °C		570	–		
	45 °C		400	–		
	25 °C		360	–		
Self Refresh Current: Self refresh mode, quarter array activation(PASR = 010)	85 °C		680	800		
	70 °C		500	–		
	45 °C		370	–		
	25 °C		340	–		

1) 0 °C ≤ T_C ≤ 70 °C (comm.); -25 °C ≤ T_C ≤ 85 °C (ext.); V_{DD} = V_{DDQ} = 1.70 V to 1.95 V

2) The On-Chip Temperature Sensor (OCTS) adjusts the refresh rate in self refresh mode to the component's actual temperature with a much finer resolution than supported by the 4 distinct temperature levels as defined by JEDEC for TCSR. At production test the sensor is calibrated, and IDD6 max. current is measured at 85°C. Typ. values are obtained from device characterization.

3.4 Pullup and Pulldown Characteristics

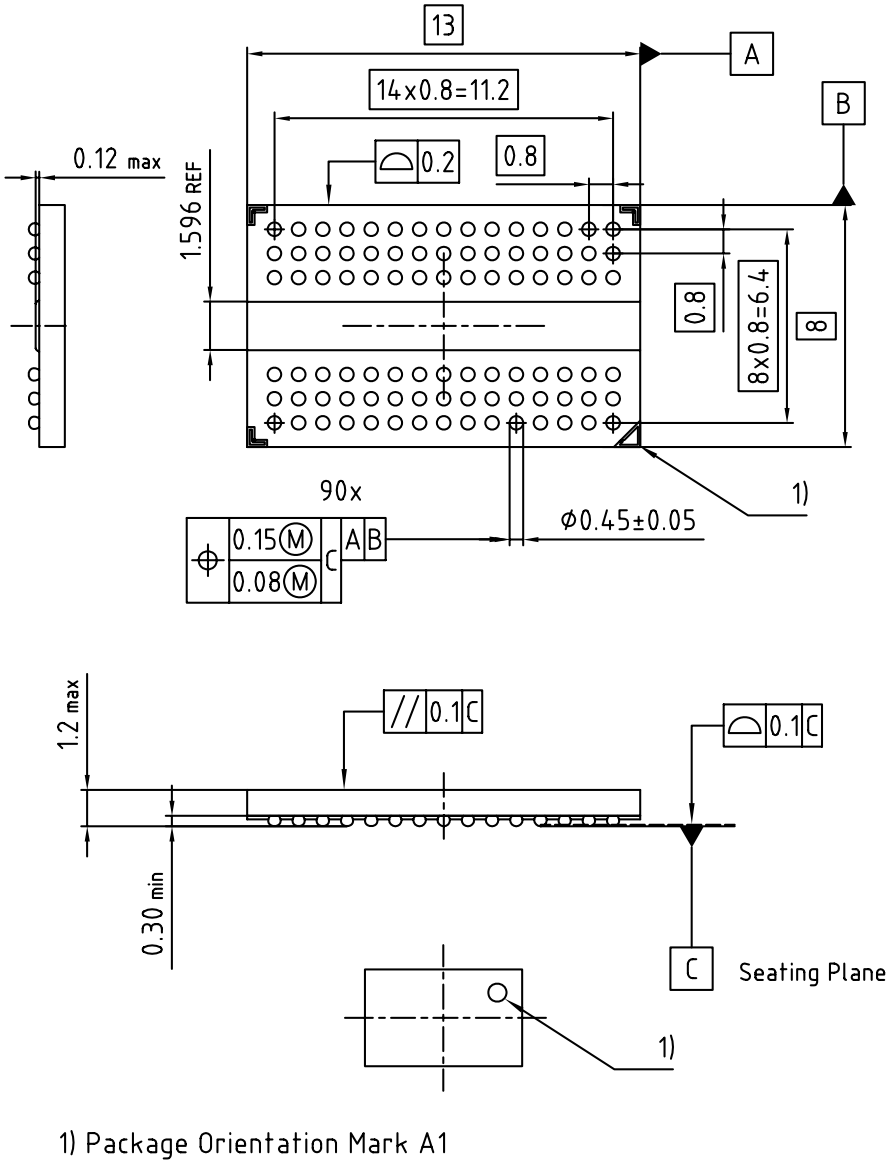
TABLE 16
Half Drive Strength and Full Drive Strength

Voltage (V)	Half Drive Strength				Full Drive Strength			
	Pull-Down Current (mA)		Pull-Up Current (mA)		Pull-Down Current (mA)		Pull-Up Current (mA)	
	Nominal Low	Nominal High	Nominal Low	Nominal High	Nominal Low	Nominal High	Nominal Low	Nominal High
0.00	0.0	0.0	-19.7	-33.4	0.0	0.0	-39.3	-66.7
0.40	15.1	20.5	-18.8	-32.0	30.2	41.0	-37.6	-63.9
0.65	20.3	28.5	-18.2	-31.0	40.5	57.0	-36.4	-61.9
0.85	22.0	32.0	-17.6	-29.9	43.9	64.0	-35.1	-59.8
1.00	22.6	33.5	-16.7	-28.7	45.2	67.0	-33.3	-57.3
1.40	23.5	35.0	-9.4	-20.4	46.9	70.0	-18.8	-40.7
1.50	23.6	35.3	-6.6	-17.1	47.2	70.5	-13.2	-34.1
1.65	23.8	35.5	-1.8	-11.4	47.5	71.0	-3.5	-22.7
1.80	23.9	35.7	3.8	-4.8	47.7	71.4	7.5	-9.6
1.95	24.0	35.9	9.8	2.5	48.0	71.8	19.6	5.0

The above characteristics are specified under nominal process variation / conditionTemperature (Tj): Nominal = 50 °C, V_{DDQ}: Nominal = 1.80 V

4 Package Outlines

FIGURE 3
PG-TFBGA-90-3 (Plastic Thin Fine Ball Grid Array Package)



1) Package Orientation Mark A1

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