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1 Function Description

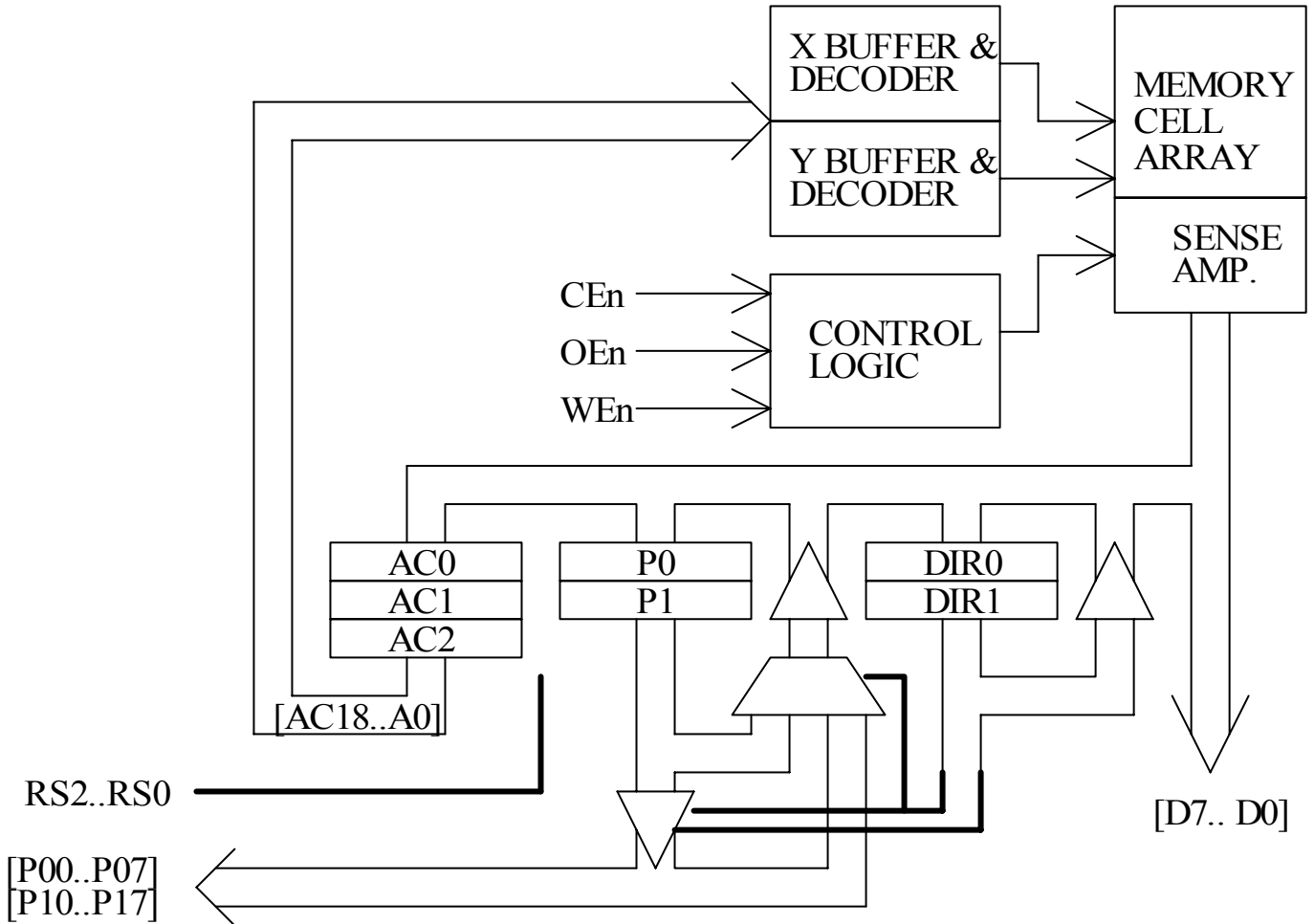
The HF88M08 is a command interfaced 1M x 8 bit Mask ROM. It features command mode interface with external CPU or MCU. In other words, it uses only 8-bit data bus and a few additional control pins to load addresses and provide the ROM access as well as expansion I/O ports capability. This design not only reduces pin count required to access data in ROM dramatically but also allows for systems expansion to higher capacity memories while using the existing board design. The application areas include voice, graphic, data storage in consumer product.

2 Features

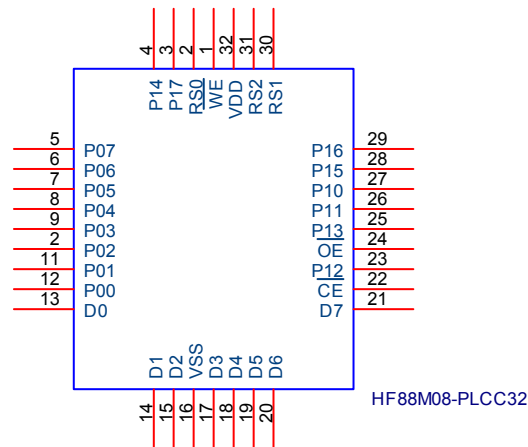
- ✓ Data File Mode with only 11 pin interface
- ✓ Sixteen-bit Expansion I/O pins with three-state mode
- ✓ Voltage range 2.4V ~ 5.5V
- ✓ Organization
 - Memory Cell Array: 1M x 8
- ✓ Sequential Read Operation in Data File Operation Mode
 - Sequential Access : 120ns (min.) at $V_{DD} = 5.0V$
- ✓ Command/Address/Data Multiplexed I/O port
- ✓ Low Operation Current (Typical)
 - 10 μ A Standby mode Current
 - 10mA Active Read Current
- ✓ Package bare chip, PLCC32



3 Functional block diagram



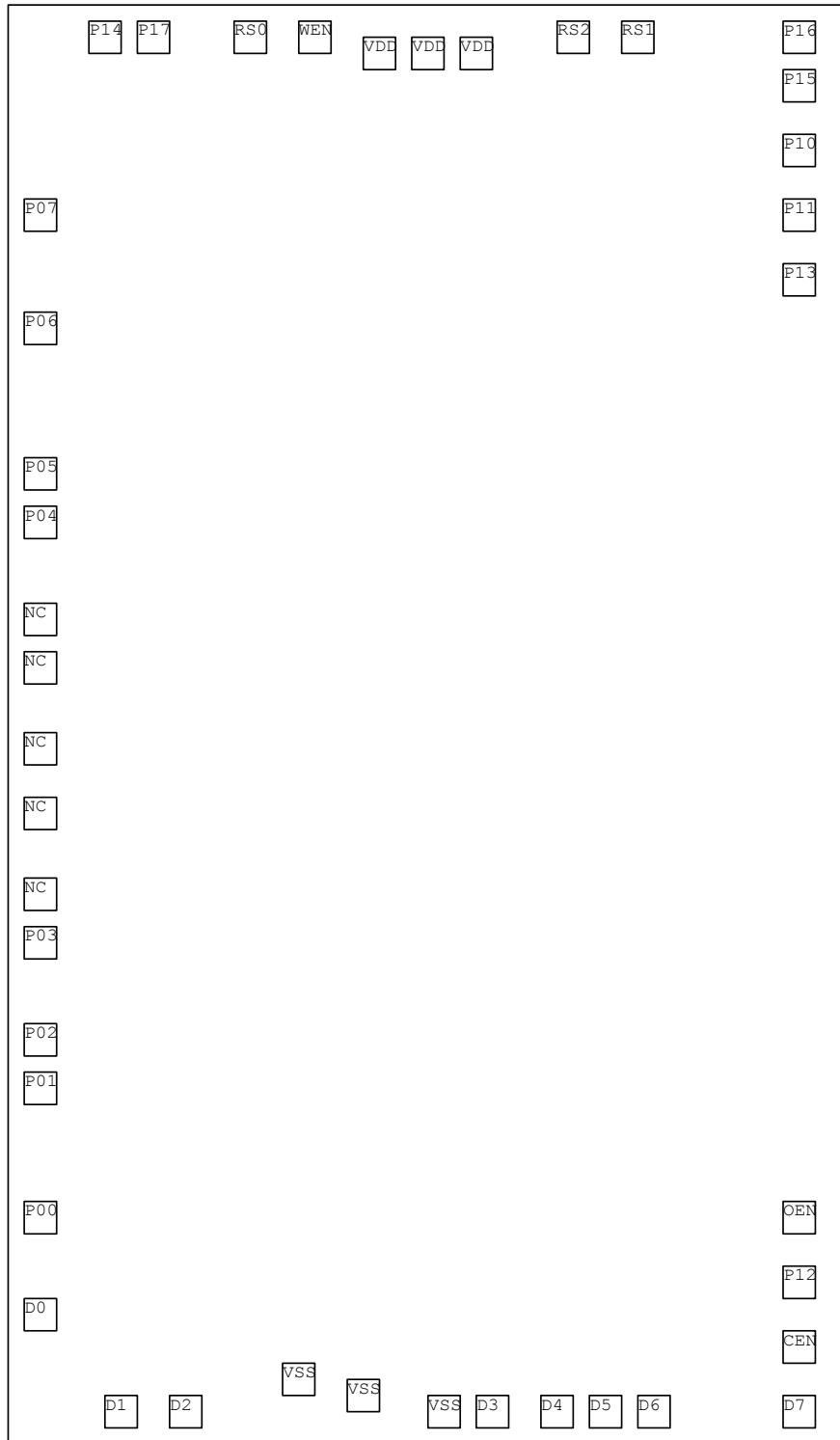
4 Pin Description



Symbol	Pin No.	I/O	Description
VDD	32	P	Positive power supply input pin.
VSS	16	P	Ground pin.
CEn	22	I	The CEn (Chip Enable) input is the device selection and power control for internal Mask ROM array. Whenever CEn goes high, the internal Mask ROM will enter standby (power saving) mode and accesses to internal registers are inhibited. Otherwise, it is in active mode and the contents of the ROM and registers can be accessed. Please note that only accesses to the internal registers are inhibited, but the status of I/O registers are not affected by the CEn pin and will remain unchanged. CEn is also useful to uniquely select a certain device for applications where multiple-chip array is required.
WEn	1	I	WEn controls writing to internal registers such as the Output Port Registers, Direction Registers, Address Counter and Data on D7 ~ D0 are latched on the rising edge of the WE pulse.
OEn	24	I	OEn (Output Enable) is the output control which gates ROM array data, expansion I/O ports, Direction Registers to the data I/O pins D7 ~ D0. The internal Address Counter will automatically increment by one with each rising edge of OEn pin in Sequentially Read mode.
RS2~RS0		I	Register Select pins RS2 ~ RS0 for accessing ROM data, Address Counter, as well as expansion I/O ports.
P17 ~ P10		I/O	Bi-directional I/O port P1.
P07 ~ P00		I/O	Bi-directional I/O port P0.
D7 ~ D0	21 ~ 17, 15 ~ 13	IO	The Bi-directional Data I/O pins are used to input Starting Address, setting the Expansion I/O direction and Output Registers, and to output ROM array data during read operations, contents of I/O Registers and status of input pins. The D7 ~ D7 float to high-impedance when the chip is deselected (CEn high) or when the outputs are disabled.



5 Pad Location





Die Size: X= 2870 μ m, Y=4840 μ m, and substrate is connected to GND.

Pad No.	Pad Name	X Coord.	Y Coord.	Pad No.	Pad Name	X Coord.	Y Coord.
1	WEN	1028.23	4726.24	22	VSS	1222.34	140.91
2	RS0	836.35	4726.24	23	VSS	1501.38	108.09
3	P17	495.57	4722.3	24	D3	1664.02	109.14
4	P14	308.13	4722.3	25	D4	1851.18	109.14
5	P07	108.33	4097.34	26	D5	2038.62	109.14
6	P06	108.33	3743.44	27	D6	2225.78	109.14
7	P05	108.33	3262.4	28	D7	2725.87	105.79
8	P04	108.33	3071.78	29	CEN	2725.87	340.24
9	NC	108.33	2786.78	30	P12	2725.87	537.52
10	NC	108.33	2598.09	31	OEN	2725.87	730.47
11	NC	108.33	2315.6	32	P13	2728.88	3911.29
12	NC	108.33	2127.68	33	P11	2728.88	4116.11
13	NC	108.33	1843.32	34	P10	2728.88	4318.77
14	P03	108.33	1656.15	35	P15	2728.87	4531.23
15	P02	108.33	1357.04	36	P16	2728.87	4725.13
16	P01	108.33	1169.6	37	RS1	2107.66	4736
17	P00	108.33	758.2	38	RS2	1908.12	4736
18	D0	108.33	403.24	39	VDD	1578.76	4688.71
19	D1	395.97	109.14	40	VDD	1404.34	4688.71
20	D2	583.13	109.14	41	VDD	1229.92	4688.71
21	VSS	985.16	190.94				

6 Device Operation

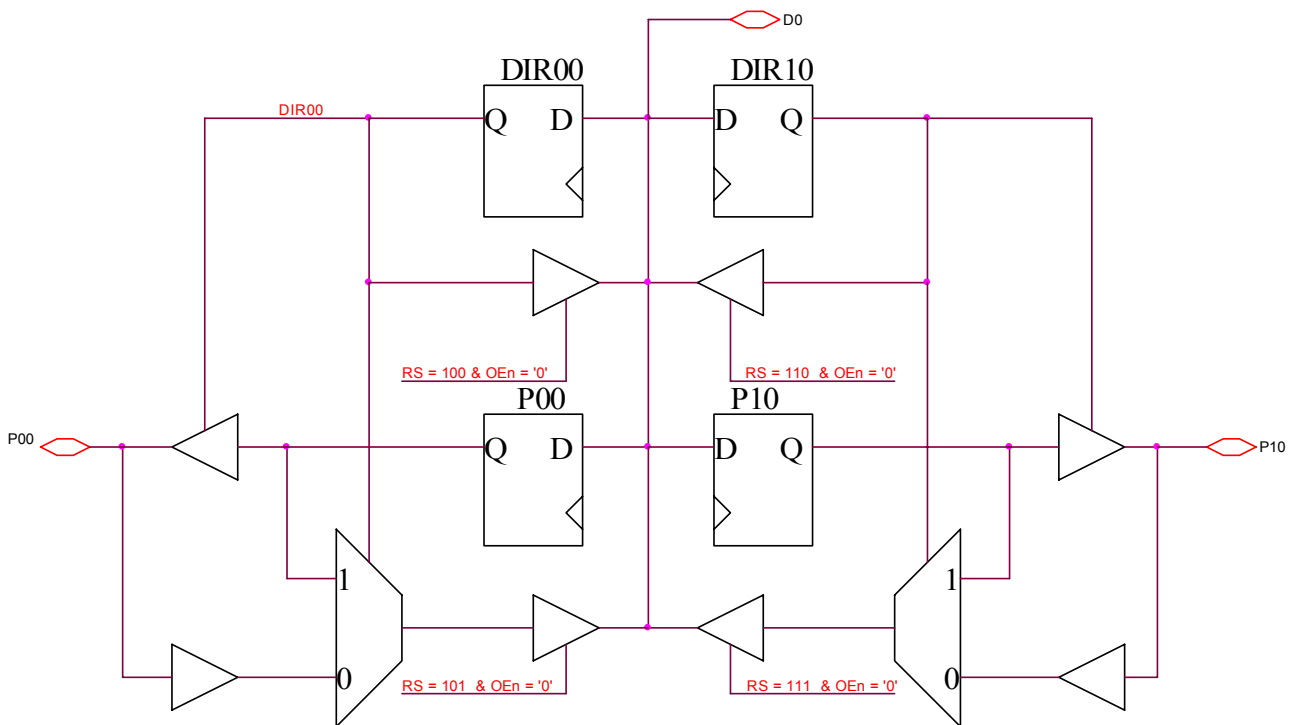
The device provides the capability of accessing the contents of ROM array by external MCU not through standard address and data bus configuration but through minimal number of 8-bit data bus and control pins. Only 11 pins D7 ~ D0, CEn, OEn, WEn are required to use the device as a Data File device. By fixing the RS2 to '0', only CEn, WEn, OEn and D0 ~ D7 are required to access the ROM array data.

The CEn pin is device selection pin to uniquely select one device when more than one device are used in parallel and control the access to Mask ROM contents and internal registers. Whenever CEn goes high, the internal Mask ROM will enter standby (power saving) mode and accesses to internal registers are inhibited. Otherwise, it is in active mode. Therefore, when accessing contents of ROM is not intended, CEn should stay at '1' to conserve the power.

In addition to Data File mode, the device also provides the expansion I/O capability. Two ports of I/O pins (8 bit each) are provided. The I/O ports can be configured to function as output pin or high-impedance input pins. Only 14 pins, CEn, WEn, OEn, RS2, RS1 and D0 ~ D7 are required to provide the Data File function and full access to two I/O ports.

There are seven internal registers used to provide the functionality of Data file as well as Expansion I/O capability. These registers are selected by RS2 ~ RS0. All registers are 8-bit wide except AC2. AC2 ~ AC0 are write-only and constitute the complete 20-bit Address Counter used as pointer to the data. While the P0, P1, DIR0 and DIR1 can be read as well as written. Their initial values are as indicated in the following table. When RS2 = '0', the RS1 ~ RS0 are ignored, the Address Counter can be loaded or contents of Data File can be read. This is to reduce the required pin needed for external MCU to interface with the Device and also simplify the procedure for loading the address counter.

The P0, P1, DIR0, and DIR1 are used for expansion I/O registers. The P0 and P1 are output registers of Expansion I/O and DIR0 and DIR1 are the Direction Registers that determine the I/O mode of P0 and P1. Each pin can be configured as output or input mode individually by setting or resetting the corresponding pin of the DIR registers. Initially, both P0 and P1 are default to input mode at 'Hi' state.



The accesses to the internal registers will be inhibited when CEn is '1'. However, the status of internal registers, such as expansion I/O ports, will not be affected. For example, if a certain pin is in output mode and driving 'Hi', it will not change when CEn pin goes to '1' state. Therefore, the users are advised to take care of the power down condition of I/O ports when entering sleep mode to prevent



unnecessary power drain.

RS ₂ RS ₁ RS ₀	Symbol	Type	Description	Initial Value
0xx		R	Read data by Indirect access	
	AC2	W	Address latch 2 for A19 ~ A16	“-----“
	AC1	W	Address latch 1 for A15 ~ A8	“-----“
	AC0	W	Address latch 0 for A7 ~ A0	“-----“
100	P0	R/W	Port 0 Output Register	“1111111“
101	DIR0	R/W	Direction Register 0	“0000000“
110	P1	R/W	Port 1 Output Register	“1111111“
111	DIR1	R/W	Direction Register 0	“0000000“

6.1 Retrieve data in Data File

Accesses to the ROM contents, expansion I/O, Address Counter and Direction registers are made through 8 Data I/O pins – D7 ~ D0. With Register Selection RS = “0xx”, the starting addresses can be written through Data I/Os by bringing WEn to low and back to high. Addresses are latched on the rising edge of WEn.

Once the starting address of data block is latched into the Address Counter, data may be read out by sequentially pulsing OEn with CEn staying low. When at ‘0’, the OEn gate the data of the selected address unto Data I/O pin D7 ~ D0. With the rising edge of OEn, the internal Address Counter is incremented by one automatically.

6.2 Loading the Address Counter

Before the data can be retrieved, the Address Counter must be initialized with the starting address, then the contents of ROM pointed to by Address Counter (AC) can be accessed through D7 through D0. In order to simplify the procedure of loading 20-bit Address Counter (AC), a internal pointer is implemented and used to point to next register to write in the up to three-cycle address loading sequence. Initially, with RS = “0xx” CEn goes from ‘1’ to ‘0’ and the AC pointer is initialized. The pointer is then incremented to point to next register with falling edge of each WEn pulse. So when randomly accessing data within a 256-byte page, or within a 64K-byte block mode, then only one or two-cycle address reload process is needed to access different locations within a page or block.

The Address Counter pointer will be held in reset state in the following conditions:

1. When CEn is '1' (the device is deselected).
2. By the Read pulse (OEn is '0') and RS₂ = '0' (ROM is being accesses).

The inclusion of the 3rd condition is to force the address loading to start from LSB of Address Counter once the read cycle is initiated. However, the AC Pointer will not be reset when reading or writing



from/to expansion I/O registers (P0, P1, DIR0, DIR1). This design is useful in certain application scenarios where in the midst of the multi-byte address loading process, an interrupt to the MCU main loop occurs. And in the interrupt service routine, manipulation of expansion I/O registers is performed, i.e., key board is scanned using P0 and P1. When the execution of program returns to main loop after interrupt service routine completed, the loading of address can still resume from where it was interrupted.

6.3 Sequential Read Mode and Auto Increment of Address Counter

With each read access to the ROM data (RS = "0xx"), the Address Counter is incremented automatically by one with rising edge of OEn to facility sequential access to a block of ROM data and avoid repeated loading of addresses.

6.4 Output data to External I/O

The device's 16-bit Expansion I/O capability provides additional I/O ports for applications where the I/O pin are heavily used. To use as a certain pin as output pin, the corresponding bit in Direction Register must be set to '1'. Please refer to the following example where output 0x00 to P0 to '0' is intended.

1. Set RS to "101" (DIR0).
2. Keep D7 ~ D0 at 0xff (all bits in output mode).
3. Pulse the WEn to low then high to write contents of D-bus to DIR0.
4. Set RS to "100" (P0 Output Register).
5. Set D7 ~ D0 to 0x00.
6. Pulse the WEn to low then high to write contents of D-bus to P0 and drive all bits in P0 to low.

6.5 Reading Input pin status

To use expansion I/O ports as input pins and read the status from them, the corresponding bit in direction register must be set to '0'. Please see the following example where reading inputs from of P1 is intended.

1. Set RS to "111" (DIR1).
2. Set D7 ~ D0 to 0x00.
3. Pulse the WEn to low then high to set DIR1 to all High-Impedance input mode.
4. Set RS to "110" (P1 Output Register).
5. Pulse the OEn to low.
6. Read P1 then set the OEn back to high.

There is one thing should be noted. For any unused (open) expansion I/O pin, it is advisable to set the port to output mode either at '0' or '1' state to prevent it from floating or fix it at VDD or VSS if it is set to input mode. Otherwise, the noise might cause the unnecessary power consumption.

6.6 Retrieving the Contents of Expansion I/O registers

The contents of all four registers can be read through data bus. The ability to access the contents of



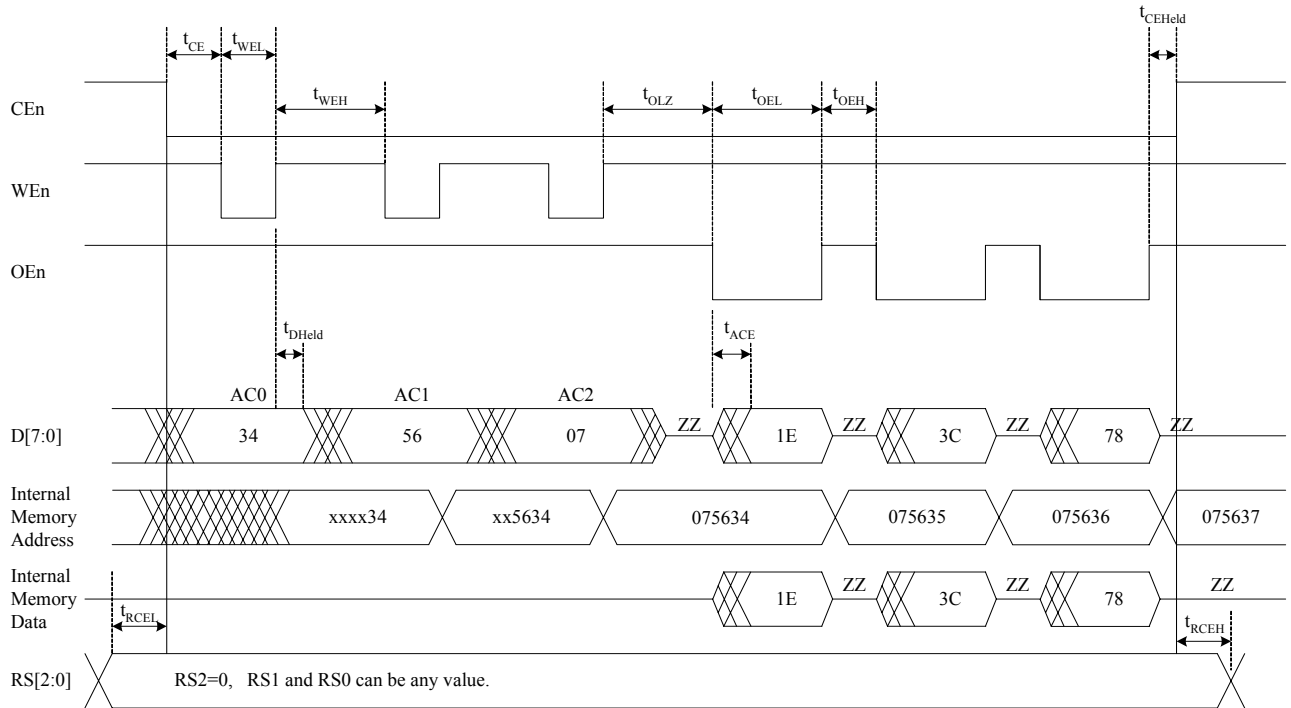
registers avoids the necessity of using the RAM as mirror to keep the current status of latches in applications. However, extra care should be taken when reading P0 and P1. To read the contents of P0 and P1, the DIR0 and DIR1 should be set to output mode. Otherwise, the pin status instead of P0 and P1 will be read. The same precaution should be applied in Read-Modify-Write sequence that read back the contents of the output latch of output mode pins and input status of input mode pins.

7 Timing Diagrams

Symbol	Parameter	Min.	Typ.	Max.	Unit
T _{CE}	Chip selected to active width	0	50	-	ns
T _{WEL}	WEn active low width	100	-	-	ns
T _{WEH}	WEn inactive low width	100	-	-	ns
T _{DHeld}	Written data hold time	50	-	-	ns
T _{OLZ}	Read-Write mode transient time	200	-	-	ns
T _{ACE}	ROM data file available time	50	-	-	ns
T _{OEL}	Output enable low duty for access ROM	250	-	-	ns
T _{OEH}	Output enable low duty for access ROM	150	-	-	ns
T _{CEHeld}	Chip selection signal holding time	50	-	-	ns
T _{ACER}	Register data available time	30	-	-	ns
T _{ORL}	Output enable low duty for access register	100	-	-	ns
T _{ORH}	Output enable low duty for access register	100	-	-	ns
T _{RCEL}	RS signal setup time	50	-	-	ns
T _{RCEH}	RS signal hold time	50	-	-	ns



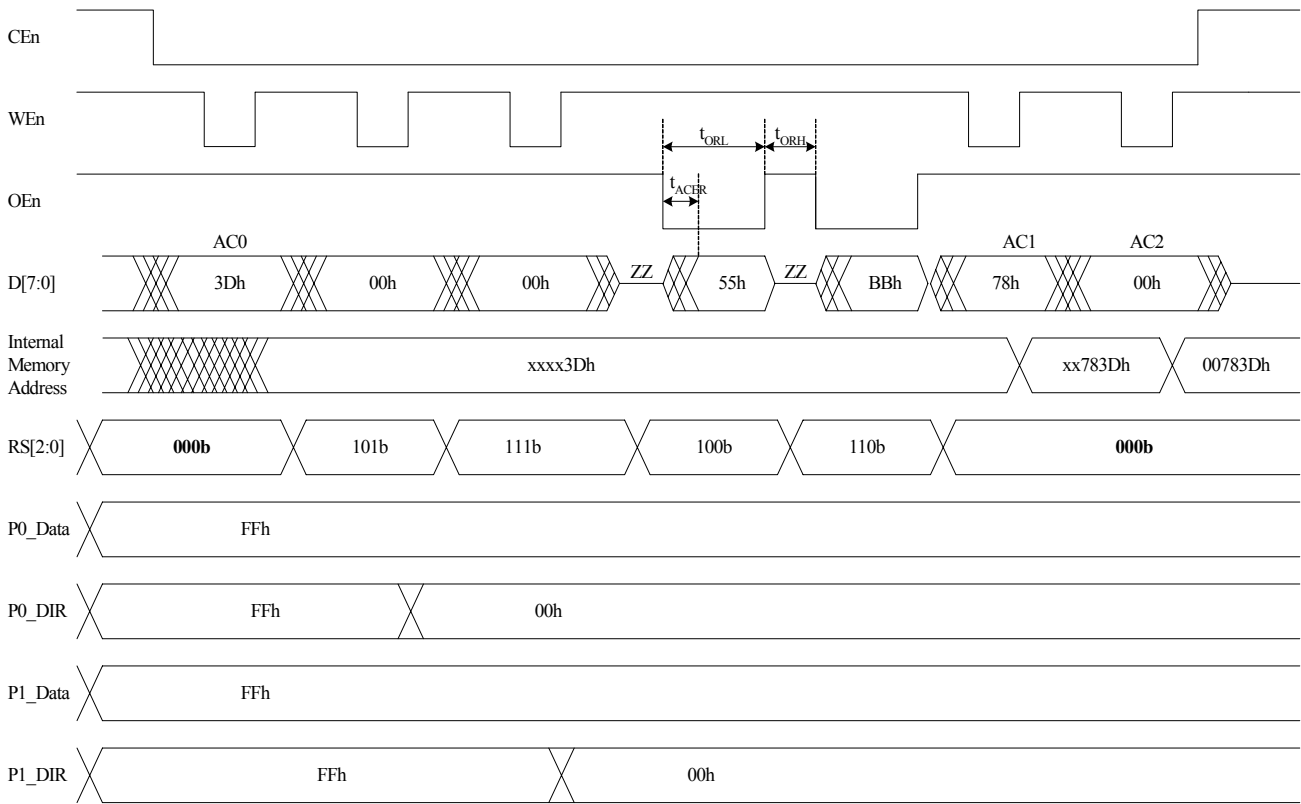
7.1 Data File Read Cycle



Data File Read Cycle



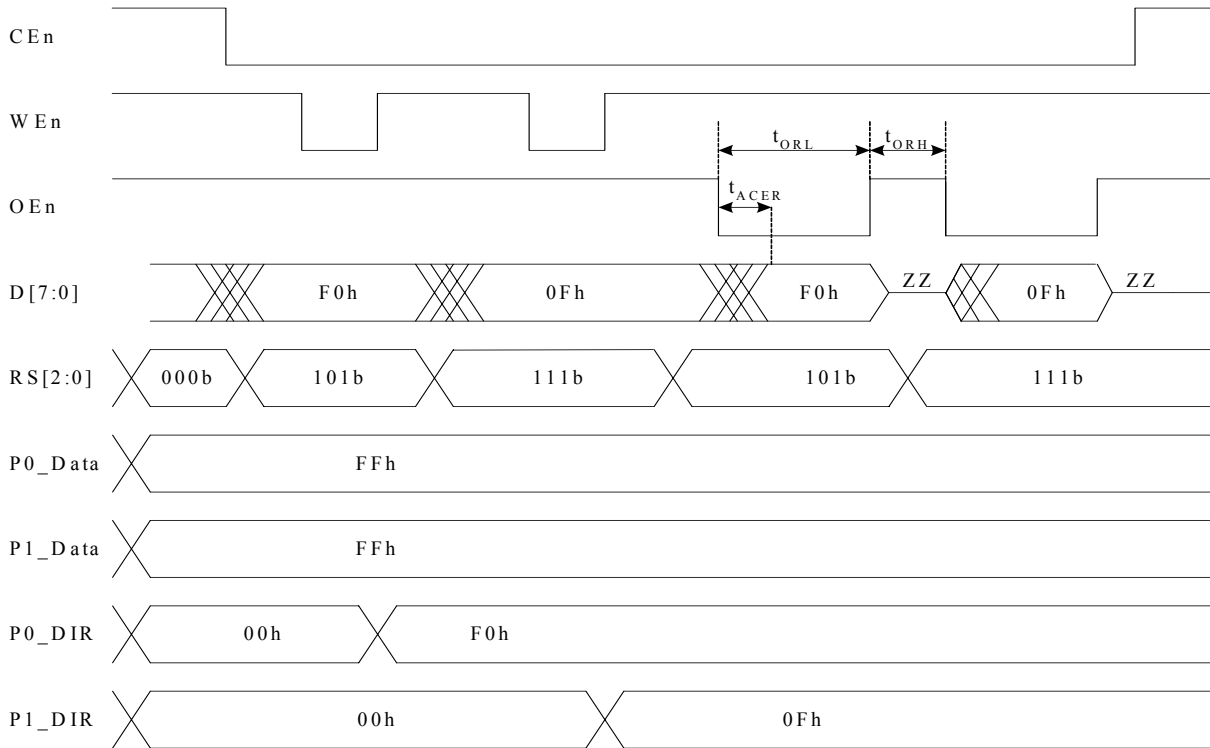
7.2 Interrupted by I/O when Loading Address Counter



Interrupted by I/O when Loading Address Counter



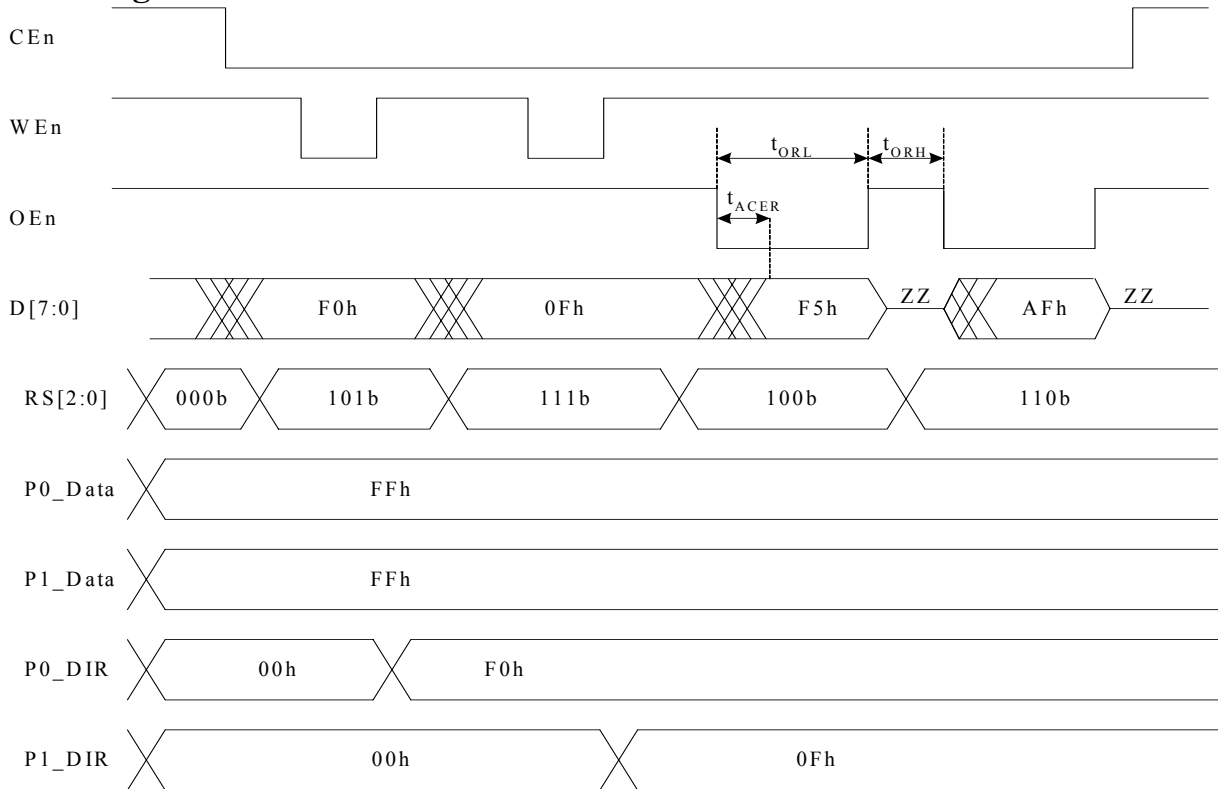
7.3 Setting and Reading the I/O Mode for P0 and P1



Setting and Reading the I/O Mode for P0 and P1



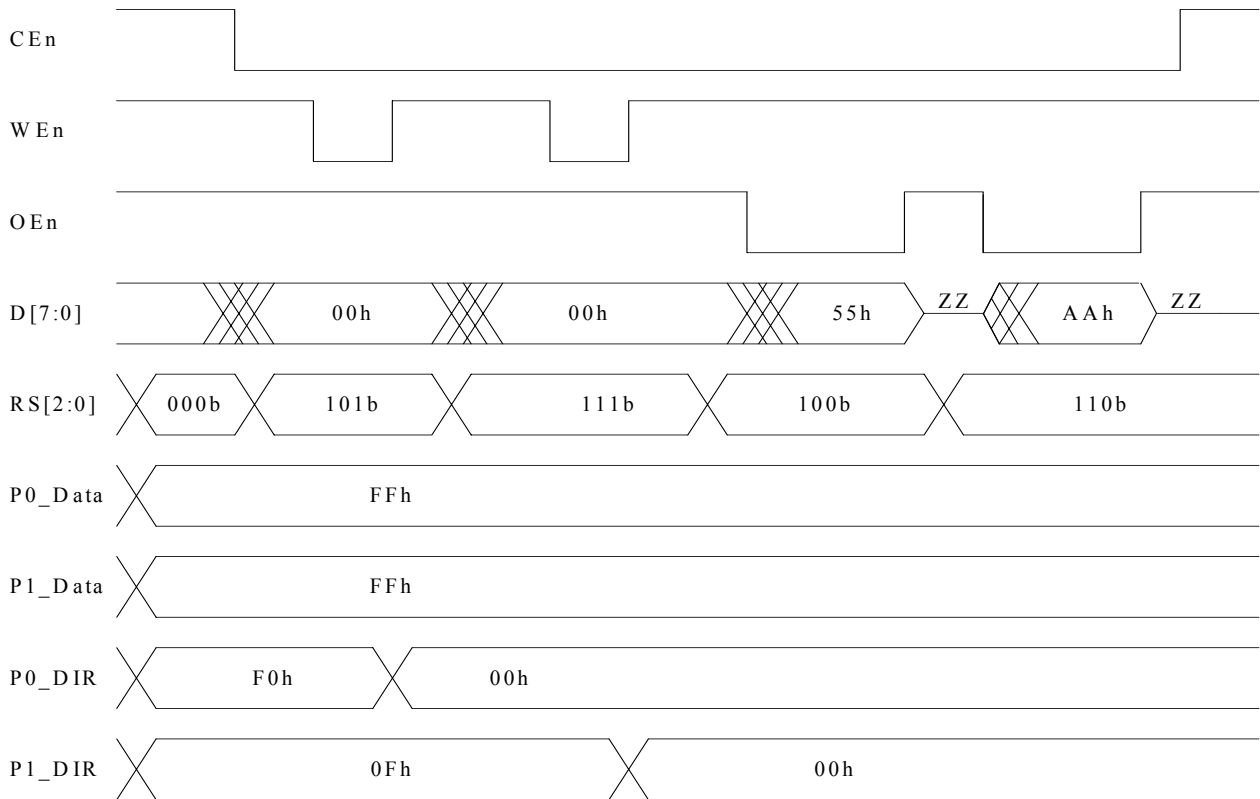
7.4 Reading P0 and P1 in Mixed-I/O Mode



Reading P0 and P1 in Mixed-I/O Mode



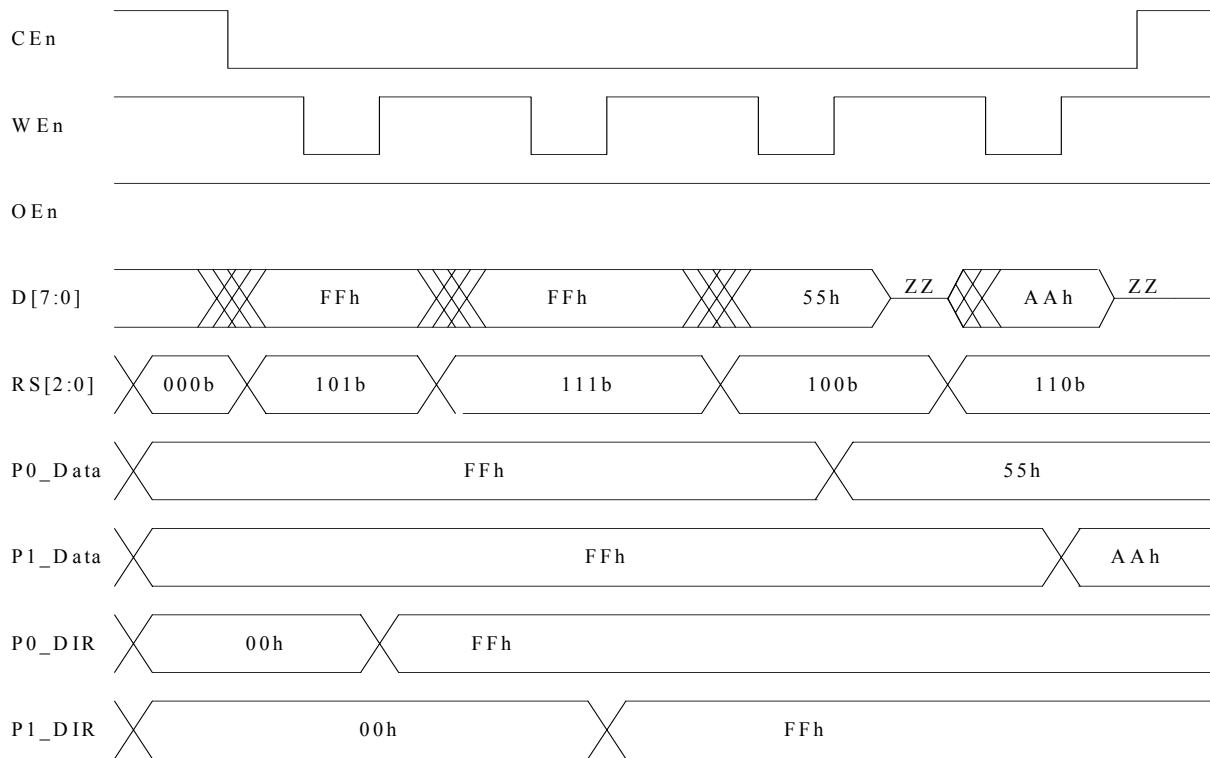
7.5 Reading the input pins



Reading the Input Pins



7.6 Output to P0 and P1 Ports



Output to P0 and P1 Ports

8 Absolute Maximum Rating

Items	Symbol	Rating	Condition
Supply Voltage	V_{DD}	-0.3 to 6 V	
Input Voltage	V_{IN}	-0.3 to $V_{DD}+0.3$ V	
Operating Temperature	T_{OPR}	-0 to 70 °C	
Storage Temperature	T_{STR}	-55 to 125 °C	

9 AC Electrical Characteristics

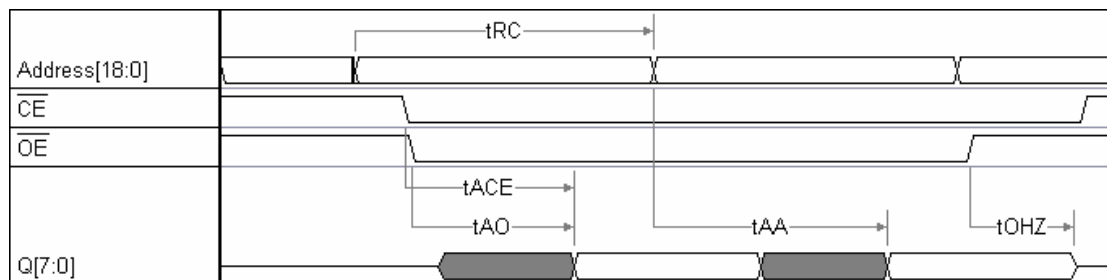
READ CYCLE

There are two ways of accessing the ROM data. The first one is to assert the valid address on the Address Bus, then assert CEn “low” to enable the ROM array. The access time in this mode is specified as t_{ACE} . The advantage of this access mode is that power consumption can be lowered. The second access mode keeps the CEn “low” while changes the addresses to access the contents of ROM data. The



access time in this way is specified as t_{AA} . In this device, the Address Access Time decrease monotonically with increasing voltage, and it is shorter than Chip Enable Access Time when the Operation Voltage is higher than 4.5 V. Therefore in V_{op} higher than 4.5 Volts, it is more advisable to use the Address Access Mode to achieve faster access to ROM data when the power consumption is not a concern.

Item	Symbol	2.4V	3.0V	3.3V	3.6V	4.5V	5.0V	5.5V	Unit	Remark
Chip Enable Access Time	t_{ACE}	-	240	210	190	180	210	250	ns	Min
Address Access Time	t_{AA}	480	230	200	180	150	140	130	ns	Min



10 DC Electrical Characteristics

($V_{SS} = 0V$, $V_{DD} = 5.0V$, $T_{OPR} = 25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Min.	Typical	Max.	Unit	Condition
Supply Voltage	V_{DD}	2.4	-	5.5	V	
Operating Current	I_{DD}	-	10	-	mA	No load
Standby Current	I_{DD}	-	10	-	μA	No load
Input voltage	V_{IH} V_{IL}	2/3 0	- -	1 1/3	V_{DD}	$V_{DD} = 4V \sim 6V$
Input current leakage	I_{IL}	-	-	+/- 10	μA	
P0, P1 Output High Voltage	V_{OH}	2.4	-	-	V	$I_{OH} = 0.4 mA$
P0, P1 Output Low Voltage	V_{OL}	-	-	0.4	V	$I_{OL} = 2.1 mA$
D Output High Voltage	V_{OH}	2.4	-	-	V	$I_{OH} = 14 mA$
D Output Low Voltage	V_{OL}	-	-	0.4	V	$I_{OL} = 3 mA$

11 Application Circuit Diagram

This application circuit illustrates that how KB83760 MCU uses two external HF88M08s for ROM expansion as well as keyboard scan functions.



12 Updated History

Version	Date	Update Description
1.10	2003/8/27	Timing diagrams modified.
1.11	2004/1/16	Add the die size