A.HE83015 Introduction

HE83015 is a member of 8-bit Micro-controller series developed by King Billion Electronics Ltd. It is a power speech controller. The built-in OP comparator can be used with (light、voice、temperature、humility) sensor and used as battery low detection. And the 7-bit current-type D/A converter and PWM device provide the complete speech output mechanism. The 128 ROM Size can be used in the storage of speech (40 seconds at 3Kbytes per second).

The instruction set of HE83015 are quite easy to learn and simple to use. Only about thirty instructions with four-type addressing mode are provided. Most of instructions take only 3 oscillator clocks (machine cycles). The processing power is enough to most of battery operation system.

B.HE83015 Features

- Operation Voltage： 2.4V – 5.5V
- System Clock： DC ~ 8MHz @ 5.0V
  DC ~ 4MHz @ 2.4V
- Internal ROM： 128K Bytes(64K Program ROM, 64K Data ROM)
- Internal RAM： 128 Bytes.
- Dual Clock System ： Normal (Fast) clock： 32.768K ~ 8MHz
  Slow clock： 32.768KHz
- Operation Mode： DUAL、FAST、SLOW、IDLE、SLEEP Mode.
- With WDT (WATCH DOG TIMER) to prevent deadlock condition..
- 24 bit Bi-directional I/O port. Mask Option can select PUSH-PULL or OPEN DRAIN output mode for each I/O pin.
- One built-in OP comparator.
- One 7-bit current-type DAC output.
- PWM device.
- Two external interrupts and two internal timer interrupts.
- Two 16-bit timer. (Clock Source reference by Fast Clock)
- Instruction set： 32 instructions, 4 addressing mode. 7-bit DATA POINTER for RAM and 17-bit TABLE POINTER for ROM.

C. Internal Block

Please always take in mind that ICE is different from IC. ICE is the whole set of HE80000 series IC, but each IC is a subset of ICE. Never use any hardware resource that real IC didn't have, especially RAM and register. KBIDS and compiler cannot prevent user to use some hardware resource that didn't exist. Please check the following table and refer the abbreviation in HE80000 user's manual.

I.F.C.	E.S.C.	I.P.R	PROM	DROM	TP	TP+1	RAM	PP	DP	I/O	DTMF	WDT	Timer
◎	◎	◎	64KB	64KB	17-bit	◎	128B	—	7-bit	24	—	◎	T1,T2

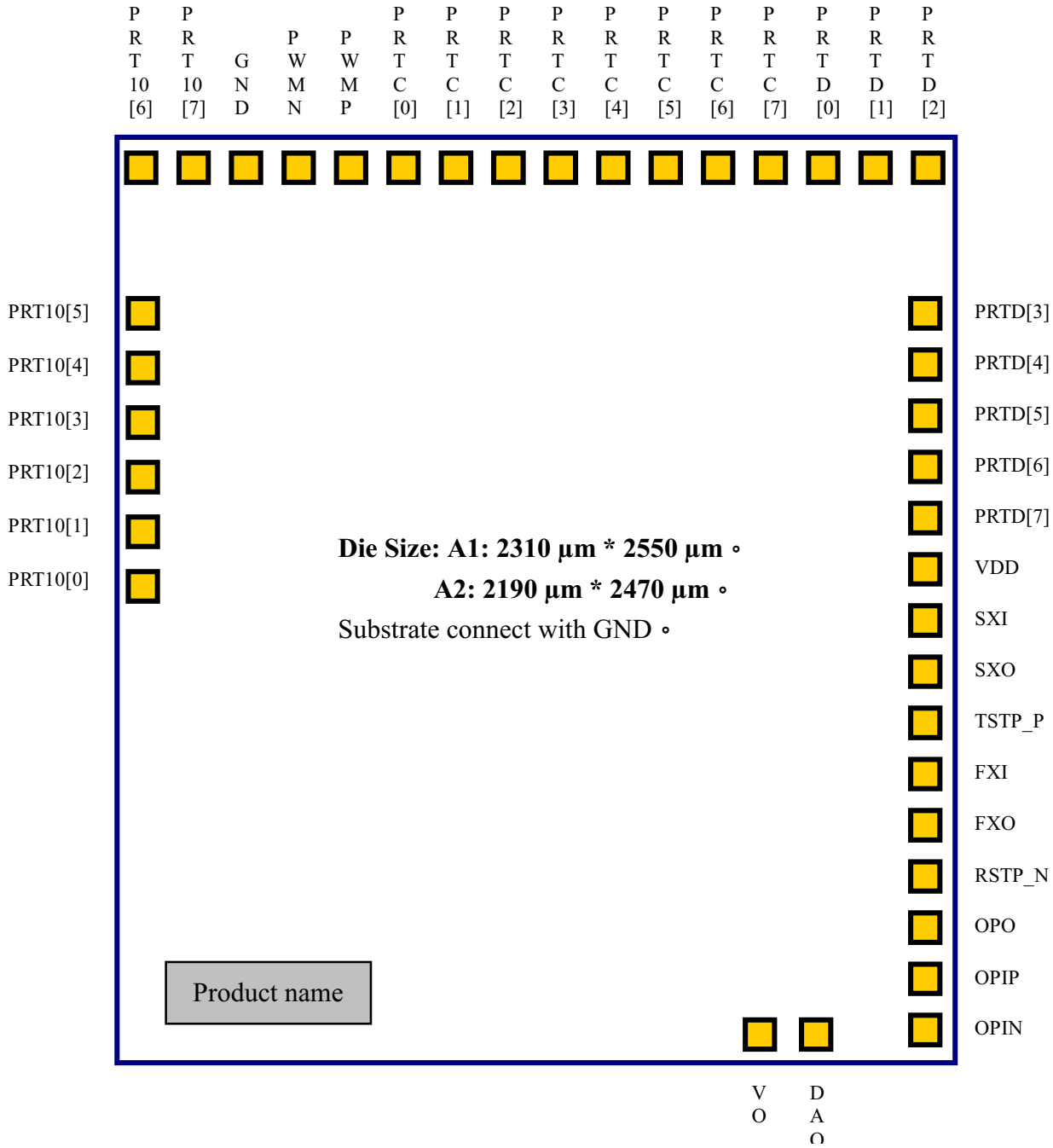
VO	DAO	OP	PWM	LCD	COM*SEG	Bias	Rgr	ChrgPmp	LV2	LR	LVG	REC	S.R.
◎	◎	◎	◎	—	—	—	—	—	—	—	—	Ext.	—

D. Pin Description

Pin #	Pin name	I/O	Function	Description
15 14	**FXI,** **FXO**	B, O	External fast clock pin. Connecting to crystal or RC to generate 32.768 kHz ~ 8MHz frequency.	Mask option setting： MO_FCK/SCKN= 00：Slow Clock only 01：Illegal 10：Dual Clock 11：Fast Clock only MO_FOSCE = 0：Internal fast osc. = 1：External fast osc.
18 17	**SXI,** **SXO**	I, O	External slow clock pin. Connecting with 32768 Hz crystal or resistor as slow clock and providing clock source for LCD display, TIMER1, Time-Base and other internal blocks.	MO_FXTAL= 0：RC osc. for fast clock = 1：X'tal osc. for fast clock MO_SXTAL= 0：RC for 32768 Hz clock = 1：X'tal for 32768 Hz clock Use OP1 and OP2 to switch among different operation mode (NORMAL, SLOW, IDEL and SLEEP). In Dual Clock mode, the main system clock is still the Fast Clock. The 32768 Hz clock is for LCD and Timer 1 only.
13	**RSTP_N**	I	System Reset.	Level trigger, active low. Except for using this pin, using mask option (MO_PORE=1) could enable IC build-in power-on reset circuit. Besides, MO_WDTE can set Watch Dog Timer： MO_WDTE=0：Disable Watch Dog Timer =1：Enable Watch Dog Timer
16	**TSTP_P**	I	Test Pin	Please bond this pin and add a test point on PCB for debugging. Leave this pin floating is OK.
28.. 35	**PRTC[7:0]**	B	8-pin bi-directional I/O port.	Mask options： MO_CPP[7..0]=1 ~ Push-pull. =0 ~ Open-drain. Output must be "1" before reading whenever use them as input (No tri-state structure).
20.. 27	**PRTD[7:0]**	B	8-pin bi-directional I/O port. PRTD[7..2] as wake-up pin. PRTD[7..6] as external interrupt pin.	Mask options： MO_DPP[7..0]=1 ~ Push-pull. =0 ~ Open-drain. Output must be "1" before reading whenever use them as input (No tri-state structure).
39 1..7	**PRT10[7:0]**	B	8-pin bi-directional I/O port.	Mask options： MO_10PP[7..0]=1 ~ Push-pull. =0 ~ Open-drain. Output must be "1" before reading whenever use them as input (No tri-state structure).
36	**PWMP**	O	The PWM positive output can drive speaker or buzzer directly.	Set the bit2 of VOC register as one to turn on PWM.
37	**PWMN**	O	The PWM positive output can drive speaker or buzzer directly.	Set the bit2 of VOC register as one to turn on PWM.
8	**VO**	O	DAC Voice Output	Set the bit1(DA=1) of VOC register to turn on DAC with VO output.
9	**DAO**	O	Alternative Output of DAC	Set the bit0(OP=1) of VOC register to turn on DAC with VO output and also turn OP comparator on.

Pin #	Pin name	I/O	Function	Description
10	**OPIN**	I	Negative input of OP comparator	Set the bit0(OP=1) of VOC register to turn on OP comparator.
11	**OPIP**	I	Positive input of OP comparator	
12	**OPO**	O	Output of OP comparator	
19	**VDD**	P	Positive Power Input	Adding 0.1 µF capacitor as by-pass capacitor is between VDD and GND is necessary.
38	**GND**	P	Power Ground Input	

E. Pin Diagram



F. Bonding Pad Location

Which version of IC decided by KB when customer gives order to KB. Please make sure which version will be used before you make a PCB!

Version A1:

PIN Number	PIN Name	X Coordinate	Y Coordinate	PIN Number	PIN Name	X Coordinate	Y Coordinate
1	PRT10[6]	X= -1043.30	Y= 1195.10	21	PRTD[6]	X= 1061.90	Y= 418.40
2	PRT10[5]	X= -1074.25	Y= 831.40	22	PRTD[5]	X= 1061.90	Y= 555.35
3	PRT10[4]	X= -1074.25	Y= 694.45	23	PRTD[4]	X= 1061.90	Y= 692.30
4	PRT10[3]	X= -1074.25	Y= 557.50	24	PRTD[3]	X= 1061.90	Y= 829.25
5	PRT10[2]	X= -1074.25	Y= 420.55	25	PRTD[2]	X= 1010.95	Y= 1195.10
6	PRT10[1]	X= -1074.25	Y= 283.60	26	PRTD[1]	X= 874.00	Y= 1195.10
7	PRT10[0]	X= -1074.25	Y= 146.65	27	PRTD[0]	X= 737.05	Y= 1195.10
8	VO	X= 582.85	Y= -1117.55	28	PRTC[7]	X= 600.10	Y= 1195.10
9	DAO	X= 730.35	Y= -1117.55	29	PRTC[6]	X= 463.15	Y= 1195.10
10	OPIN	X= 1061.90	Y= -1088.05	30	PRTC[5]	X= 326.20	Y= 1195.10
11	OPIP	X= 1061.90	Y= -951.10	31	PRTC[4]	X= 189.25	Y= 1195.10
12	OPO	X= 1061.90	Y= -814.15	32	PRTC[3]	X= 52.30	Y= 1195.10
13	RSTP_N	X= 1061.90	Y= -677.20	33	PRTC[2]	X= -84.65	Y= 1195.10
14	FXO	X= 1061.90	Y= -540.25	34	PRTC[1]	X= -221.60	Y= 1195.10
15	FXI	X= 1061.90	Y= -403.30	35	PRTC[0]	X= -358.55	Y= 1195.10
16	TSTP_P	X= 1061.90	Y= -266.35	36	PWMP	X= -495.50	Y= 1195.10
17	SXO	X= 1061.90	Y= -129.40	37	PWMN	X= -632.45	Y= 1195.10
18	SXI	X= 1061.90	Y= 7.55	38	GND	X= -769.40	Y= 1195.10
19	VDD	X= 1061.90	Y= 144.50	39	PRT10[7]	X= -906.35	Y= 1195.10
20	PRTD[7]	X= 1061.90	Y= 281.45				

Version A2:

PIN Number	PIN Name	X Coordinate	Y Coordinate	PIN Number	PIN Name	X Coordinate	Y Coordinate
1	PRT10[6]	X= -1135.45	Y= 1113.75	21	PRTD[6]	X= 871.00	Y= 445.05
2	PRT10[5]	X= -1165.40	Y= 752.75	22	PRTD[5]	X= 871.00	Y= 560.95
3	PRT10[4]	X= -1165.40	Y= 636.85	23	PRTD[4]	X= 871.00	Y= 676.85
4	PRT10[3]	X= -1165.40	Y= 520.95	24	PRTD[3]	X= 871.00	Y= 792.75
5	PRT10[2]	X= -1165.40	Y= 405.05	25	PRTD[2]	X= 701.85	Y= 1113.75
6	PRT10[1]	X= -1165.40	Y= 289.15	26	PRTD[1]	X= 585.95	Y= 1113.75
7	PRT10[0]	X= -1165.40	Y= 173.25	27	PRTD[0]	X= 470.05	Y= 1113.75
8	VO	X= 615.50	Y= -1199.55	28	PRTC[7]	X= 354.15	Y= 1113.75
9	DAO	X= 780.80	Y= -1199.55	29	PRTC[6]	X= 238.25	Y= 1113.75
10	OPIN	X= 871.00	Y= -829.85	30	PRTC[5]	X= 122.35	Y= 1113.75
11	OPIP	X= 871.00	Y= -713.95	31	PRTC[4]	X= 6.45	Y= 1113.75
12	OPO	X= 870.95	Y= -598.05	32	PRTC[3]	X= -109.45	Y= 1113.75
13	RSTP_N	X= 871.00	Y= -482.15	33	PRTC[2]	X= -225.35	Y= 1113.75
14	FXO	X= 871.00	Y= -366.25	34	PRTC[1]	X= -341.25	Y= 1113.75
15	FXI	X= 871.00	Y= -250.35	35	PRTC[0]	X= -457.15	Y= 1113.75
16	TSTP_P	X= 871.00	Y= -134.45	36	PWMP	X= -598.85	Y= 1113.75
17	SXO	X= 871.00	Y= -18.55	37	PWMN	X= -764.15	Y= 1113.75
18	SXI	X= 871.00	Y= 97.35	38	GND	X= -903.65	Y= 1113.70
19	VDD	X= 871.00	Y= 213.25	39	PRT10[7]	X= -1019.55	Y= 1113.75
20	PRTD[7]	X= 871.00	Y= 329.15				

G. DC/AC Characteristics

Absolute Maximum Rating

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	-0.5V ~ 8V	
Input Voltage	V_{in}	-0.5V ~ V_{dd}+0.5V	
Output Voltage	V_o	-0.5V ~ V_{dd}+0.5V	
Operating Temperature	T_{op}	0^0C ~ 70^0C	
Storage Temperature	T_{st}	-50^0C ~ 100^0C	

Recommended Operating Conditions

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	2.4V ~ 5.5V	
Input Voltage	V_{ih}	0.9 V_{dd} ~ V_{dd}	
	V_{il}	0.0V ~ 0.1V_{dd}	
Operating Frequency	Fmax	8MHz	V_{dd} =5.0V
		4MHz	V_{dd} =2.4V
Operating Temperature	T_{op}	0^0C ~ 70^0C	
Storage Temperature	T_{st}	-50^0C ~ 100^0C	

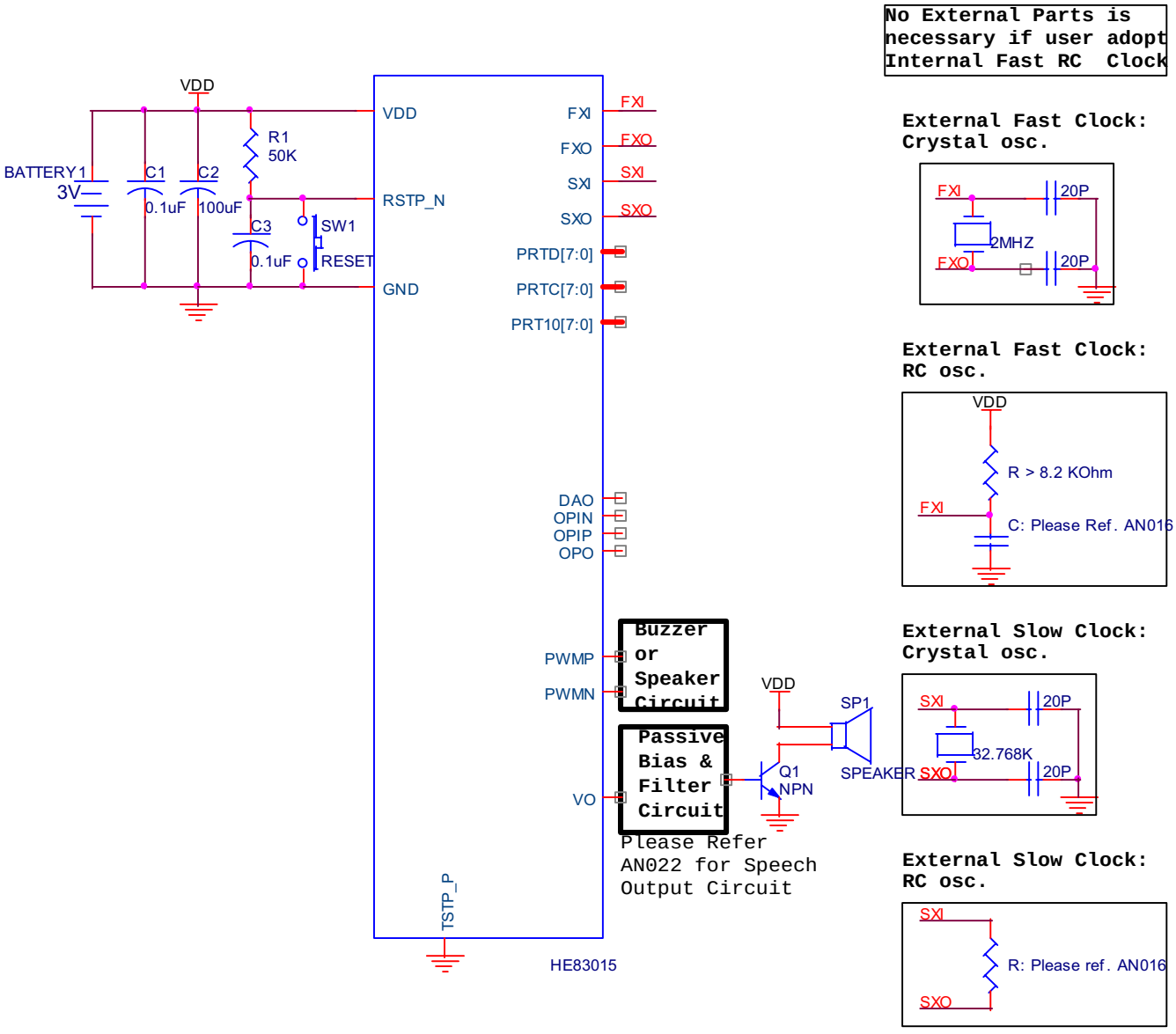
Test Condition: TEMP=25℃, VDD=3V+/-10%, GND=0V

	PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
I_{Fast}	NORMAL Mode Current	System	2M ext. R/C		0.75	1	mA
I_{Slow}	SLOW Mode Current	System	32.768K X'tal		6	9	μA
I_{Idle}	IDLE Mode Current	System	32.769K X'tal		4	7	μA
I_{Sleep}	Sleep Mode Current	System				1	μA
I_{oHPWM}	PWM Output Drive Current	PWMP, PWMN*2	V_{DD}=3V; V_{oh}=2V	12	15		mA
I_{oLPWM}	PWM Output Sink Current	PWMP, PWMN*2	V_{DD}=3V; V_{oL}=1V	33	40		mA
I_{oVO}	DAC Output Current	VO, DAO	V_{DD}=3V;VO=0~2V,Data=7F	2.5	3		mA
V_{iH}	Input High Voltage	I/O pins		0.8 V_{DD}			V
V_{iL}	Input Low Voltage	I/O pins				0.2 V_{DD}	V
V_{hys}	Input Hysteresis Width	I/O, RSTP_N	Threshold=2/3V_{DD}(input from low to high) Threshold=1/3V_{DD}(input from high to low)		1/3 V_{DD}		V
I_{oH}	Output Drive Current	I/O pull-high*1	V_{oL}=2.0V	50			μA
I_{oL_1}	Output Sink Current	I/O pull-low*1	V_{oL}=0.4V	1.0			mA
I_{iL_1}	Input Low Current	RSTP_N	V_{iL}=GND, pull high Internally		20		μA
I_{iL_2}	Input Low Current	I/O	V_{iL}=GND, if pull high Internally by user		100		μA

Note: *1: Drive Current Spec. for Push-Pull I/O port only
Sink Current Spec. for both Push-Pull and Open-Drain I/O port.

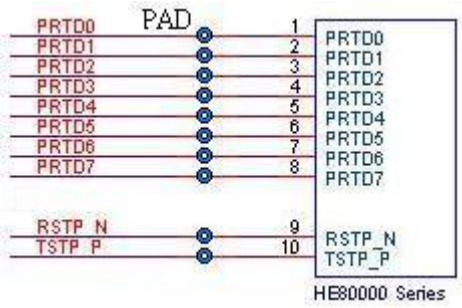
*2: This Spec. base on one driver only. There are five build-in driver, so user just multiply the number of driver he used to one driver current to get the total amount of current. (I_{oHPWM}、I_{oLPWM} * N; N=0,1,2,3,4,5)

H. Application Circuit



I. Important Note

1. For accessing any address large than 64KB, users must update TPP first, TPH then TPL. Only by this order, the pre-charge circuit of ROM will work correctly. 5us waiting is necessary before LDV instruction is executed since Data ROM is a low speed ROM. Users can not emulate this accessing process in ICE. So 5us delay should be added by firmware.
2. Please bonds the TSTP_P, RSTP_N and PRTD[7:0] with test point on PCB (can be soldered and probed) as you can, then KB can do some IC testing job on PCB. Neither VDD nor GND connection is necessary for TSTP_P. The following figure is an example (Testing point with through hole).



J. Updated Record

Version	Date	Section	Original Content	New Content
V3.2	Dec 25,2001	B, H	2.2V (VDD operation voltage)	2.4V
		C,I		New Section