AKD5384
AK5384 Evaluation Board Rev.A

GENERAL DESCRIPTION

AKD5384 is an evaluation board for the digital audio 24bit 96kHz 4ch A/D converter, AK5384. The AKD5384 includes the input circuit and also has a digital interface transmitter. Further, the AKD5384 can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD5384 --- AK5384 Evaluation Board

FUNCTION

- **DIT with optical output**
- **BNC connector for an external clock input**

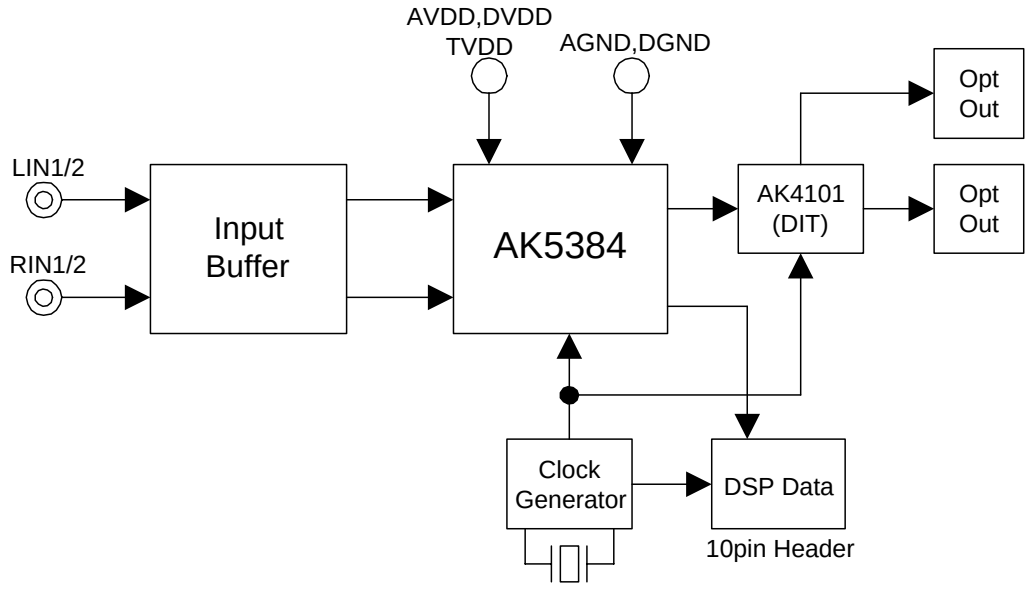


Figure 1. AKD5384 Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

■ Operation sequence

1) Set up the power supplies lines.

[AVDD]	(red)	= 4.75 ~ 5.25V	: for AVDD of AK5384 (typ. 5.0V)
[DVDD]	(red)	= 4.75 ~ 5.25V	: for DVDD of AK5384 (typ. 5.0V)
[TVDD]	(orange)	= 3.0 ~ 5.25V	: for TVDD of AK5384 (typ. 5.0V)
[+15V]	(green)	= +15V	: for Op-amp
[–15V]	(blue)	= –15V	: for Op-amp
[VCC]	(red)	= 5V	: for logic
[AGND]	(black)	= 0V	: for analog ground
[DGND]	(black)	= 0V	: for logic ground

Each supply line should be distributed from the power supply unit.

2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

3) Power on.

The AK5384 and AK4101 should be reset once bringing SW1 = "L" upon power-up.

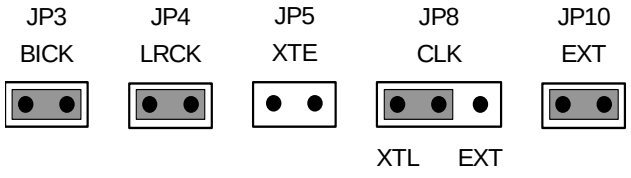
Note: When the AK5384 is TDM mode, the AK4101 does not support TDM mode. So, PORT1 (DIT1) and PORT2 (DIT2) are not used. PORT3 (DSP) should be used.

■ Evaluation mode

(1) Slave Mode

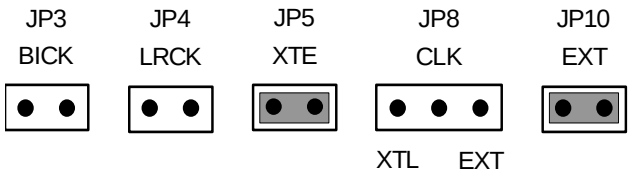
(1-1) A/D evaluation using DIT function of AK4101

PORT1 (DIT1) and PORT2 (DIT2) are used. DIT generates audio bi-phase signal from received data and which is output through optical connector (TOTX176). It is possible to connect AKM's D/A converter evaluation boards on the digital-amplifier, which equips DIR input. Nothing should be connected to PORT3 (DSP). In case of using external clock through a BNC connector (J5), select EXT on JP8 (CLK) and short JP5 (XTE) and open JP10 (EXT).



(1-2) Feeding all clocks from PORT3 (DSP)

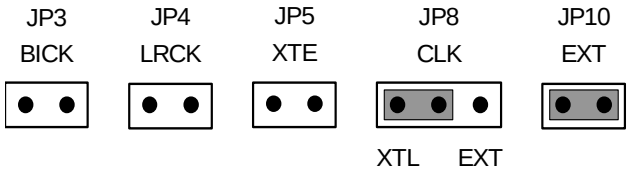
Under the following set-up, all external clocks (MCLK, BICK, LRCK) can be fed through PORT3 (DSP). The A/D converted data is output from SDTO1/SDTO2 of PORT3 (DSP). Also, the A/D converted data is output through optical connector (TOTX176).



(2) Master Mode

(2-1) A/D evaluation using DIT function of AK4101

PORT1 (DIT1) and PORT2 (DIT2) are used. DIT generates audio bi-phase signal from received data and which is output through optical connector (TOTX176). It is possible to connect AKM's D/A converter evaluation boards on the digital-amplifier, which equips DIR input. Nothing should be connected to PORT3 (DSP). In case of using external clock through a BNC connector (J5), select EXT on JP8 (CLK) and short JP5 (XTE) and open JP10 (EXT).



■ Other jumper pins set up

1. JP1 (GND) : Analog ground and Digital ground
   OPEN : Separated.
   SHORT : Common. (The connector "DGND" can be open.) <Default>

2. JP2 (AVDD) : Select AVDD for AK5384
   AVDD : Supply from AVDD connector <Default>
   REG : Supply from regulator. AVDD connector should be supplied +15V.

3. JP6 (BCFS) : Select BICK frequency
   64 : In case of MCLK=256fs/512fs/768fs <Default>
   128 : In case of MCLK=384fs or BICK frequency of TDM128 mode
   256 : BICK frequency of TDM256 mode

4. JP7 (MCLK) : Supply MCLK frequency for 74HC4040
   256 : In case of MCLK=256fs
   512 : In case of MCLK=512fs <Default>
   384/768 : In case of MCLK=384fs/768fs

5. JP9 (LRFS) : Select LRCK frequency
   256 : In case of MCLK=256fs/512fs/768fs <Default>
   384 : In case of MCLK=384fs

■ Clock Setting

Mode	fs	MCLK	JP6(BCFS)	JP7(MCLK)	JP9(LRFS)	
Normal	8kHz	256fs = 2.048MHz	64	256	256	
		384fs = 3.072MHz	128	384/768	384	
		512fs = 4.096MHz	64	512	256	
		768fs = 6.144MHz	64	384/768	256	
	32kHz	256fs = 8.192MHz	64	256	256	
		384fs = 12.288MHz	128	384/768	384	
		512fs = 16.384MHz	64	512	256	
		768fs = 24.576MHz	64	384/768	256	
	44.1kHz	256fs = 11.2896MHz	64	256	256	
		384fs = 16.9344MHz	128	384/768	384	
		512fs = 22.5792MHz	64	512	256	
		768fs = 33.8688MHz	64	384/768	256	
	48kHz	256fs = 12.288MHz	64	256	256	
		384fs = 18.432MHz	128	384/768	384	
		512fs = 24.576MHz	64	512	256	Default
		768fs = 36.864MHz	64	384/768	256	
	88.2kHz	256fs = 22.5792MHz	64	256	256	
		384fs = 33.8688MHz	128	384/768	384	
	96kHz	256fs = 24.576MHz	64	256	256	
		384fs = 36.864MHz	128	384/768	384	
TDM256	8kHz	512fs = 4.096MHz	256	512	256	
	32kHz	512fs = 16.384MHz	256	512	256	
	44.1kHz	512fs = 22.5792MHz	256	512	256	
	48kHz	512fs = 24.576MHz	256	512	256	
TDM128	8kHz	256fs = 2.048MHz	128	256	256	
		512fs = 4.096MHz	128	512	256	
	32kHz	256fs = 8.192MHz	128	256	256	
		512fs = 16.384MHz	128	512	256	
	44.1kHz	256fs = 11.2896MHz	128	256	256	
		512fs = 22.5792MHz	128	512	256	
	48kHz	256fs = 12.288MHz	128	256	256	
		512fs = 24.576MHz	128	512	256	
	88.2kHz	256fs = 22.5792MHz	128	256	256	
	96kHz	256fs = 24.576MHz	128	256	256	

Table 1. Clock Setting

■ DIP Switch set up

[SW2] (MODE): Setting the evaluation mode for AK5384 and AK4101
ON is "H", OFF is "L".

No.	Name	OFF ("L")	ON ("H")	Default
1	DIF	MSB justified	I^2S Compatible	OFF ("L")
2	TDM1	See Table 3		OFF ("L")
3	TDM0			OFF ("L")
4	M/S	Slave mode	Master mode	OFF ("L")
5	CKS	MCLK = 256fs	MCLK = 512fs	ON ("H")
6	CKS1	See Table 4		ON ("H")
7	CKS0			OFF ("L")

Table 2. Mode Setting

TDM1	TDM0	Mode	BICK	
L	L	Normal	48 ~ 128fs	Default
L	H	TDM256	256fs	
H	L	N/A	N/A	
H	H	TDM128	128fs	

Table 3. Mode Setting of AK5384

Mode	CKS1	CKS0	MCLK	fs	
0	L	L	256fs	~ 96kHz	
1	L	H	N/A	N/A	
2	H	L	512fs	~ 48kHz	Default
3	H	H	384fs	~ 48kHz	

Table 4. MCLK Frequency Setting of AK4101

Note: AK4101 does not support MCLK=768fs.

■ The function of the toggle SW

Upper-side is "H" and lower-side is "L".

[SW1] (PDN): Resets the AK5384 and AK4101. Keep "H" during normal operation.

■ Input Circuit

Analog signal is input to LIN1-2/RIN1-2 pins via J1 ~ J4 connectors.
R11, R18, R25 and R32 should be changed depending on the output impedance of signal source.

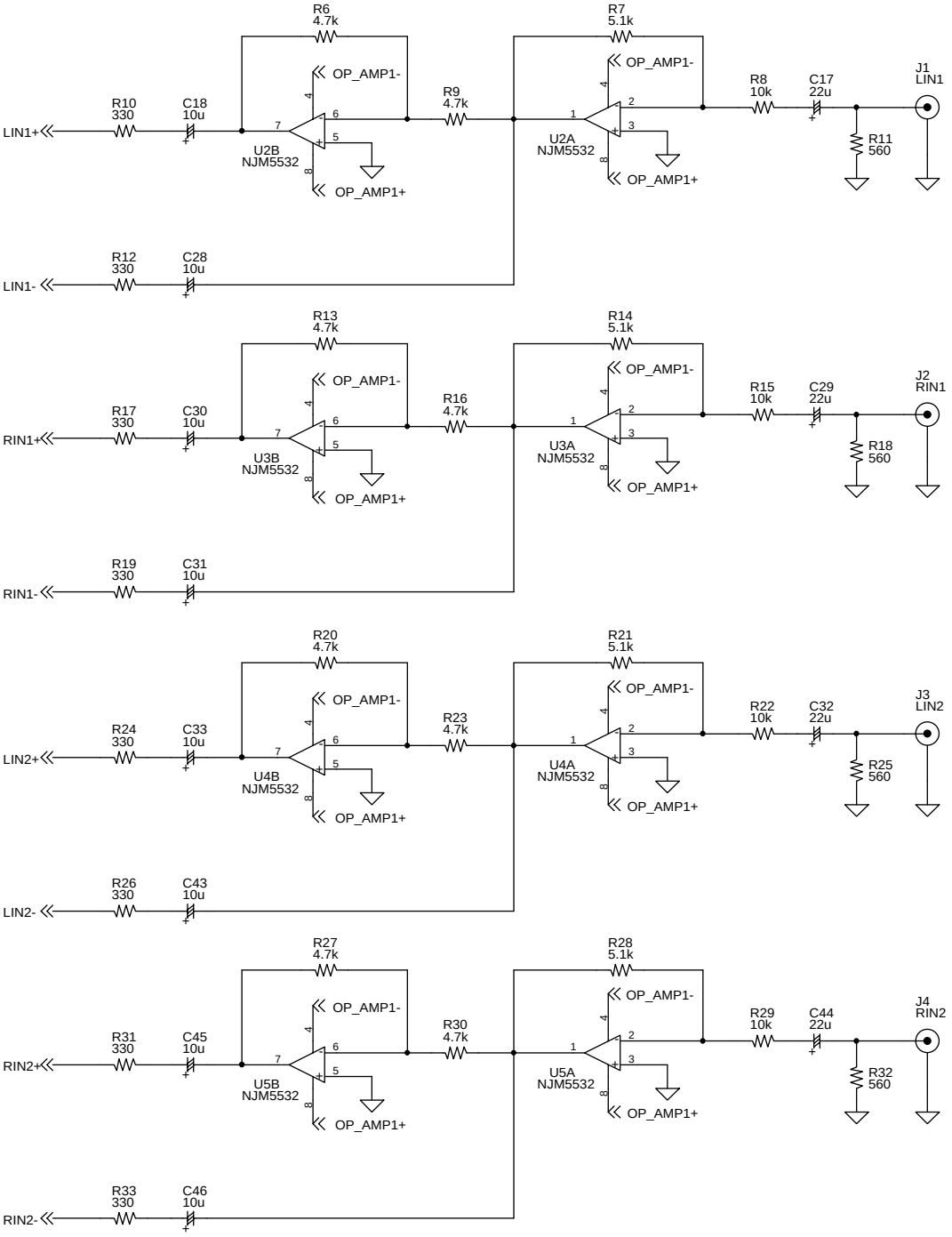


Figure 2. LIN1-2/RIN1-2 Input circuits

* AKM assumes no responsibility for the trouble when using the circuit examples.

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit : Audio Precision, System Two Cascade
- MCLK : 256fs
- BICK : 64fs
- fs : 48kHz, 96kHz
- Bit : 24bit
- Power Supply : AVDD = DVDD = TVDD = 5.0V
- Interface : DIT
- Temperature : Room

[Measurement Results]

Parameter	Result		Unit
ADC Analog Input Characteristics	LIN1 / RIN1	LIN2 / RIN2	
S/(N+D)			
(fs=48kHz, –1dBFS)	100.8 / 100.7	101.3 / 101.2	dB
(fs=96kHz, –1dBFS)	96.4 / 95.1	95.4 / 94.4	dB
D-Range			
(fs=48kHz, –60dBFS, A-weighted)	107.6 / 107.5	107.6 / 107.4	dB
(fs=96kHz, –60dBFS)	102.4 / 102.4	102.4 / 102.4	dB
S/N			
(fs=48kHz, A-weighted)	107.6 / 107.5	107.6 / 107.4	dB
(fs=96kHz)	102.4 / 102.4	102.4 / 102.4	dB
Interchannel Isolation	119.5 / 122.4	120.5 / 124.0	dB

[ADC Plot : fs=48kHz]

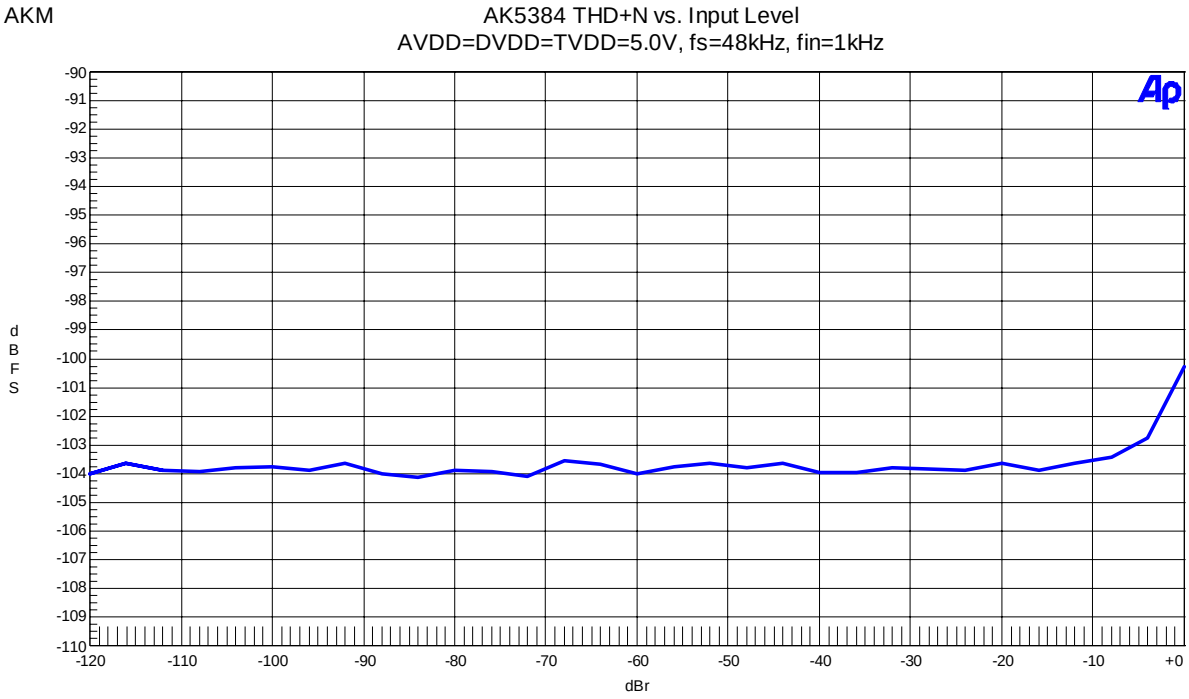


Figure 1. THD+N vs. Input Level

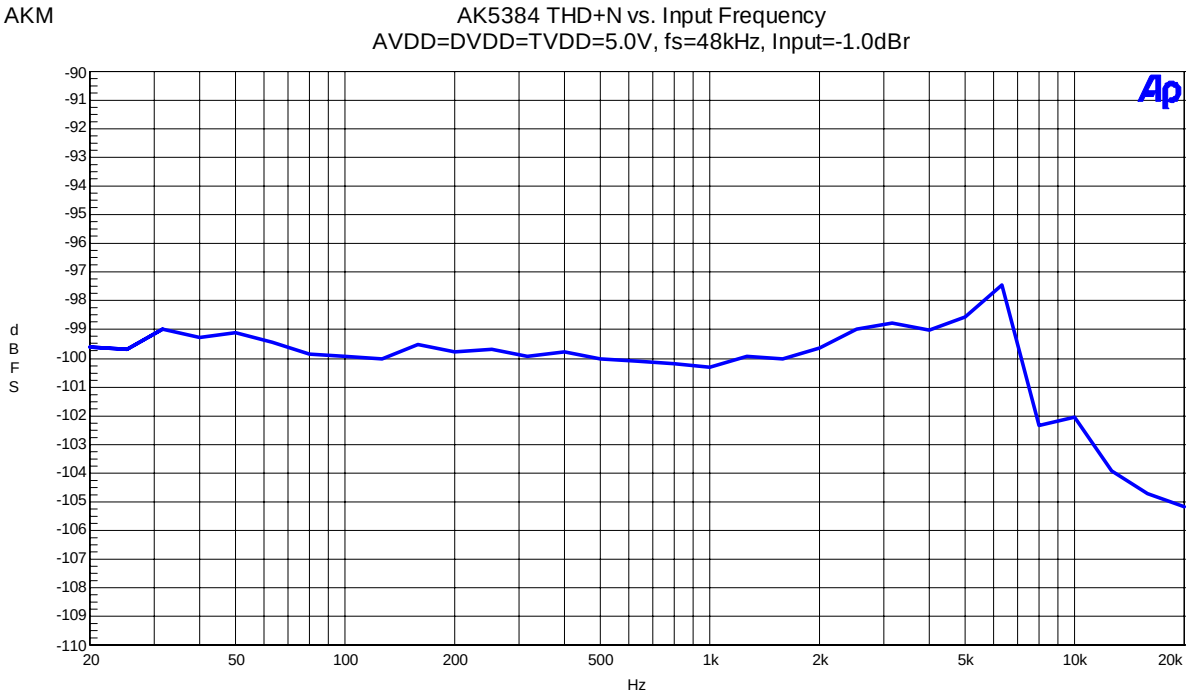


Figure 2. THD+N vs. Input Frequency

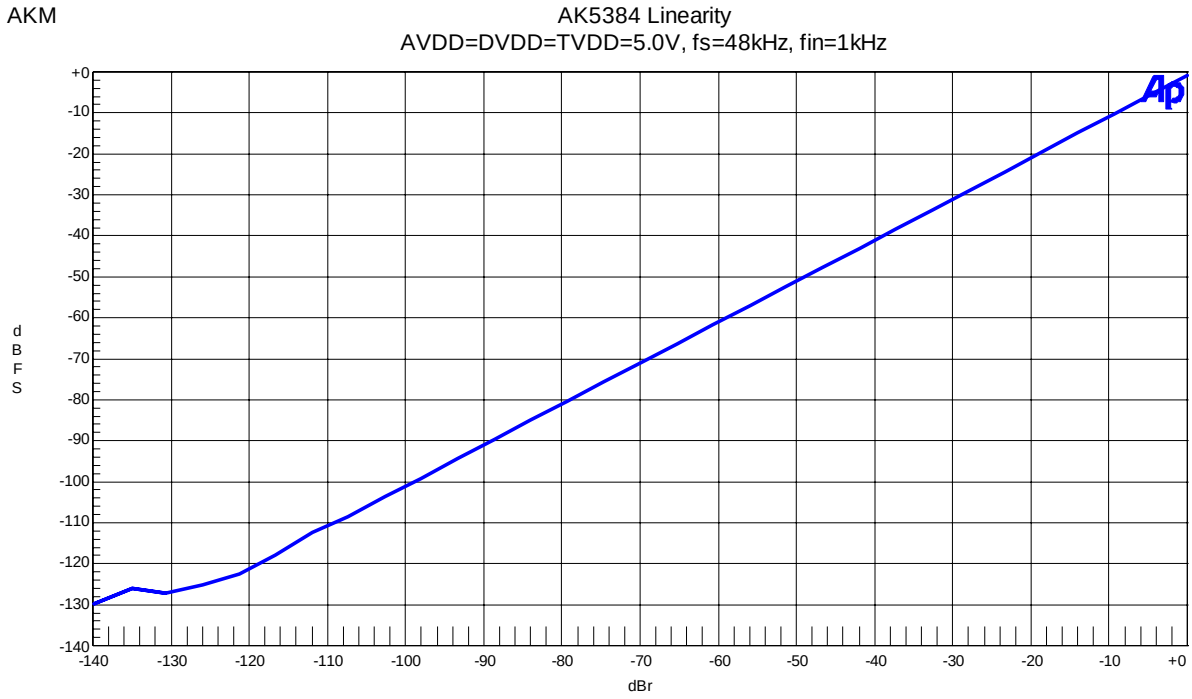


Figure 3. Linearity

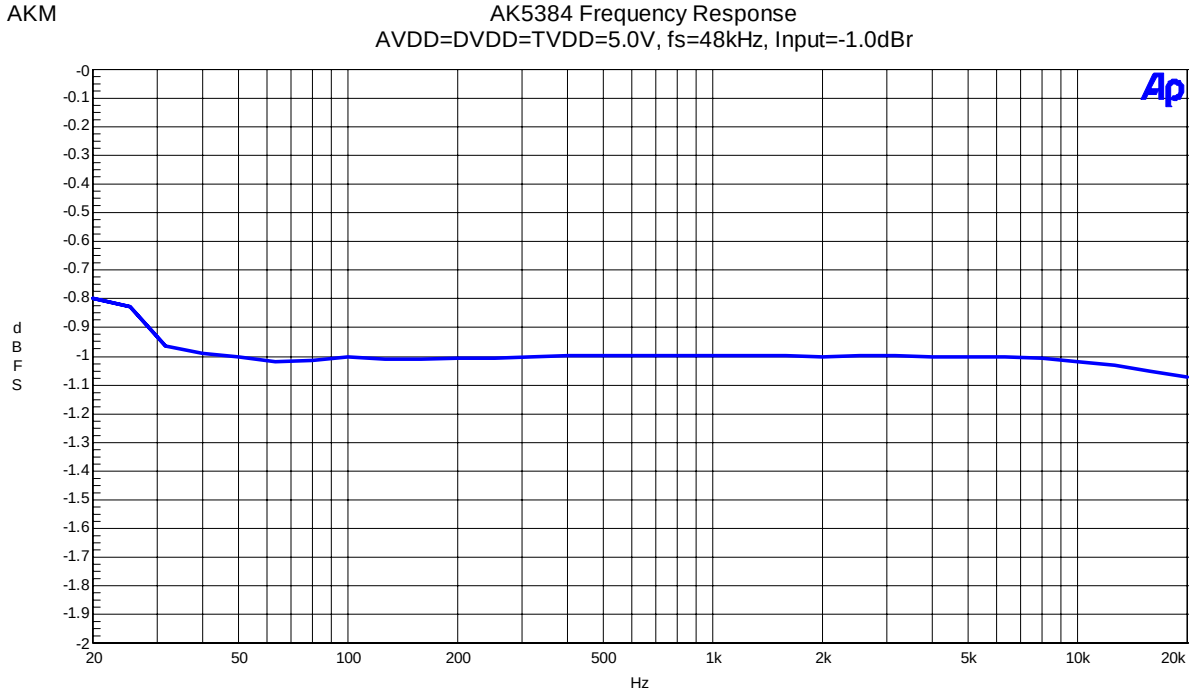


Figure 4. Frequency Response

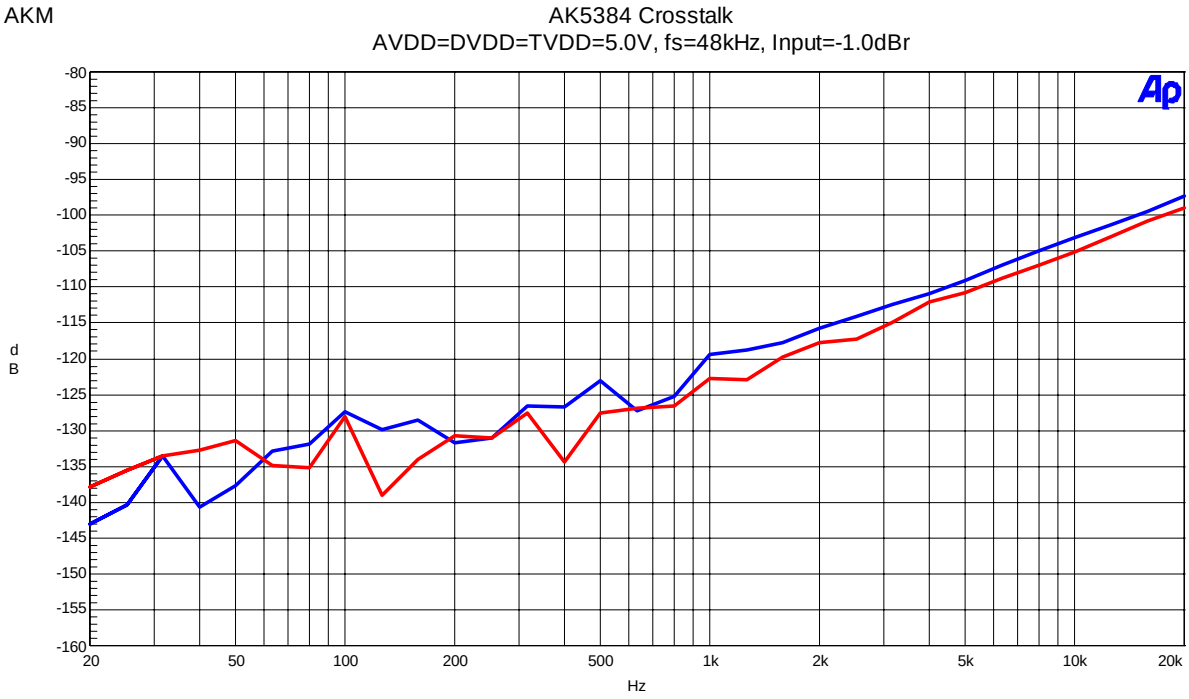


Figure 5. Crosstalk

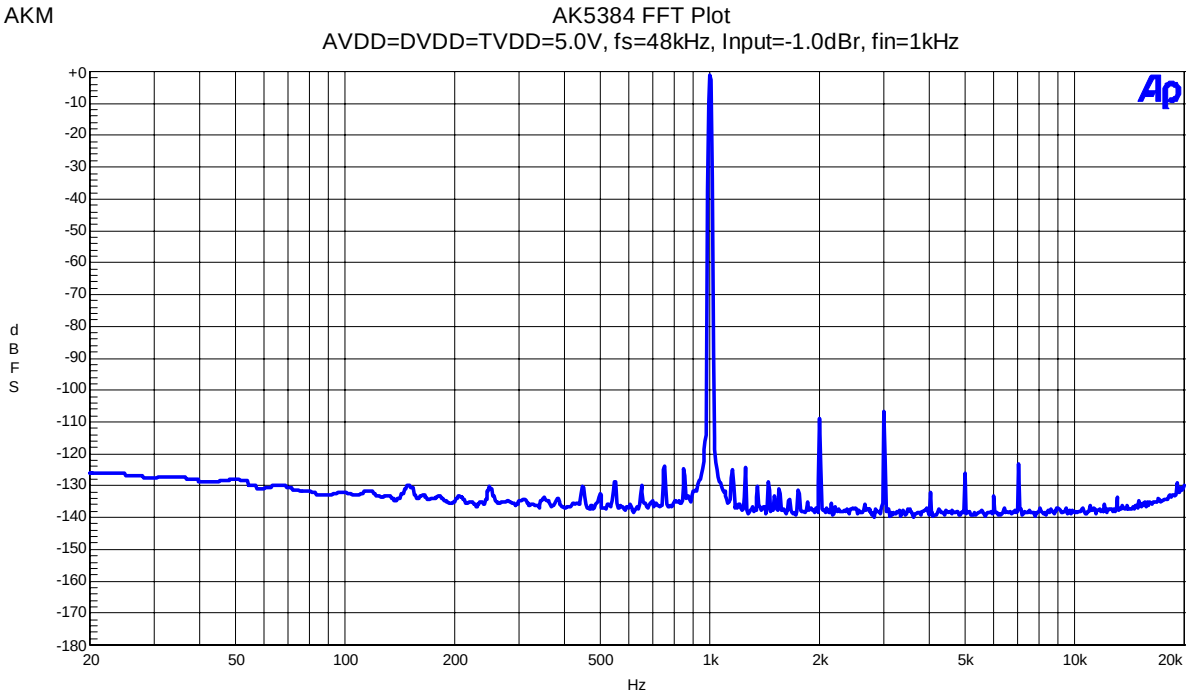


Figure 6. FFT Plot

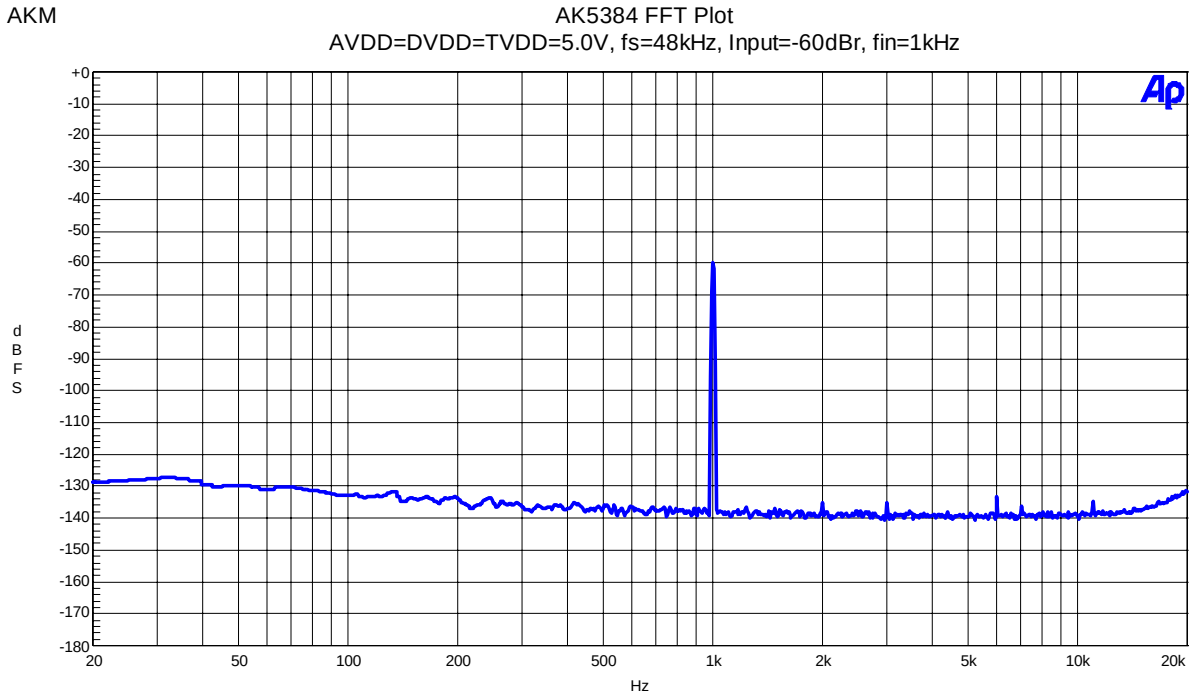


Figure 7. FFT Plot

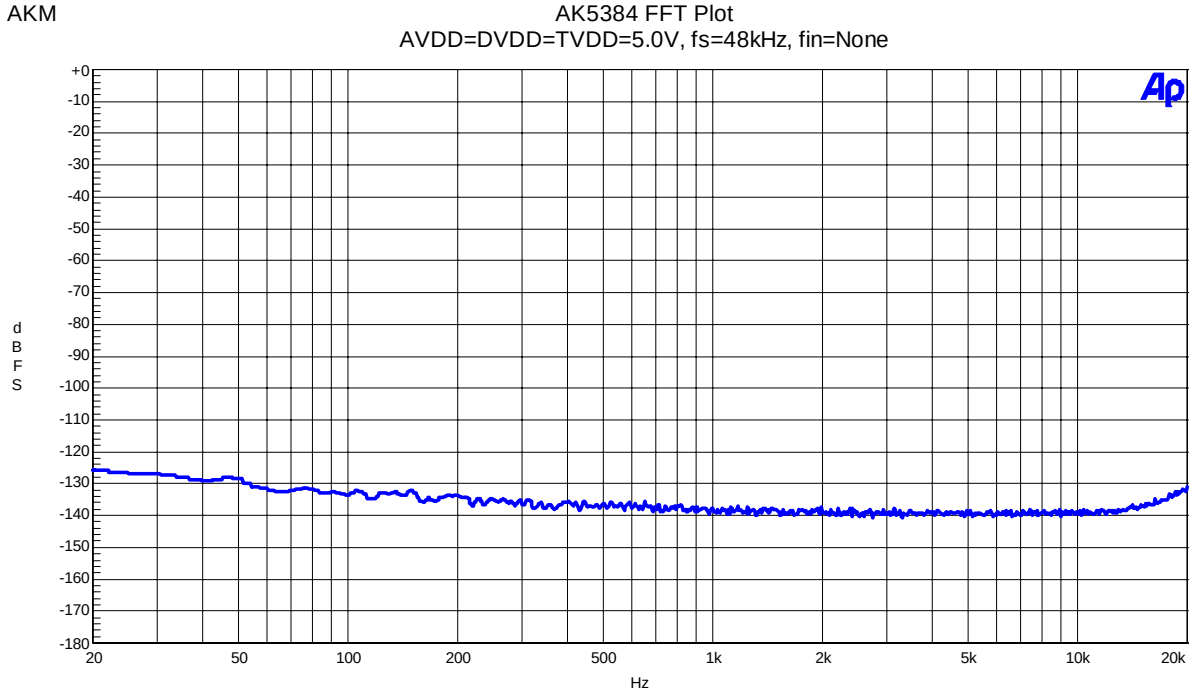


Figure 8. FFT Plot

[ADC Plot : fs=96kHz]

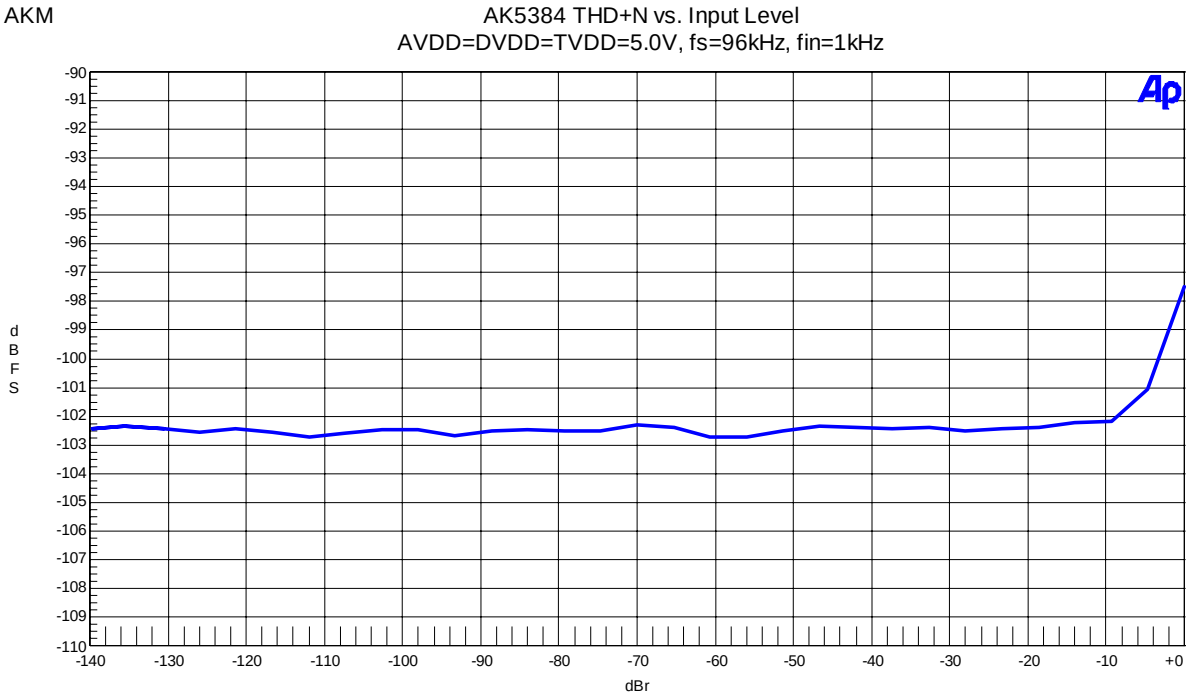


Figure 9. THD+N vs. Input Level

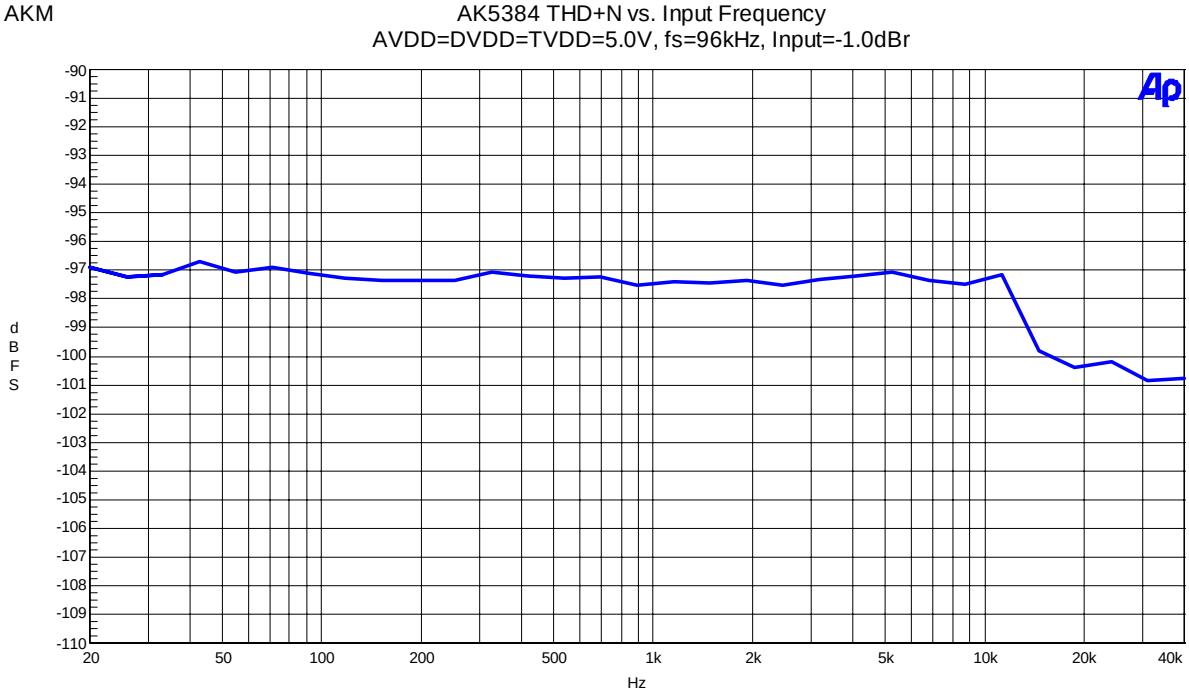


Figure 10. THD+N vs. Input Frequency

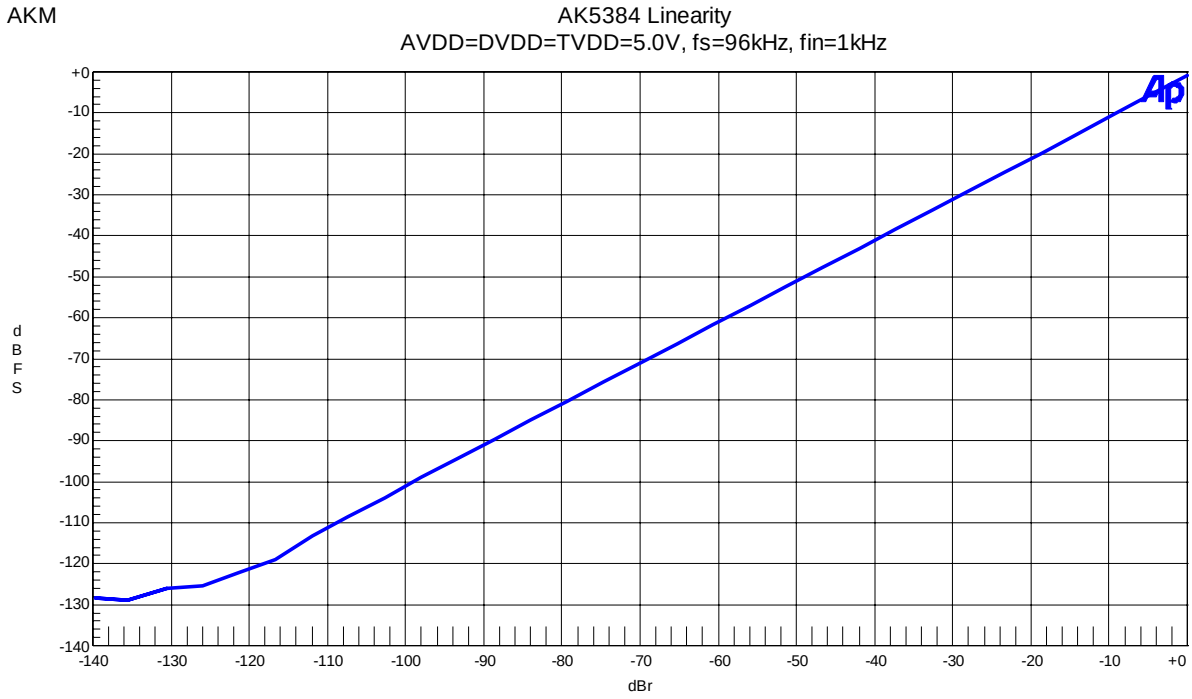


Figure 11. Linearity

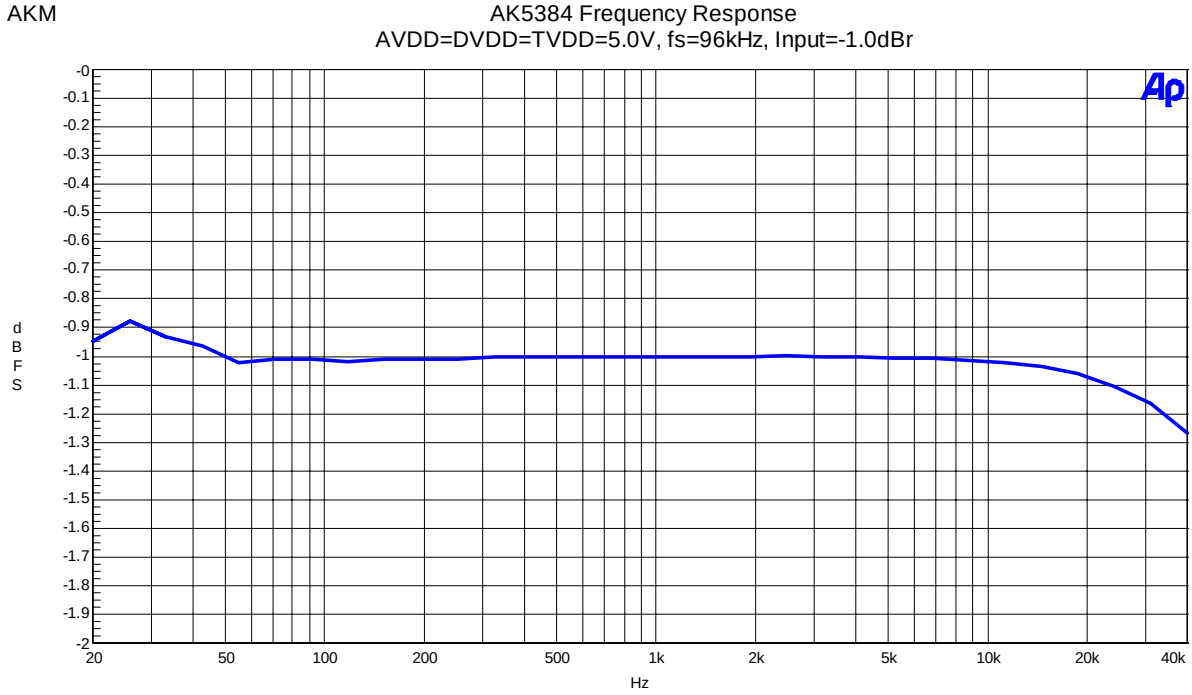


Figure 12. Frequency Response

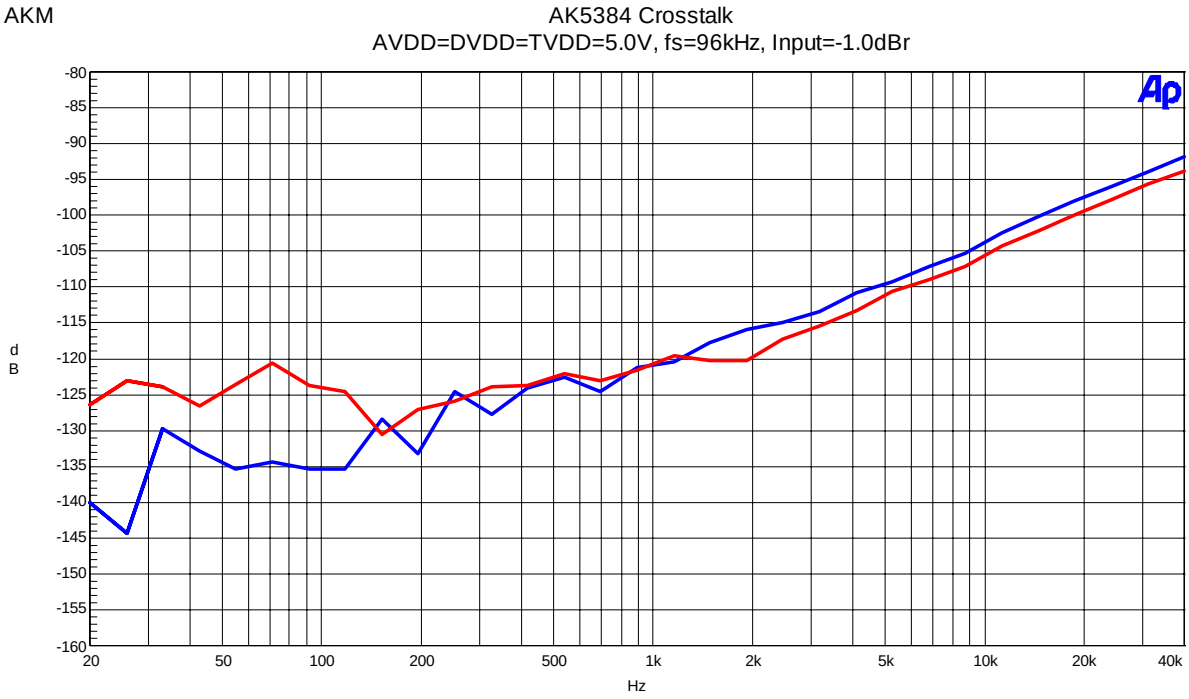


Figure 13. Crosstalk

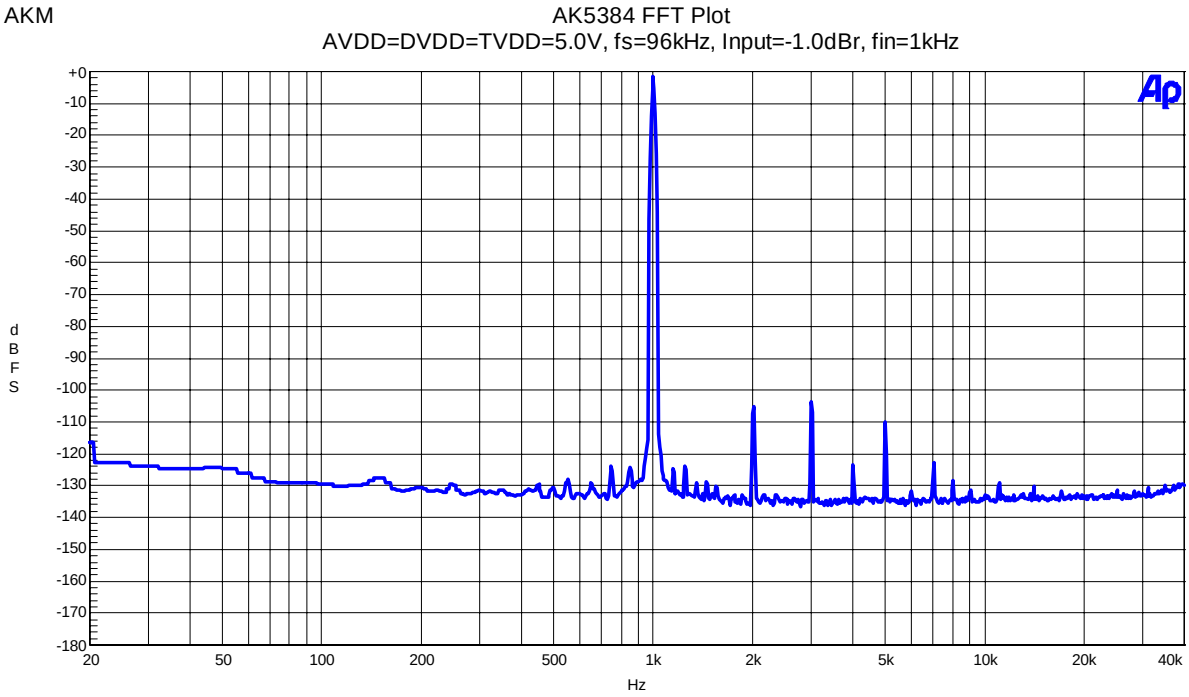


Figure 14. FFT Plot

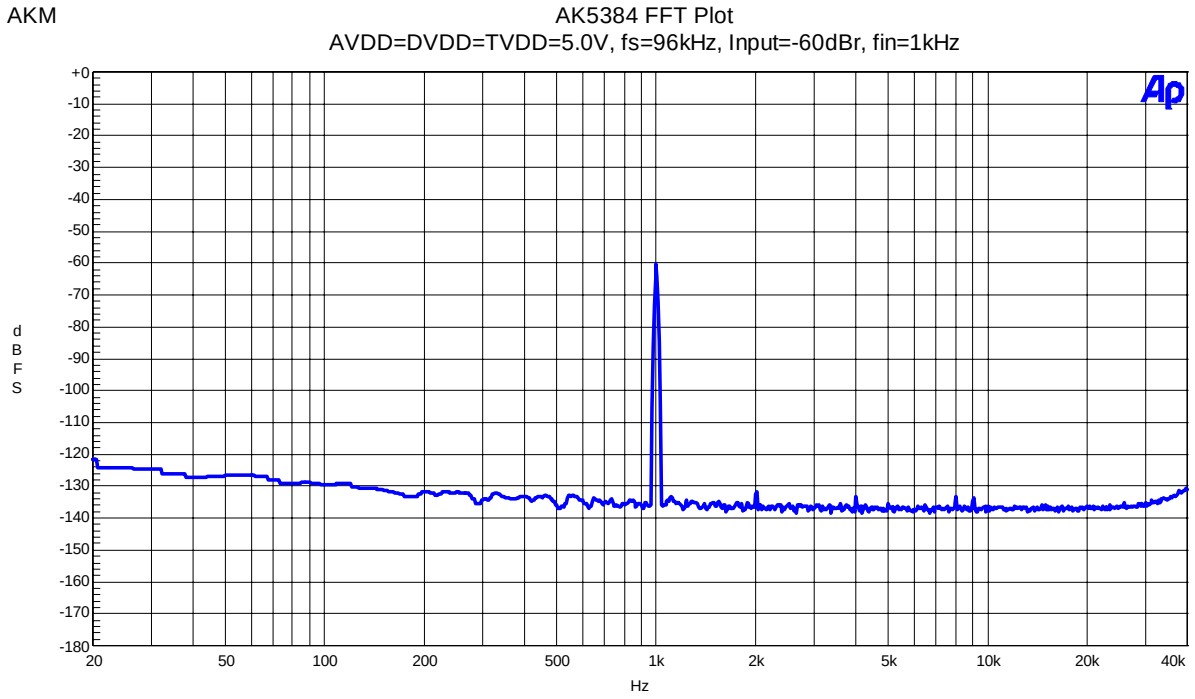


Figure 15. FFT Plot

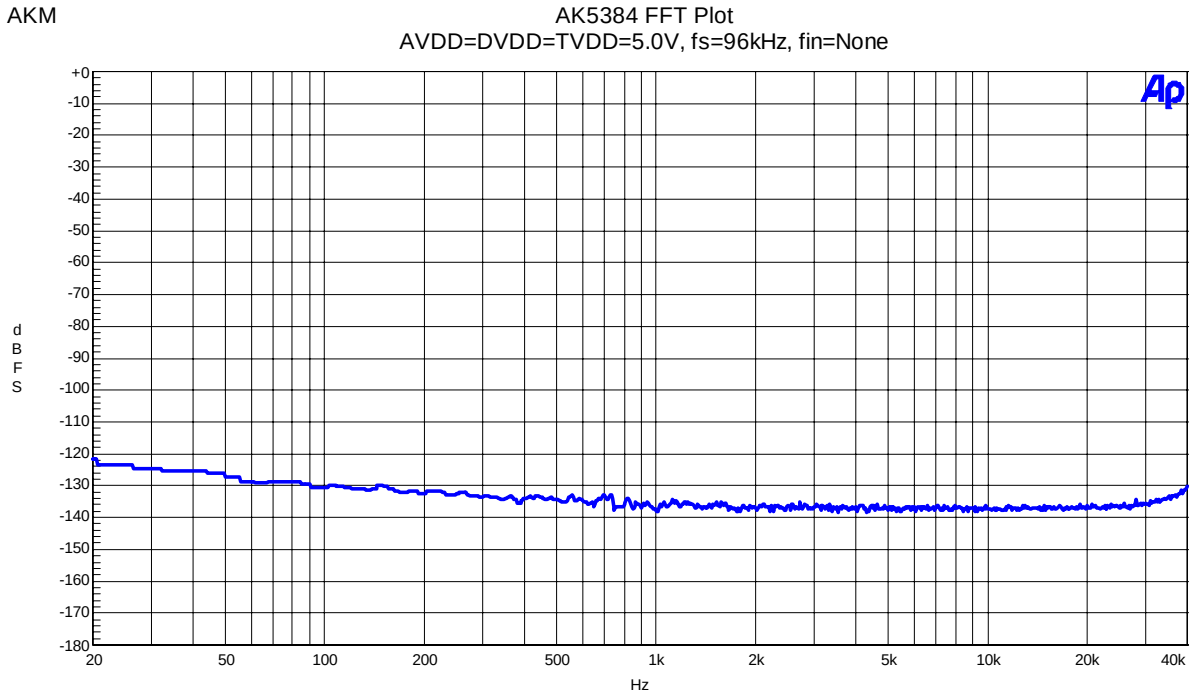


Figure 16. FFT Plot

Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
02/11/01	KM070100	0	First edition	
05/10/17	KM070101	1	Circuit Change	Condenser: Capacitance Value Change: C57,C58: open → 5p

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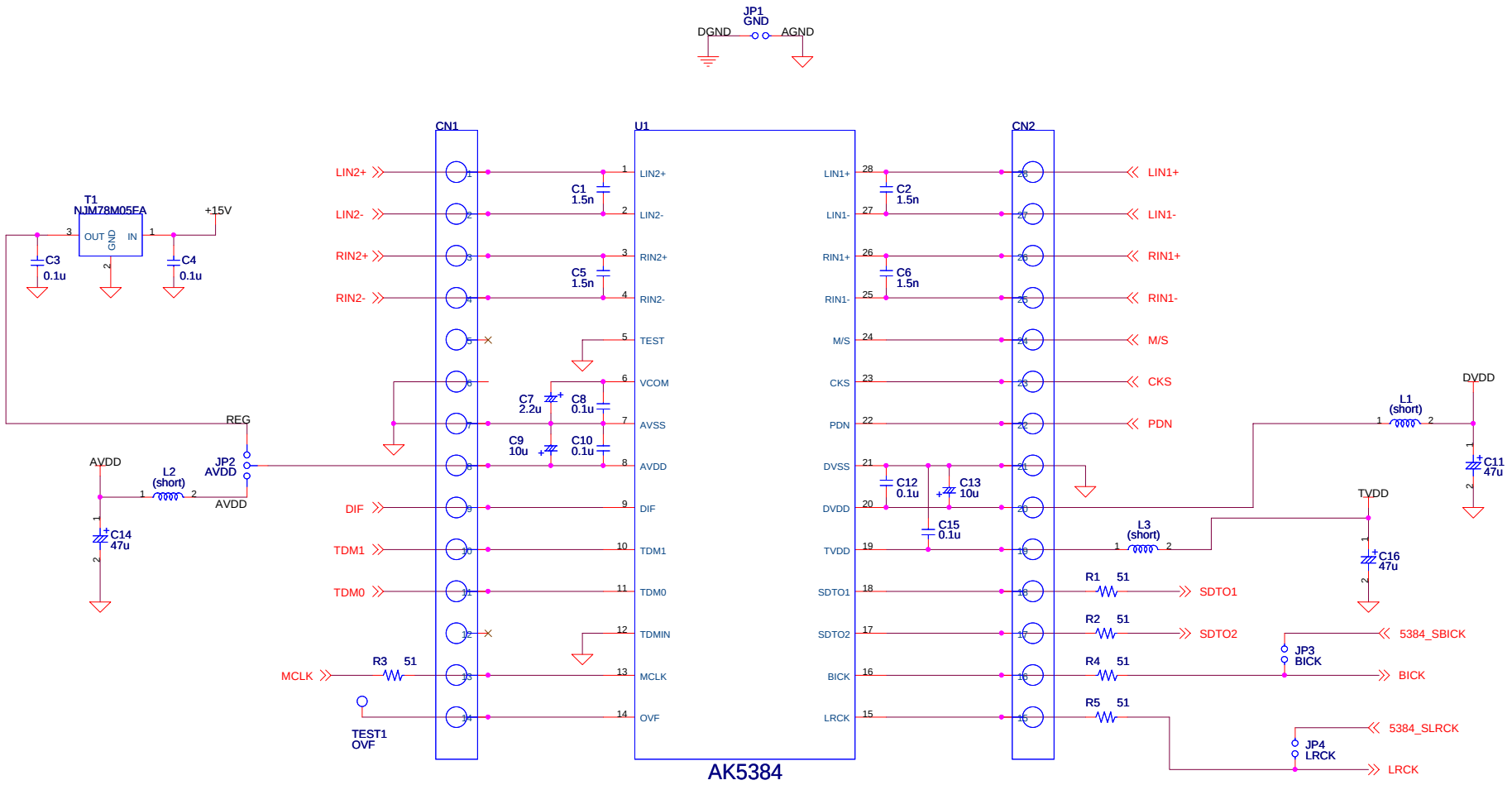

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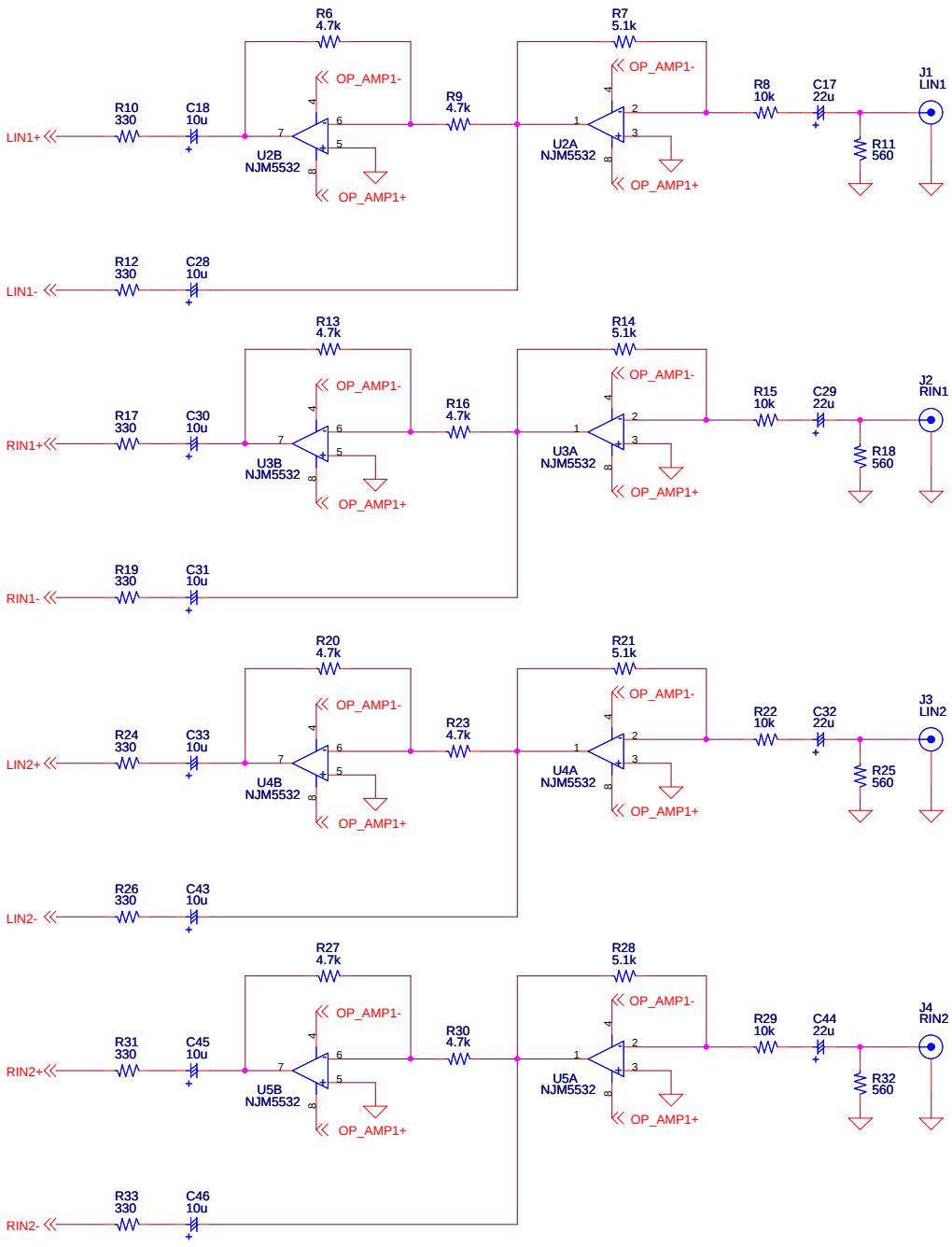

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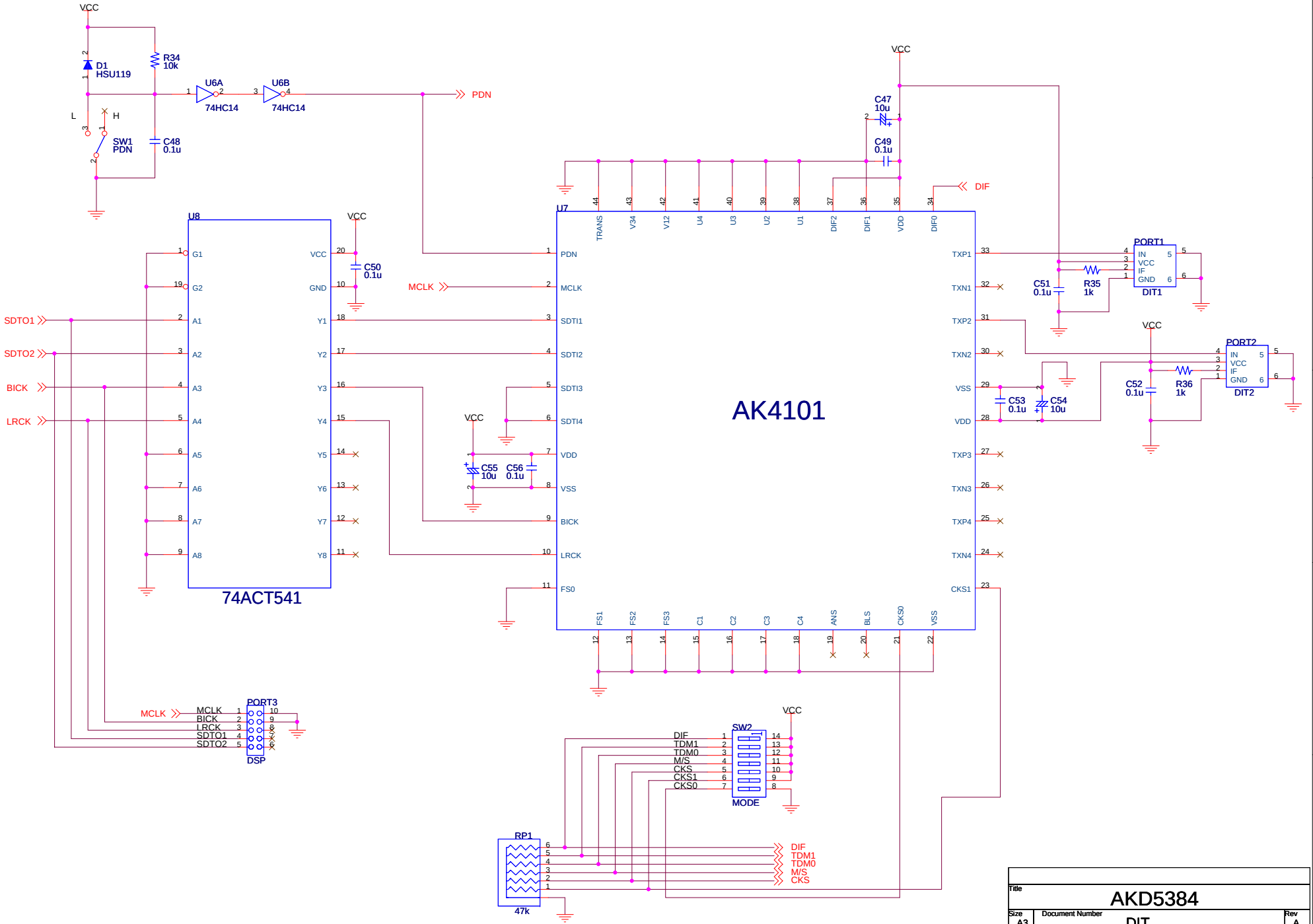

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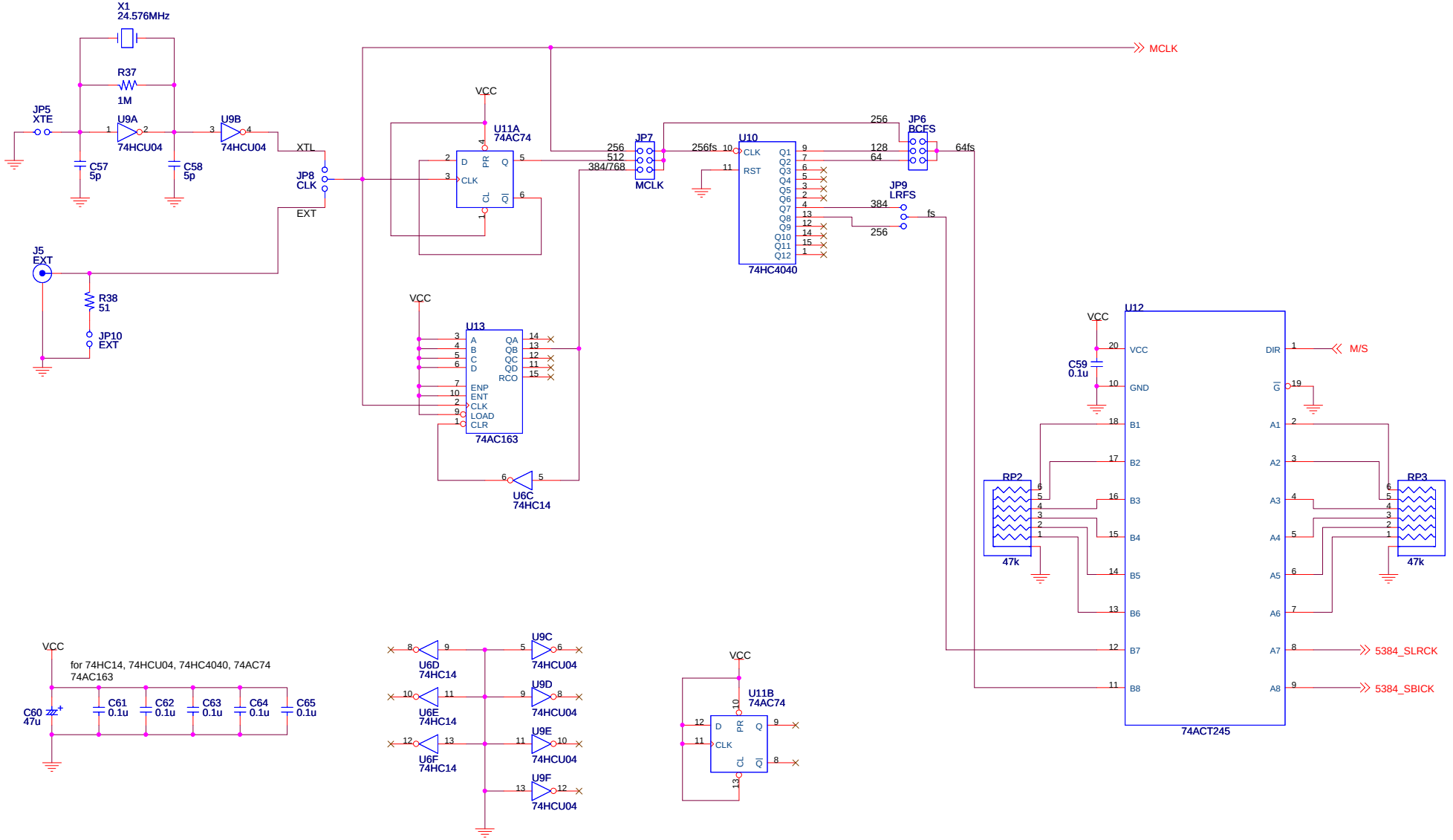

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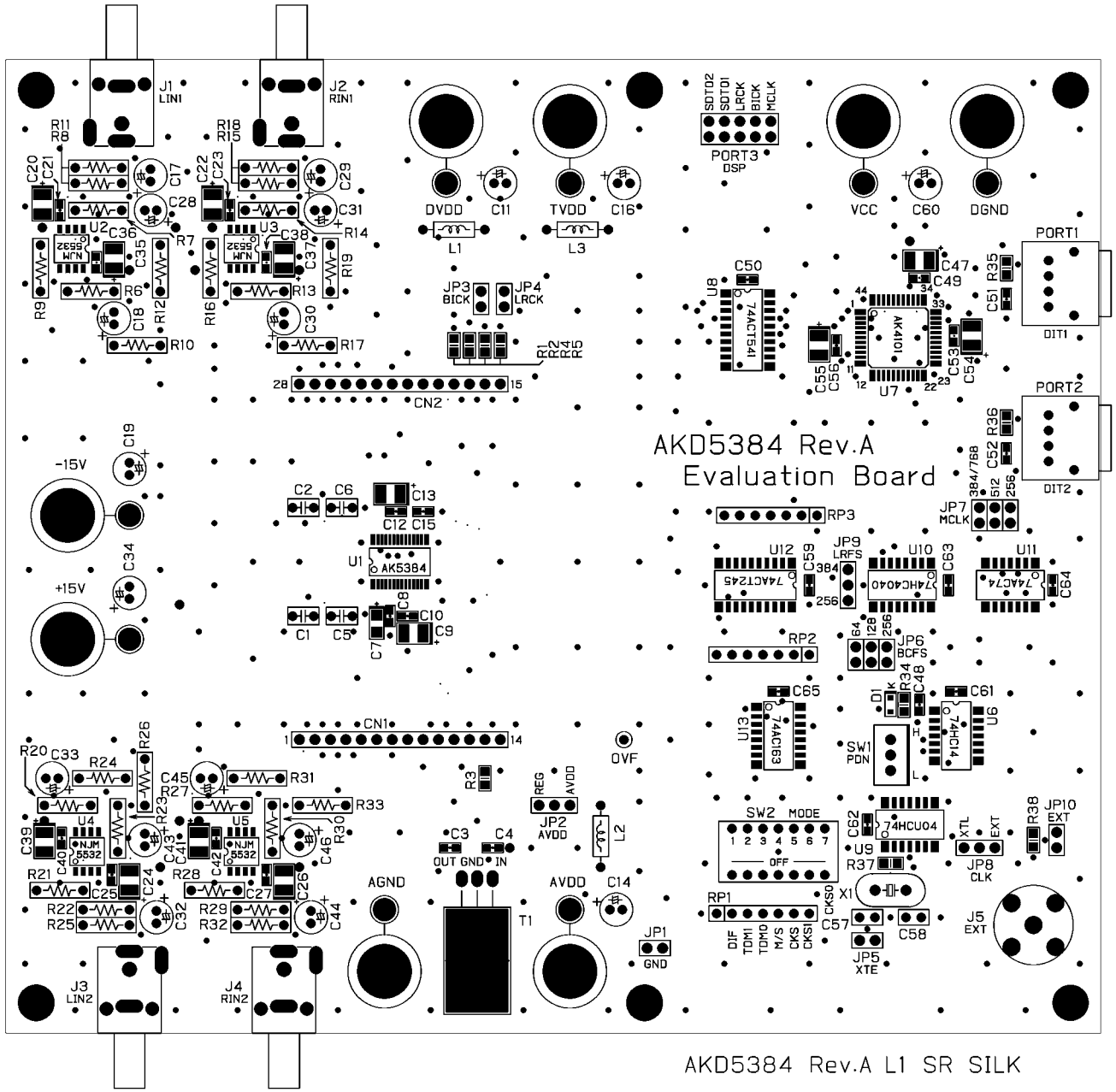
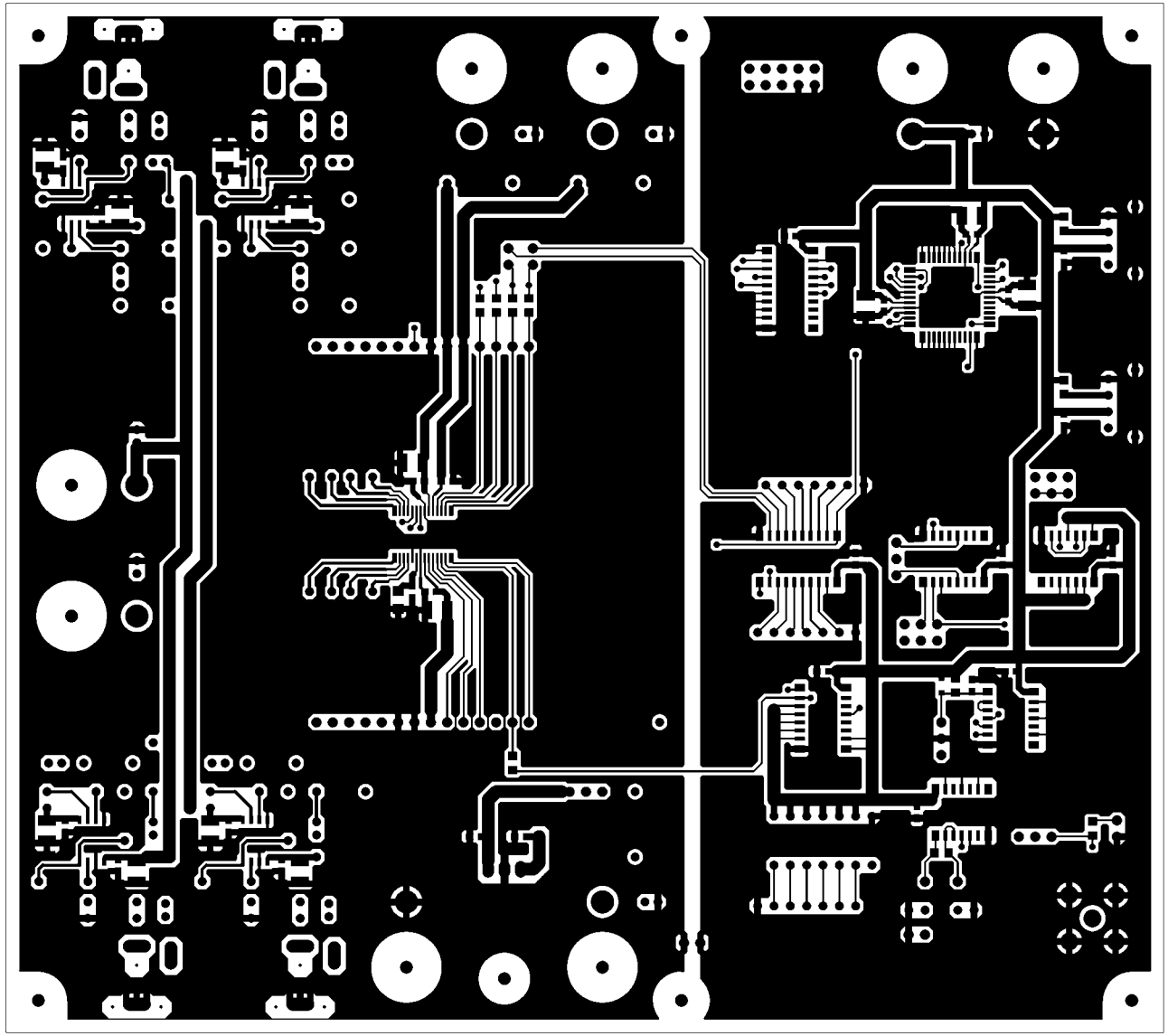


AKD5384 Rev.A L1 SR SILK



AKD5384 Rev.A L1

AKD5384 Rev.A L2