AKD4682-A
AK4682 Evaluation Board Rev.0

FEATURE

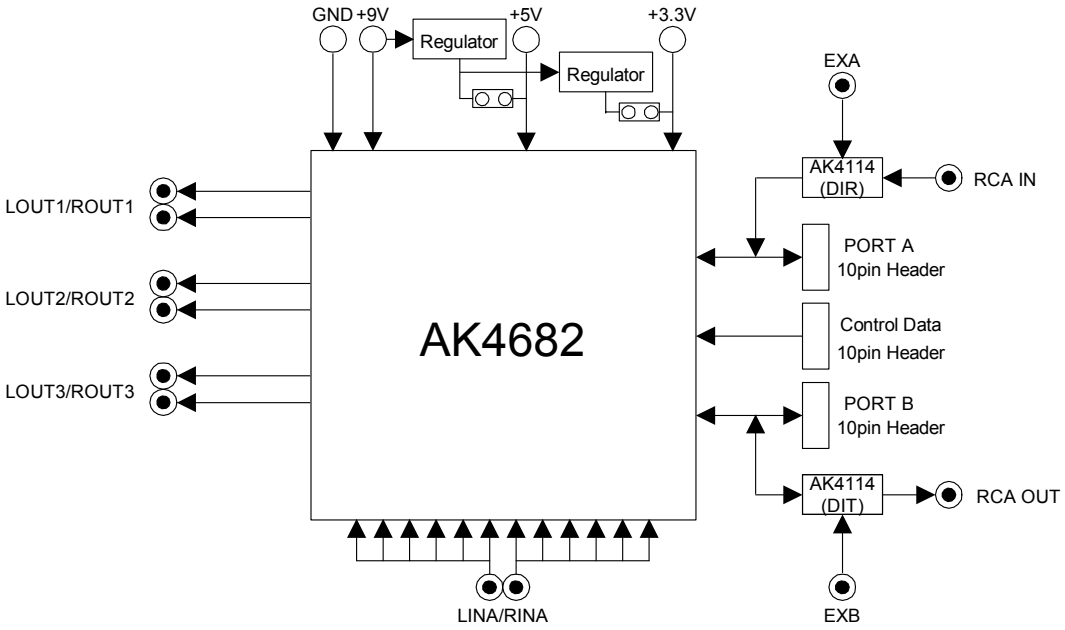
AKD4682-A is an evaluation board for AK4682, a single chip 24bit CODEC that has two channels of ADC and four channels of DAC. This board has interfaces with AKM's evaluation boards for A/D converter and D/A converter and makes easy to evaluate AK4682. Also this board has the digital audio interface and then achieves the interface with digital audio systems via RCA connector.

■ **Ordering guide**

AKD4682-A --- AK4682 Evaluation Board
10 wire flat cable for connection with printer port of PC (IBM-AT compatible machine), control software for AK4682, driver for control software on Windows 2000/XP are packed with this.
Control software does not work on Windows NT
Windows 2000/XP needs an installation of driver.
Windows 95/98/ME does not need an installation of driver.

FUNCTION

- ☐ **On-board clock generators (AK4114 x2)**
- ☐ **Compatible with 2 types of digital audio interface**
  - **RCA (S/PDIF) input/output**
  - **10pin headers for interfacing with external data source (x2)**
- ☐ **RCA connectors for clock input with external clock source**
- ☐ **10pin headers for register control**



(Note) Each AK4114 integrates DIR, DIT and X'tal oscillator.
Figure 1. AKD4682-A Block Diagram
(* Circuit diagram and PCB layout are attached at the end of this manual.)

EVALUATION BOARD MANUAL

■ Operating sequence

1. Set up power supply lines.

Name of Jack	Color of Jack	Voltage	Used for	Comment and attention	Default
AVDD1	Orange	+4.5~+5.5V	AVDD1 and DVDD1 of AK4682	Should be always connected when JP25 (AVDD1_SEL) is set to AVDD1 side. Can be open when JP25 (AVDD1_SEL) is set to REG side.	Open
AVDD2	Orange	+4.5~+5.5V	AVDD2 and DVDD2 of AK4682	Should be always connected when JP26 (AVDD2_SEL) is set to AVDD2 side. Can be open when JP26 (AVDD2_SEL) is set to AVDD1 side.	Open
D3.3V	Orange	+3.0~+3.6V	Power supply of logic	Should be always connected when JP45 (D3.3V_SEL) is set to D3.3V side. Can be open when JP45 (D3.3V_SEL) is set to REG side.	Open
TVDD (4682)	Orange	+2.7~+5.5V	TVDD of AK4682 TVDD of AK4114	Should be always connected when JP32 (TVDD_SEL) is set to TVDD side. Can be open when JP32 (TVDD_SEL) is set to REG side.	Open
PVDD	Red	+9~+12V	PVDD of AK4682 Regulator	Should be always connected	+9V
AVSS1	Black	0V	Analog Ground	Should be always connected	0V
AVSS2	Black	0V	Analog Ground	Should be always connected	0V
DGND	Black	0V	Digital Ground	Should be always connected	0V

Table 1. Power supply lines

Each supply line should be distributed from the power supply unit.

2. Set up evaluation mode and jumper pins. (Refer to the following item.)

3. Connect cables. (Refer to the following item.)

4. Power on.
The AK4682 should be reset once bringing PDN (SW1) “L” upon power-up.

5. Set up control software registers. (Refer to the following item.)

■ Evaluation modes

(1) DAC with external DIR

1. Connection of connector
   For digital (S/PDIF) input, RCA connector J22 (PORTA_RX0) is available.
   For analog output, RCA connector J15 (LOUT1) and JP28 (ROUT1) are available.

2. Setting of jumper pin
   Setting of interface signal of PORTA: AK4114 (U7) is as follows.
   (Default input of PORTA is SDTIA1.)

Jumper	JP10	JP13	JP14	JP16	JP17	JP18
	XTIA	SDTIA1_SEL	SDTIA2_SEL	MCLKA_SEL	BICKA	LRCKA
Default	Open	DIR	GND	MCKO1	Short	Short

Table 2. Setting of interface signal of PORTA: AK4114 (U7) (1/3)

3. Setting of toggle switch

Switch	SW3
Default	H

Table 3. Setting of interface signal of PORTA: AK4114 (U7) (2/3)

4. Setting of DIP switch

Switch	SW2					
	DIF0	DIF1	DIF2	CM0	OCKS0	OCKS1
Default	H	L	H	L	L	L

Table 4. Setting of interface signal of PORTA: AK4114 (U7) (3/3)

(2) ADC with external DIT

1. Connection of connector
   For analog input, RCA connector J3 (LINA)/J6 (RINA), J7 (LINB)/J9 (RINB) are available.
   Setting of jumpers without inputs are open.
   For digital (S/PDIF) output, RCA connector J26 (PORTB_TX1) is available.

2. Setting of jumper pin
   Setting of analog inputs.

Inputs	JP39 (LIN1)/ JP33 (RIN1)	JP40 (LIN2)/ JP34 (RIN2)	JP41 (LIN3)/ JP35 (RIN3)	JP42 (LIN4)/ JP36 (RIN4)	JP43 (LIN5)/ JP37 (RIN5)	JP44 (LIN6)/ JP38 (RIN6)	
LIN1/ RIN1	LINA/RINA	Open	Open	Open	Open	Open	(Default)
LIN2/ RIN2	Open	LINA/RINA	Open	Open	Open	Open	
LIN3/ RIN3	Open	Open	LINA/RINA	Open	Open	Open	
LIN4/ RIN4	Open	Open	Open	LINA/RINA	Open	Open	
LIN5/ RIN5	Open	Open	Open	Open	LINA/RINA	Open	
LIN6/ RIN6	Open	Open	Open	Open	Open	LINA/RINA	

Table 5. Setting of inputs through LINA/RINA

Inputs	JP39 (LIN1)/ JP33 (RIN1)	JP40 (LIN2)/ JP34 (RIN2)	JP41 (LIN3)/ JP35 (RIN3)	JP42 (LIN4)/ JP36 (RIN4)	JP43 (LIN5)/ JP37 (RIN5)	JP44 (LIN6)/ JP38 (RIN6)
LIN1/ RIN1	LINB/RINB	Open	Open	Open	Open	Open
LIN2/ RIN2	Open	LINB/RINB	Open	Open	Open	Open
LIN3/ RIN3	Open	Open	LINB/RINB	Open	Open	Open
LIN4/ RIN4	Open	Open	Open	LINB/RINB	Open	Open
LIN5/ RIN5	Open	Open	Open	Open	LINB/RINB	Open
LIN6/ RIN6	Open	Open	Open	Open	Open	LINB/RINB

Table 6. Setting of inputs through LINB/RINB

Setting of interface signal of PORTB: AK4114 (U10) is as follows.
X3 (12.288MHz) is used as Clock (256fs) .

Jumper	JP20	JP27	JP28	JP29	JP46
	EXA50	MCLKB_SEL1	BICKB_SEL	LRCKB_SEL	MCLKB_SEL2
Default	Open	Open	BICK	LRCK	MCKO1

Table 7. Setting of interface signal of PORTB: AK4114 (U10) (1/3)

3. Setting of toggle switch

Switch	SW5
Default	H

Table 8. Setting of PORTB: AK4114 (U10) (2/3)

4. Setting of DIP switch

Switch	SW4					
	DIF0	DIF1	CM0	OCKS0	OCKS1	MSB
Default	H	L	H	L	L	L

Table 9. Setting of interface signal of PORTB: AK4114 (U7) (3/3)

(3) Analog input to analog output (Through: Analog input → Analog output)

1. Connection of connector
For analog input, RCA connector J3 (LINA)/J6 (RINA), J7 (LINB)/J9 (RINB) are available.
Setting of jumpers without inputs are open.
For analog output, RCA connector J15 (LOUT1)/J28 (ROUT1), J16 (LOUT2)/J18 (ROUT2), J17 (LOUT3)/J27 (ROUT3) are available.

2. Setting of jumper pin
Setting of analog inputs.

Inputs	JP39 (LIN1)/ JP33 (RIN1)	JP40 (LIN2)/ JP34 (RIN2)	JP41 (LIN3)/ JP35 (RIN3)	JP42 (LIN4)/ JP36 (RIN4)	JP43 (LIN5)/ JP37 (RIN5)	JP44 (LIN6)/ JP38 (RIN6)	
LIN1/ RIN1	LINA/RINA	Open	Open	Open	Open	Open	(Default)
LIN2/ RIN2	Open	LINA/RINA	Open	Open	Open	Open	
LIN3/ RIN3	Open	Open	LINA/RINA	Open	Open	Open	
LIN4/ RIN4	Open	Open	Open	LINA/RINA	Open	Open	
LIN5/ RIN5	Open	Open	Open	Open	LINA/RINA	Open	
LIN6/ RIN6	Open	Open	Open	Open	Open	LINA/RINA	

Table 10. Setting of inputs through LINA/RINA

Inputs	JP39 (LIN1)/ JP33 (RIN1)	JP40 (LIN2)/ JP34 (RIN2)	JP41 (LIN3)/ JP35 (RIN3)	JP42 (LIN4)/ JP36 (RIN4)	JP43 (LIN5)/ JP37 (RIN5)	JP44 (LIN6)/ JP38 (RIN6)
LIN1/ RIN1	LINB/RINB	Open	Open	Open	Open	Open
LIN2/ RIN2	Open	LINB/RINB	Open	Open	Open	Open
LIN3/ RIN3	Open	Open	LINB/RINB	Open	Open	Open
LIN4/ RIN4	Open	Open	Open	LINB/RINB	Open	Open
LIN5/ RIN5	Open	Open	Open	Open	LINB/RINB	Open
LIN6/ RIN6	Open	Open	Open	Open	Open	LINB/RINB

Table 11. Setting of inputs through LINB/RINB

3. Setting of toggle switch

Switch	SW3	SW5
Default	L	H

Table 12. Setting of interface signal of PORTB: AK4114 (U7, U10)

(4) Analog input to analog output with external DIR (Analog input → ADC → DAC → Analog output)

1. Connection of connector

For analog input, RCA connector J3 (LINA)/J6 (RINA), J7 (LINB)/J9 (RINB) are available.
Setting of jumpers for unused inputs are open.
For analog output, RCA connector J15 (LOUT1)/J28 (ROUT1), J16 (LOUT2)/J18 (ROUT2), J17 (LOUT3)/J27 (ROUT3) are available.
* X2 is available for clock. X2 is the X'tal for 11.2896MHz on the evaluation board. Change the X'tal depends on Fs.

2. Setting of jumper pin

Setting of analog inputs.

Inputs	JP39 (LIN1)/ JP33 (RIN1)	JP40 (LIN2)/ JP34 (RIN2)	JP41 (LIN3)/ JP35 (RIN3)	JP42 (LIN4)/ JP36 (RIN4)	JP43 (LIN5)/ JP37 (RIN5)	JP44 (LIN6)/ JP38 (RIN6)	
LIN1/ RIN1	LINA/RINA	Open	Open	Open	Open	Open	(Default)
LIN2/ RIN2	Open	LINA/RINA	Open	Open	Open	Open	
LIN3/ RIN3	Open	Open	LINA/RINA	Open	Open	Open	
LIN4/ RIN4	Open	Open	Open	LINA/RINA	Open	Open	
LIN5/ RIN5	Open	Open	Open	Open	LINA/RINA	Open	
LIN6/ RIN6	Open	Open	Open	Open	Open	LINA/RINA	

Table 13. Setting of inputs through LINA/RINA

Inputs	JP39 (LIN1)/ JP33 (RIN1)	JP40 (LIN2)/ JP34 (RIN2)	JP41 (LIN3)/ JP35 (RIN3)	JP42 (LIN4)/ JP36 (RIN4)	JP43 (LIN5)/ JP37 (RIN5)	JP44 (LIN6)/ JP38 (RIN6)
LIN1/ RIN1	LINB/RINB	Open	Open	Open	Open	Open
LIN2/ RIN2	Open	LINB/RINB	Open	Open	Open	Open
LIN3/ RIN3	Open	Open	LINB/RINB	Open	Open	Open
LIN4/ RIN4	Open	Open	Open	LINB/RINB	Open	Open
LIN5/ RIN5	Open	Open	Open	Open	LINB/RINB	Open
LIN6/ RIN6	Open	Open	Open	Open	Open	LINB/RINB

Table 14. Setting of inputs through LINB/RINB

Setting of interface signal of PORTA: AK4114 (U7) is as follows.
(Default input of PORTA is SDTIA1.)

Jumper	JP10	JP13	JP14	JP16	JP17	JP18
	XTIA	SDTIA1_SEL	SDTIA2_SEL	MCLKA_SEL	BICKA	LRCKA
Default	Open	DIR	GND	MCKO1	Short	Short

Table 15. Setting of interface signal of PORTA: AK4114 (U7) (1/5)

Setting of interface signal of PORTB: AK4114 (U10) is as follows.

Jumper	JP20	JP27	JP28	JP29	JP46
	EXA50	MCLKB_SEL1	BICKB_SEL	LRCKB_SEL	MCLKB_SEL2
Default	Open	Open	BICKA	LRCKA	MCLKA

Table 16. Setting of interface signal of PORTB: AK4114 (U10) (2/5)

3. Setting of toggle switch

Switch	SW3	SW5
Default	H	H

Table 17. Setting of interface signal of PORTB: AK4114 (U7, U10) (3/5)

4. Setting of DIP switch

Switch	SW2					
	DIF0	DIF1	DIF2	CM0	OCKS0	OCKS1
Default	H	L	H	H	L	L

Table 18. Setting of interface signal of PORTA: AK4114 (U7) (4/5)

Switch	SW4					
	DIF0	DIF1	CM0	OCKS0	OCKS1	MSB
Default	H	L	H	L	L	L

Table 19. Setting of interface signal of PORTB: AK4114 (U7) (5/5)

■ Register control

AKD4682-A can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT2 (uP-I/F) to PC by 10-line flat cable packed with this. Take care of the direction of connector. There is a mark at connector. Connect the mark of 10-pin connector to pin#6 of PORT2. (Figure 2.)

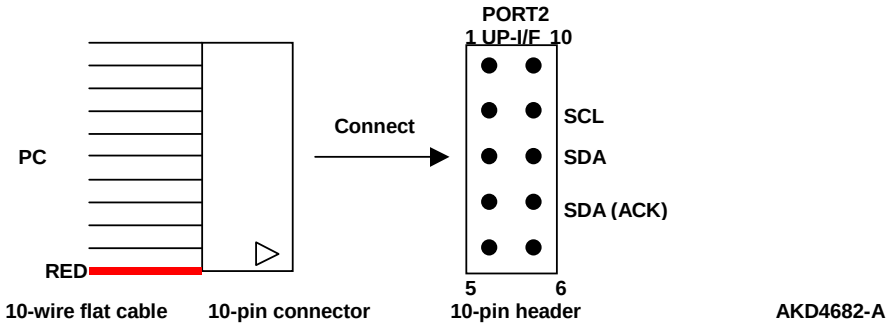


Figure 2. PORT2 pin layout

Control software is packed with this evaluation board. Software operation procedure is included in evaluation board manual.

■ Set-up DIP switch (SW2)

No.	Name	Content	Default
1	DIF0	Setting of AK4114 Audio Interface Format (Refer Table 20.)	ON
2	DIF1		OFF
3	DIF2		ON
4	CM0	Selection of AK4114 Clock Mode (Clock Source) (Refer Table 21.)	OFF
6	OCKS0	Selection of AK4114 Master Clock Output frequency (Refer Table 22.)	OFF
7	OCKS1		OFF

Table 20. Set up modes of AK4114 (U7) and AK4682 (U1)

Mode	DIF2	DIF1	DIF0	DAUX	SDTO	LRCK		BICK		
							I/O		I/O	
0	0	0	0	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O	
1	0	0	1	24bit, Left justified	18bit, Right justified	H/L	O	64fs	O	
2	0	1	0	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
3	0	1	1	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
4	1	0	0	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	
5	1	0	1	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	
6	1	1	0	24bit, Left justified	24bit, Left justified	H/L	I	64-128fs	I	<Default>
7	1	1	1	24bit, I^2S	24bit, I^2S	L/H	I	64-128fs	I	

Table 21. AK4114 Audio Interface Format

Mode	CM0	PLL	X'tal	Clock source	SDTO	
0	0	ON	ON(Note)	PLL	RX	<Default>
1	1	OFF	ON	X'tal	DAUX	

Table 22. AK4114 Clock Mode (Clock Source)

No.	OCKS1	OCKS0	MCKO1	MCKO2	X'tal	fs (max)	
0	0	0	256fs	256fs	256fs	96 kHz	<Default>
1	0	1	256fs	128fs	256fs	96 kHz	
2	1	0	512fs	256fs	512fs	48 kHz	
3	1	1	128fs	64fs	128fs	192 kHz	

Table 23. AK4114 Master Clock Output Frequency

■ Toggle switch

[SW1] PDN:
Switch for power down reset of AK4682 (U1). Keep "H" during operation of AK4682 (U1).
Power down reset of AK4682 will be done by setting SW1 to "L" once, after power on.

[SW3] AK4114 (U7)-PDN:
Switch for power down reset of AK4114 (U7). Keep "H" during operation of AK4114 (U7).
Power down reset of AK4114 (U7) will be done by setting SW1 to "L" once, after power on.

[SW5] AK4114 (U10)-PDN:
Switch for power down reset of AK4114 (U10). Keep "H" during operation of AK4114 (U10).
Power down reset of AK4114 (U10) will be done by setting SW1 to "L" once, after power on.

■ LED indication

[LED1] ERF:
LED for output of AK4114 (U7): INT0. It turns on when output of AK4114 (U7): INT0 is "H".

[LED2] ERF:
LED for output of AK4114 (U10): INT0. It turns on when output of AK4114 (U10): INT0 is "H".

■ Set up Jumper pins

Jumper	Evaluation Mode			
	1	2	3	4
JP39 (LIN1)	Open	LINA	LINA	Open
JP40 (LIN2)	Open	Open	Open	Open
JP41 (LIN3)	Open	Open	Open	Open
JP42 (LIN4)	Open	Open	Open	Open
JP43 (LIN5)	Open	Open	Open	Open
JP44 (LIN6)	Open	Open	Open	Open
JP33 (RIN1)	Open	RINA	RINA	Open
JP34 (RIN2)	Open	Open	Open	Open
JP35 (RIN3)	Open	Open	Open	Open
JP36 (RIN4)	Open	Open	Open	Open
JP37 (RIN5)	Open	Open	Open	Open
JP38 (RIN6)	Open	Open	Open	Open
JP10 (XTIA)	Open	Open	Open	Open
JP13 (SDTIA1_SEL)	DIR	GND	GND	DIR
JP14 (SDTIA2_SEL)	GND	GND	GND	GND
JP16 (MCLKA_SEL)	MCKO1	Open	Open	MCKO1
JP17 (BICKA)	Short	Open	Open	Short
JP18 (LRCKA)	Short	Open	Open	Short
JP27 (MCLKB_SEL1)	Open	Open	Open	MCLKA
JP28 (BICKB_SEL)	Open	BICK	Open	BICK
JP29 (LRCKB_SEL)	Open	LRCK	Open	LRCK
JP46 (MCLKB_SEL2)	Open	MCKO1	Open	MCKO1
JP25 (AVDD1_SEL)	REG	REG	REG	REG
JP26 (AVDD2_SEL)	REG	REG	REG	REG
JP32 (TVDD_SEL)	REG	REG	REG	REG
JP45 (D3.3V_SEL)	REG	REG	REG	REG
JP19 (EXA50)	Open	Open	Open	Open
JP20 (EXB50)	Open	Open	Open	Open

(Default)

■ Set up control software registers

After the reset, setting example files are available as follows in CD-ROM to set registers in each evaluation modes.

Evaluation Mode 1
ADC/DAC: ak4682_dac_mode1.akr

Evaluation Mode 2
ADC/DAC: ak4682_adc_mode2.akr

Evaluation Mode 3
ADC/DAC: ak4682_analog_through _mode3.akr

Evaluation Mode 4
ADC/DAC: ak4682_loopback_mode4.akr

■ Analog Input Circuit

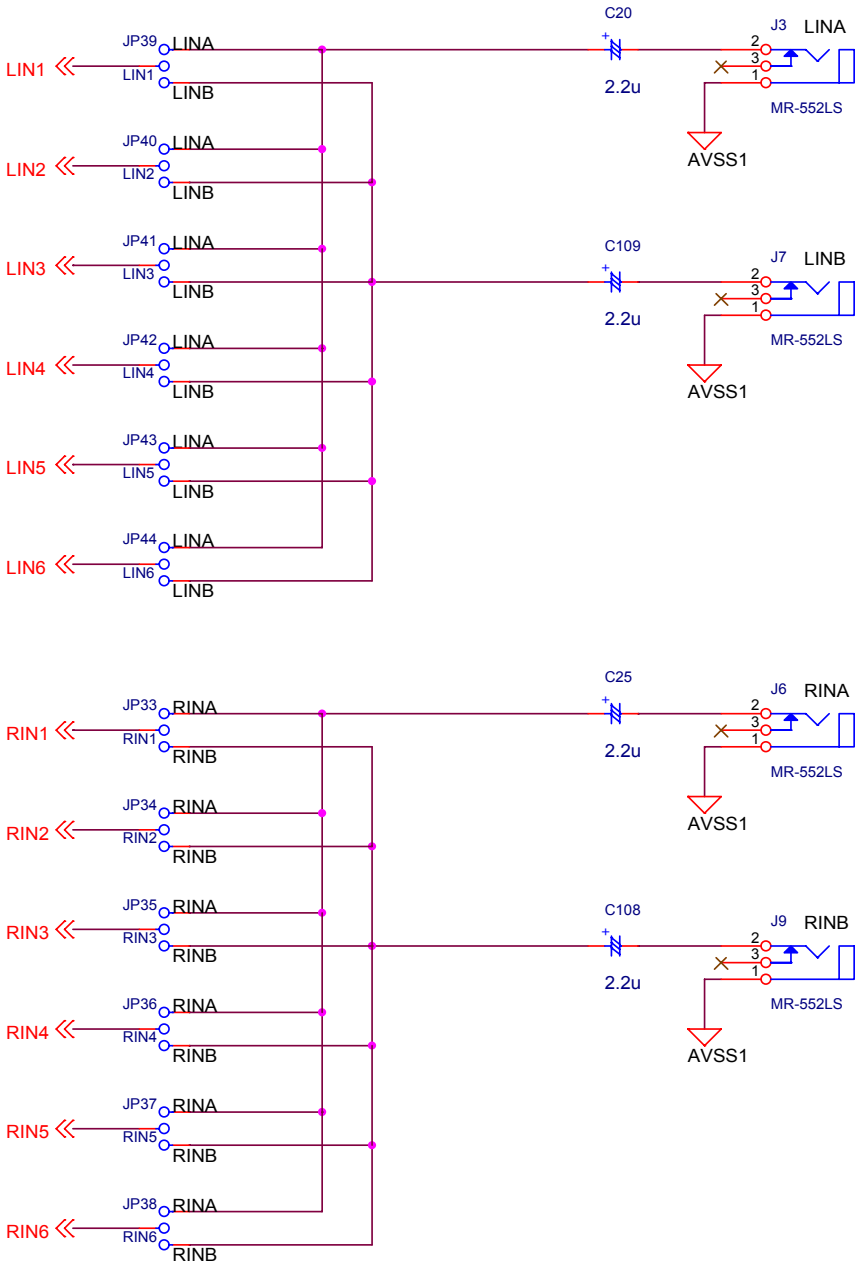


Figure 3. Analog Input Circuit

For analog input, RCA connector: J3 (LINA), J6 (RINA), J7 (LINB), J9 (RINB) are available to use.
Analog inputs are single-ended and input ranges of each channel are nominally 5.6 Vpp@5V.

■ Analog Output Circuit

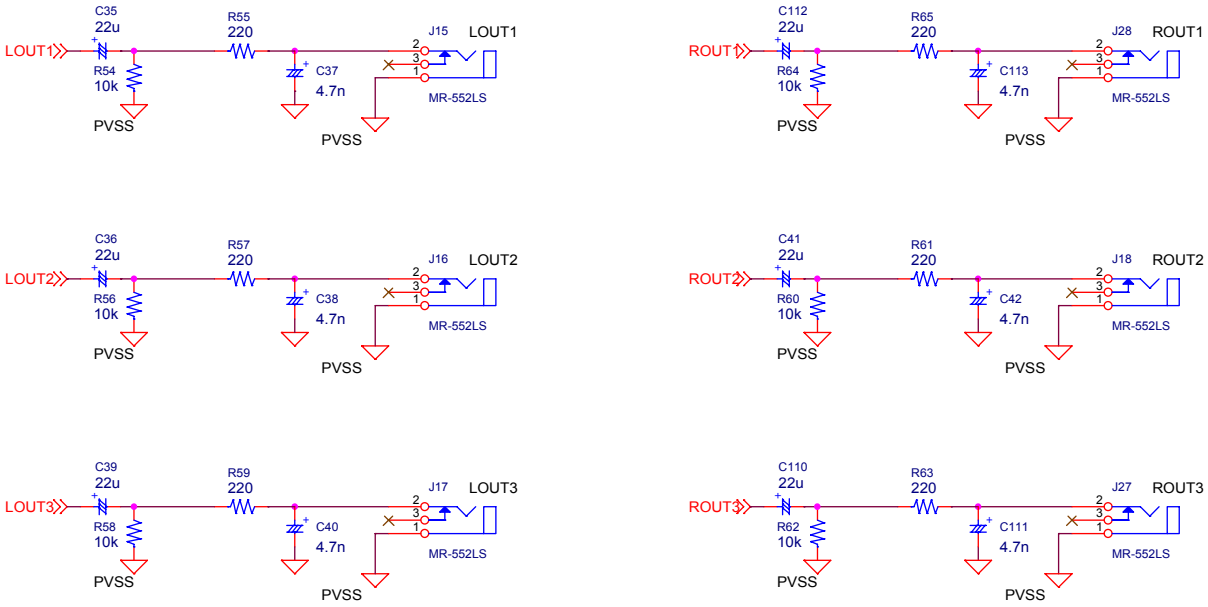


Figure 4. Analog Output Circuit

For analog output, RCA connector: J15 (LOUT1), J28 (ROUT1), J16 (LOUT2), J18 (ROUT2), J17(LOUT3), J27(ROUT3) are available to use.
Analog outputs are single-ended and output ranges of each channel are nominally 5.6Vpp@5V.
Output range: AOUT is proportional to AVDD2 (AOUT=2 x AVDD2/5 x 1.4 x 2 = 2 x 5/5 x 1.4 x 2 =5.6Vpp).

■ Digital Input Circuit (External DIR : PORTA)

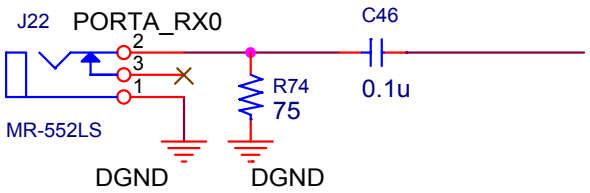


Figure 5. Digital Input Circuit (External DIR)

For digital input, RCA connector: J22 (PORTA-RX0) is available.

■ Digital Output Circuit (External DIT : PORTB)

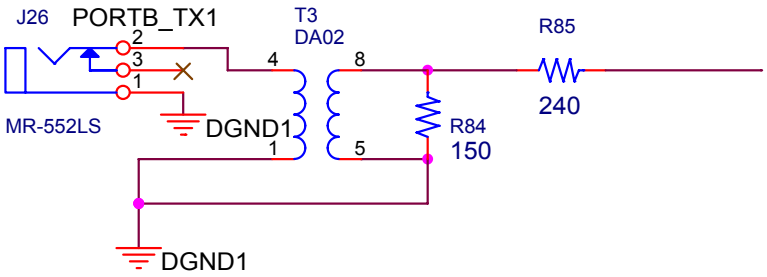


Figure 6. Digital Output Circuit (External DIT)

For digital output, RCA connector: J26 (PORTB-TX1) is available.

Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4682-A according to previous term.

2. Connect IBM-AT compatible PC with AKD4682-A by 10-line type flat cable (packed with AKD4682-A). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled "AKD4682-A Evaluation Kit" into the CD-ROM drive.

4. Access the CD-ROM drive, and double-click the icon of "akd4682-a.exe", and set up the control program.
   akd4682-a.exe: AK4682-A control program

5. Then evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click "Port Reset" button.

■ Explanation of each buttons

1. [Port Reset]: Set up the USB interface board (AKDUSBIF-A).
2. [Write default]: Initialize the registers.
3. [All Write]: Write all registers data that is currently displayed.
4. [Function1]: Dialog to write data by keyboard operation.
5. [Function2]: Dialog to write data by keyboard operation.
6. [Function3]: The sequence of register setting can be set and executed.
7. [Function4]: The sequence that is created on [Function3] can be assigned to buttons and executed.
8. [Function5]: The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
9. [SAVE]: Save the current register setting.
10. [OPEN]: Write the saved values to all register.
11. [Write]: Dialog to write data by mouse operation.

■ Indication of data

Input data is indicated on the register map. Red letter indicates "H" or "1" and blue one indicates "L" or "0". Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes “H” or “1”. If not, “L” or “0”.

When writing the input data to register, click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog]: Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.
Data Box: Input registers data in 2 figures of hexadecimal.

When writing the input data to register, click [OK] button. If not, click [Cancel] button.

3. [Function2 Dialog]: Dialog to evaluate ATT

This is a dialog corresponding to address: 08H, 09H, 0AH, 0BH, 0CH, and 0DH of AK4682.

Address Box: Input registers address in 2 figures of hexadecimal.
Start Data Box: Input starts data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to register by this interval.
Step Box: Data changes by this step.
Mode Select Box:

With checking this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

Without checking this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

When writing the input data to register, click [OK] button. If not, click [Cancel] button.

4. [Save] and [Open]

4-1. [Save]

Save the current register setting data to the file. The extension of file name is “akr”.

(Operation flow)
(1) Click [Save] Button.
(2) Set the file name and push [Save] Button. The extension of file name is “akr”.

4-2. [Open]

The register setting data saved to the file by [Save] is written to register. The file type is the same as [Save].

(Operation flow)
(1) Click [Open] Button.
(2) Select the file (*.akr) and Click [Open] Button.

5. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button.

Set the control sequence.

Set the address, Data and Interval time. Set “-1” to the address of the step where the sequence should be paused.

(3) Click [Start] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step. This sequence can be saved and opened by [Save] and [Open] button on the [Function3] window. The extension of file name is “aks”.

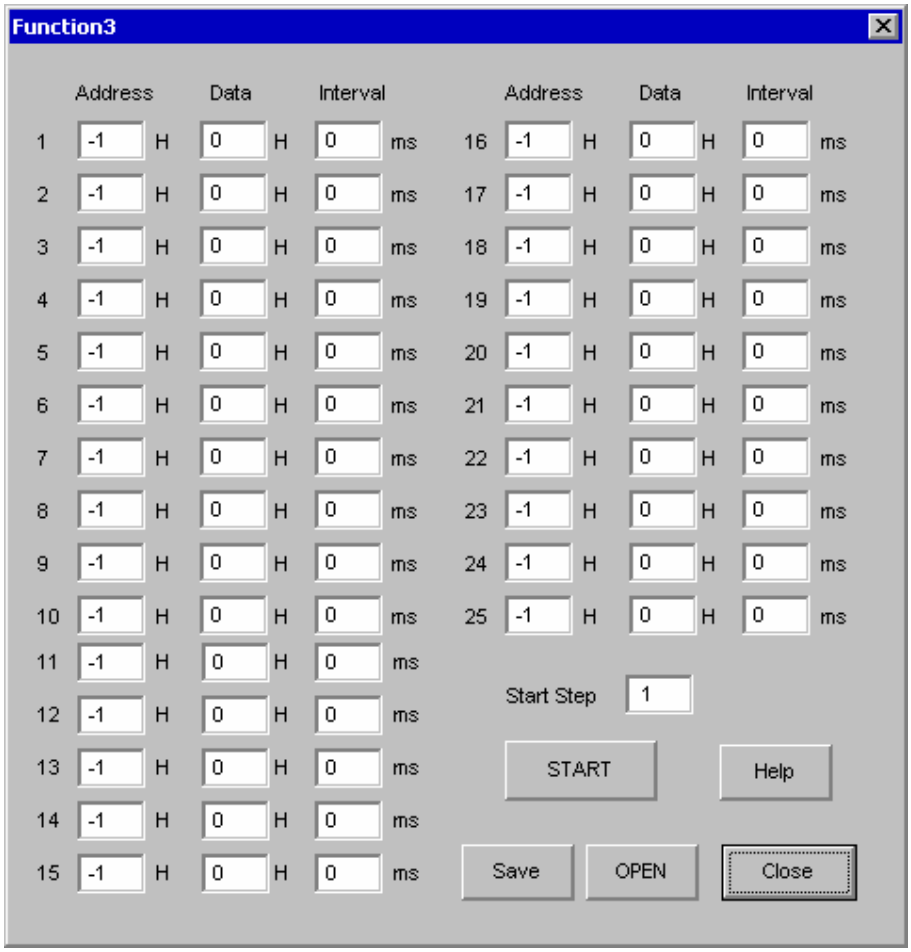


Figure 7. Window of [F3]

6. [Function4 Dialog]

The sequence that is created on [Function3] can be assigned to buttons and executed. When [F4] button is clicked, the window as shown in Figure 8 opens.

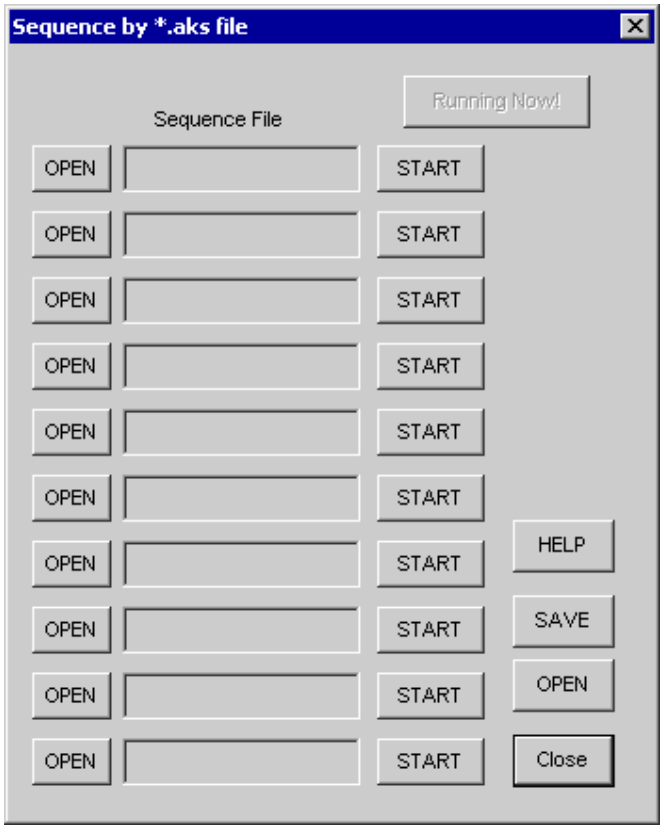


Figure 8. [F4] window

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks).

The sequence file name is displayed as shown in Figure 9.

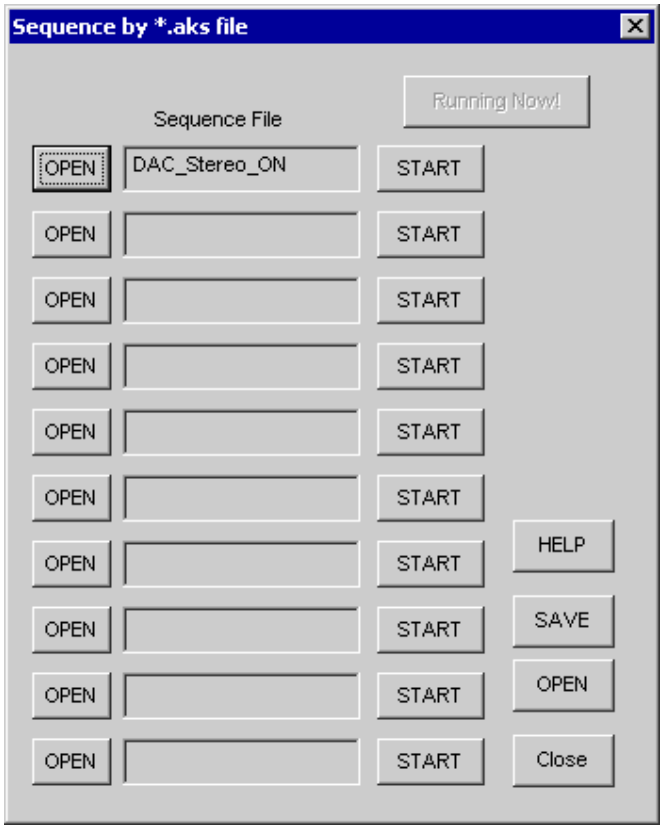


Figure 9. [F4] window(2)

(2) Click [START] button, then the sequence is executed.

6-2. [SAVE] and [OPEN] buttons on right side

[SAVE]: The sequence file names can assign be saved. The file name is *.ak4.

[OPEN]: The sequence file names assign that are saved in *.ak4 are loaded.

6-3. Note

(1) [Function4] doesn't support the pause function of sequence function.

(2) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(3) When the sequence is changed in [Function3], the file should be loaded again in order to reflect the change.

7. [Function5 Dialog]

The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed. When [F5] button is clicked, the following window as shown in Figure 10 opens.

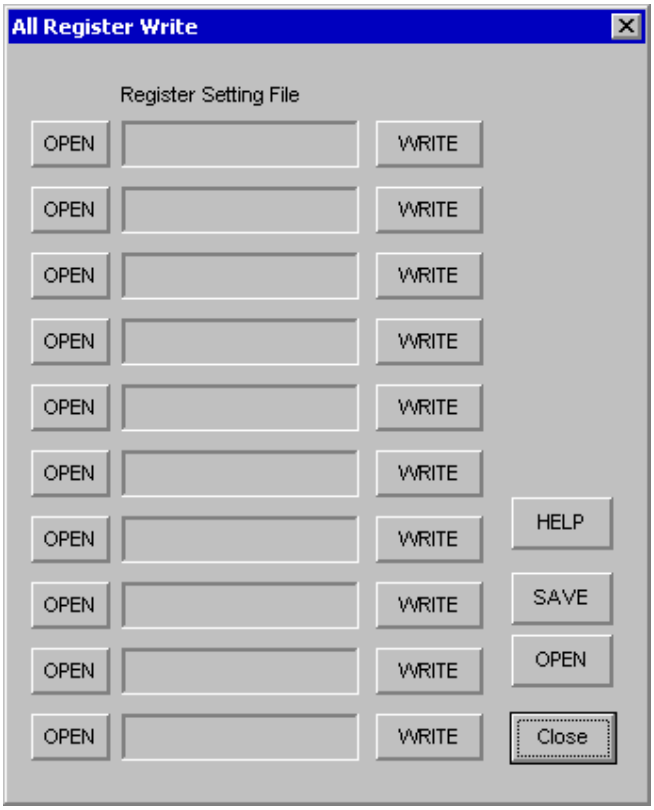


Figure 10. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

(2) Click [WRITE] button, then the register setting is executed.

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE]: The register setting file names assign can be saved. The file name is *.ak5.

[OPEN]: The register setting file names assign that are saved in *.ak5 are loaded.

7-3. Note

(1) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(2) When the register setting is changed by [Save] Button in main window, the file should be loaded again in order to reflect the change.

Measure Result

1) ADC part

[Measurement condition]

- Measurement unit : Audio Precision
- MCLK : 256fs (fs=48kHz)
- BICK : 64fs
- fs : 48kHz
- BW : 20Hz~20kHz (fs=48kHz)
- Bit : 24bit
- Power Supply : AVDD1=AVDD2=DVDD1=DVDD2=5V, TVDD=3V, PVDD =9V
- Interface : External DIT (fs=48kHz,)
- Temperature : Room Temp

fs=48kHz (ADC)

Parameter	Input signal	Measurement filter	Results [dB]	
			Lch	Rch
S/(N+D)	1kHz, -0.5dB	20kLPF	90.7	90.9
DR	1kHz, -60dB	20kLPF	93.5	93.6
DR	1kHz, -60dB	20kLPF, A-weighted	96.1	96.1
S/N	No signal	20kLPF	93.5	93.6
S/N	No signal	20kLPF, A-weighted	96.1	96.1

2) DAC part

[Measurement condition]

- Measurement unit : Audio Precision
- MCLK : 256fs (fs=48kHz, 96kHz), 128fs (fs=192kHz)
- BICK : 64fs
- fs : 48kHz, 96kHz, 192kHz
- BW : 20Hz~20kHz (fs=48kHz), 20Hz~40kHz (fs=96kHz), 20Hz~40kHz (fs=192kHz)
- Resolution : 24bit
- Power Supply : AVDD1=AVDD2=DVDD1=DVDD2=5V, TVDD=3V, PVDD =9V
- Interface : External DIR (48kHz, 96kHz, 192kHz)
- Temperature : Room Temp

fs=48kHz

Parameter	Input signal	Measurement filter	Results [dB]	
			Lch	Rch
S/(N+D)	1kHz, 0dB	20kLPF	87.9	87.4
DR	1kHz, -60dB	20kLPF	98.7	98.4
DR	1kHz, -60dB	22kLPF, A-weighted	101.4	101.2
S/N	“0” data	20kLPF	98.7	98.4
S/N	“0” data	22kLPF, A-weighted	101.4	101.2

fs=96kHz

Parameter	Input signal	Measurement filter	Results [dB]	
			Lch	Rch
S/(N+D)	1kHz, 0dB	40kLPF	87.2	86.8
DR	1kHz, -60dB	40kLPF	96.6	96.3
DR	1kHz, -60dB	22kLPF, A-weighted	101.4	101.2
S/N	“0” data	40kLPF	96.6	96.3
S/N	“0” data	22kLPF, A-weighted	101.4	101.2

fs=192kHz

Parameter	Input signal	Measurement filter	Results [dB]	
			Lch	Rch
S/(N+D)	1kHz, 0dB	40kLPF	87.1	86.7
DR	1kHz, -60dB	40kLPF	96.4	96.2
DR	1kHz, -60dB	22kLPF, A-weighted	101.4	101.2
S/N	“0” data	40kLPF	96.5	96.3
S/N	“0” data	22kLPF, A-weighted	101.4	101.2

1. ADC part

(ADC fs=48kHz)

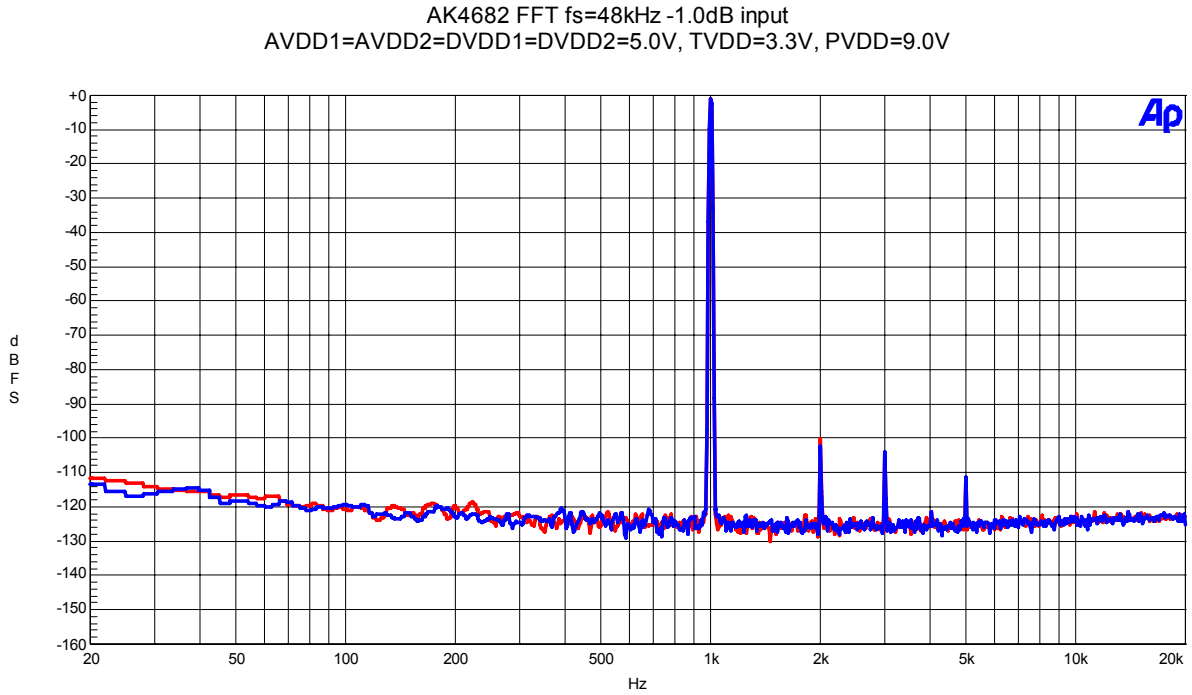


Figure 11. FFT(Input Frequency =1kHz,Input Level=-1.0dBFS)

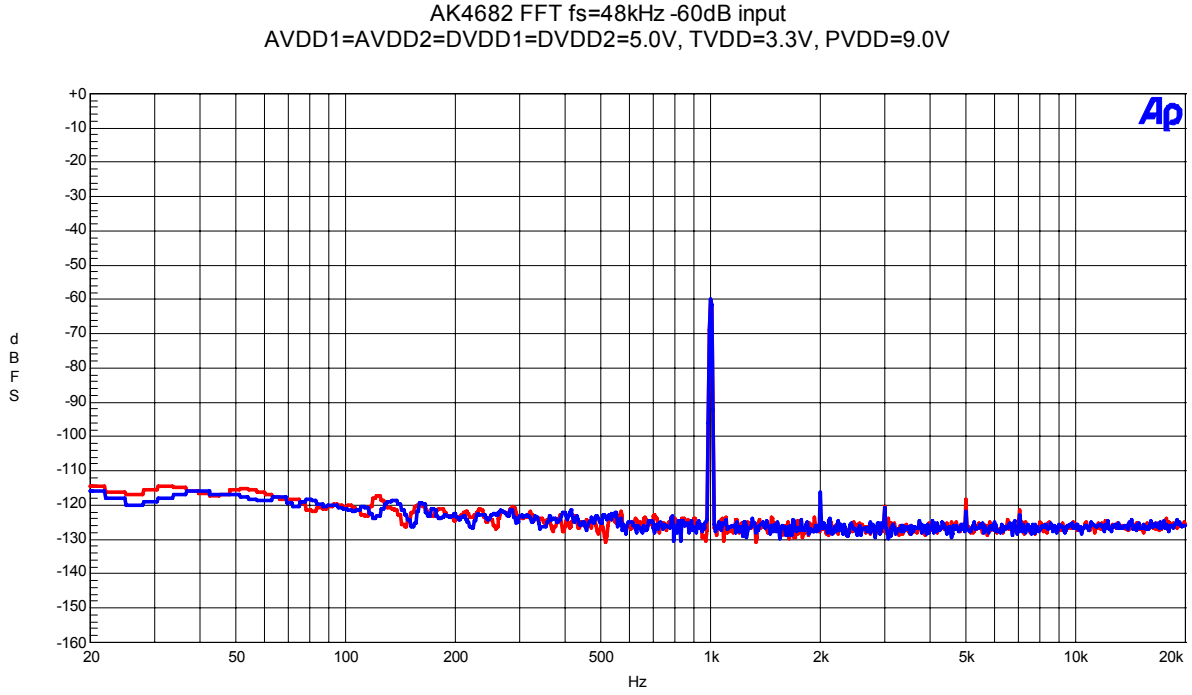


Figure 12. FFT(Input Frequency =1kHz,Input Level=-60dBFS)

(ADC fs=48kHz)

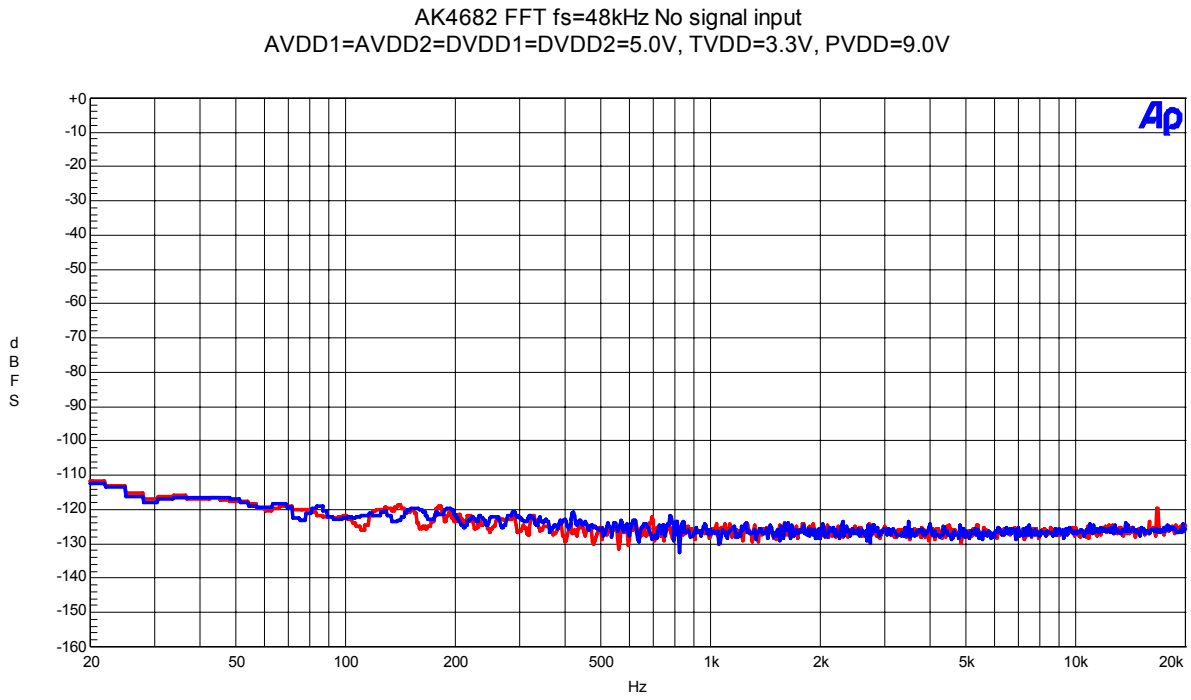


Figure 13. FFT(noise floor)

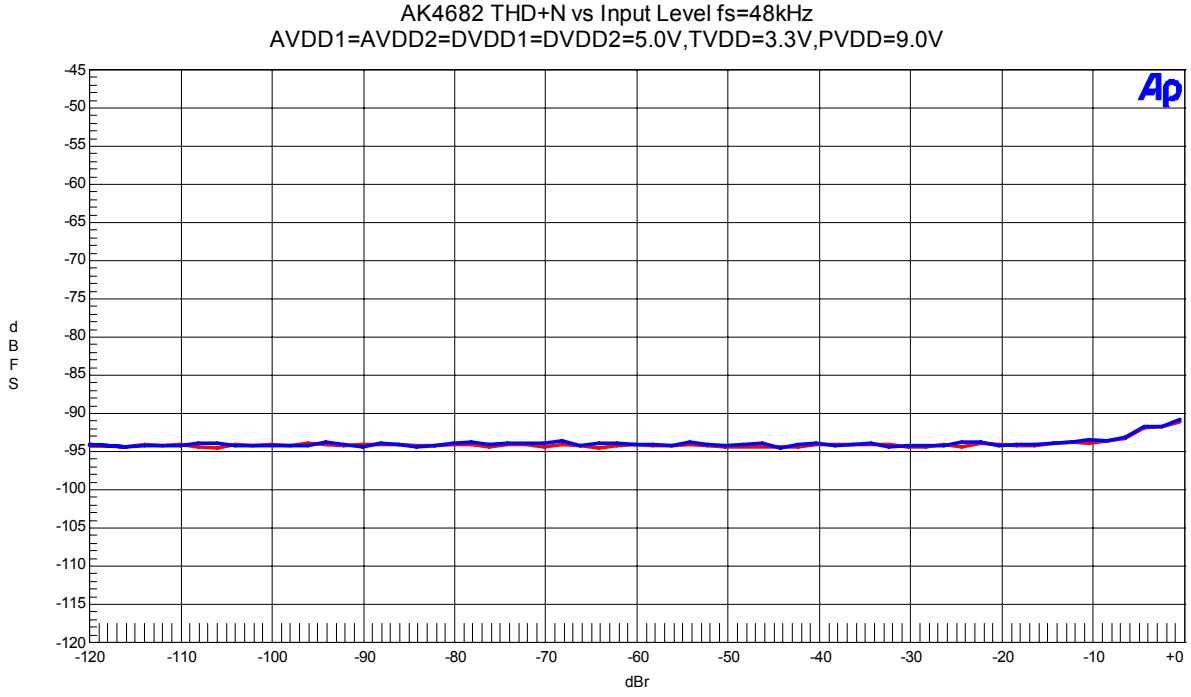


Figure 14. THD + N vs Input Level (Input Frequency =1kHz)

(ADC fs=48kHz)

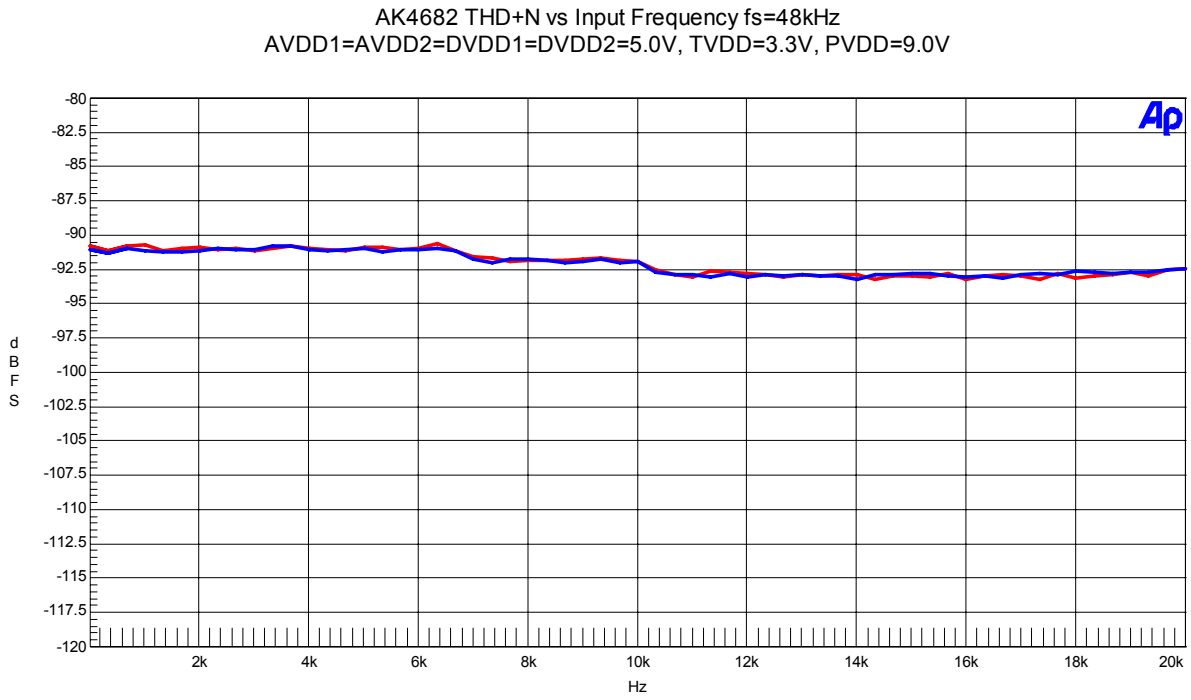


Figure 15. THD + N vs Input Frequency (Input Level=-1.0dBFS)

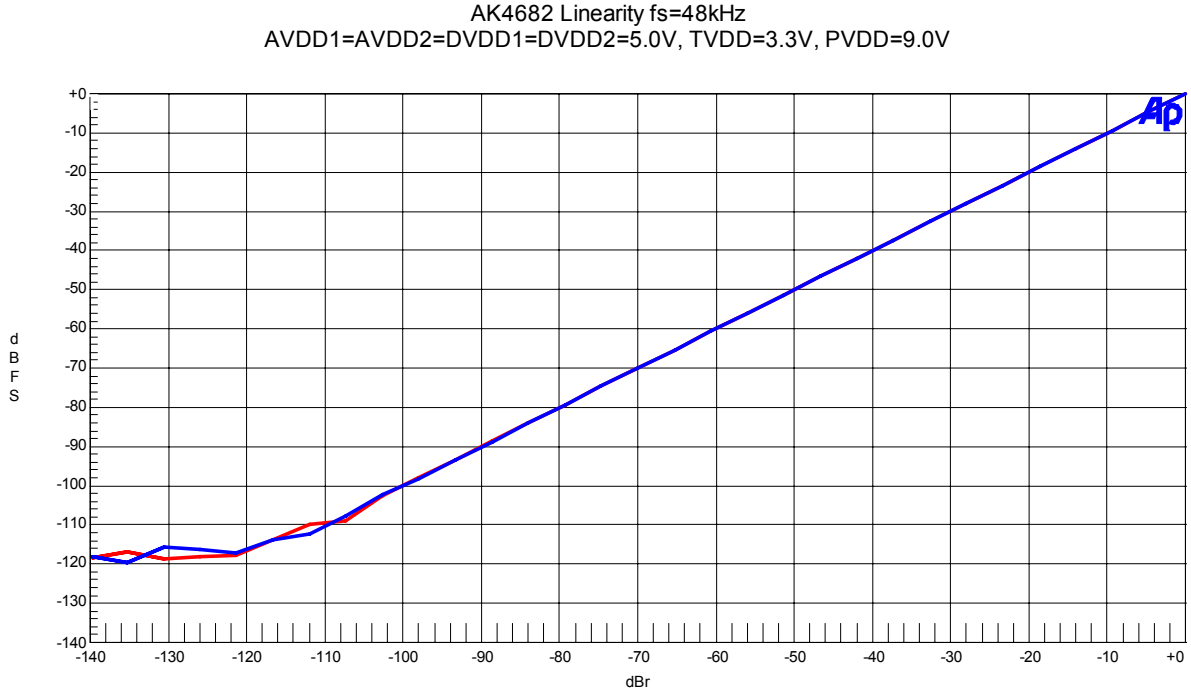


Figure 16. Linearity (Input Frequency =1kHz)

(ADC fs=48kHz)

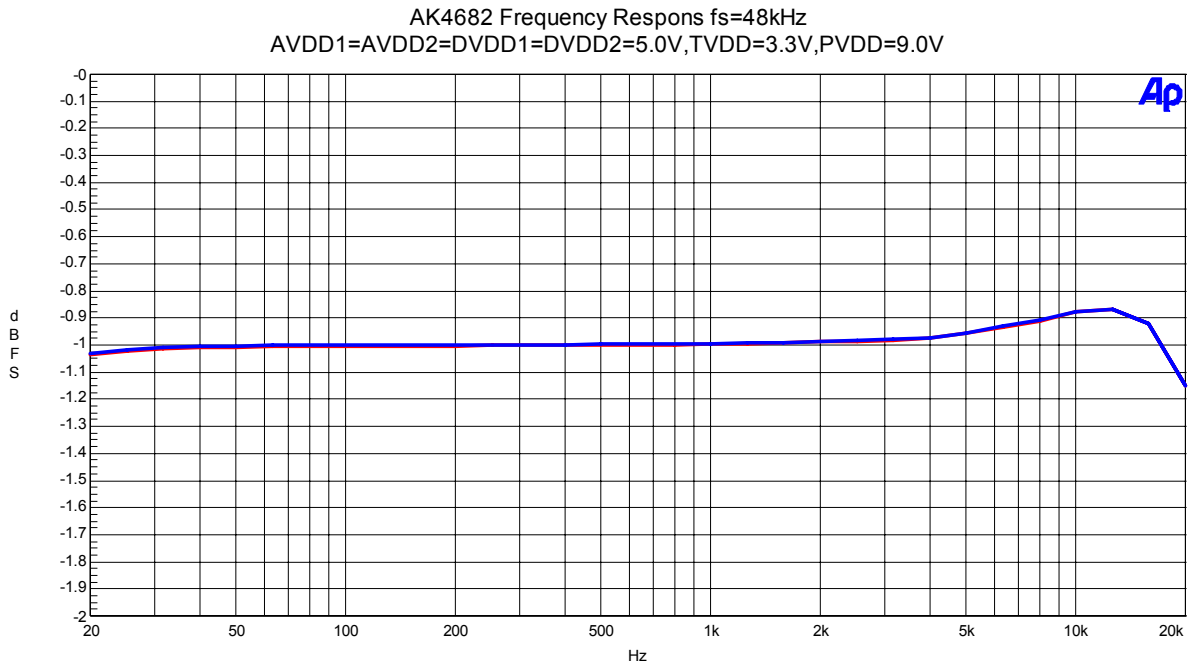


Figure 17. Frequency Response (Input Level=-1.0dBFS)

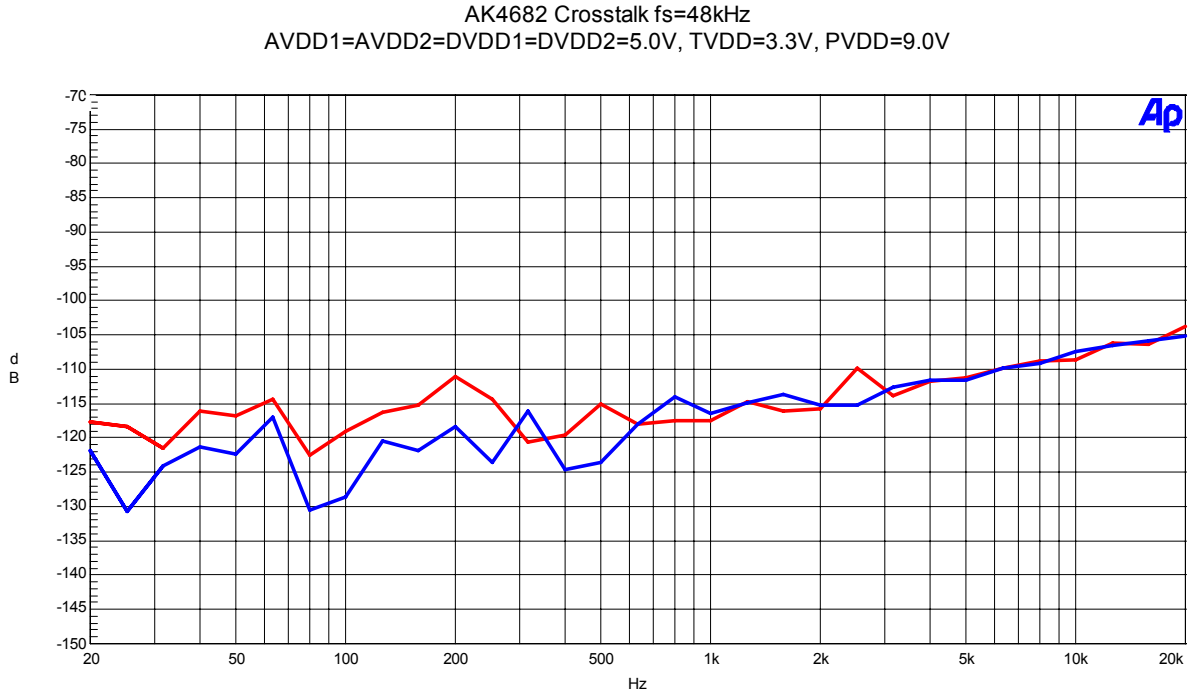


Figure 18. Crosstalk (Input Level=-1.0dBFS)

2. DAC part

(DAC fs=48kHz)

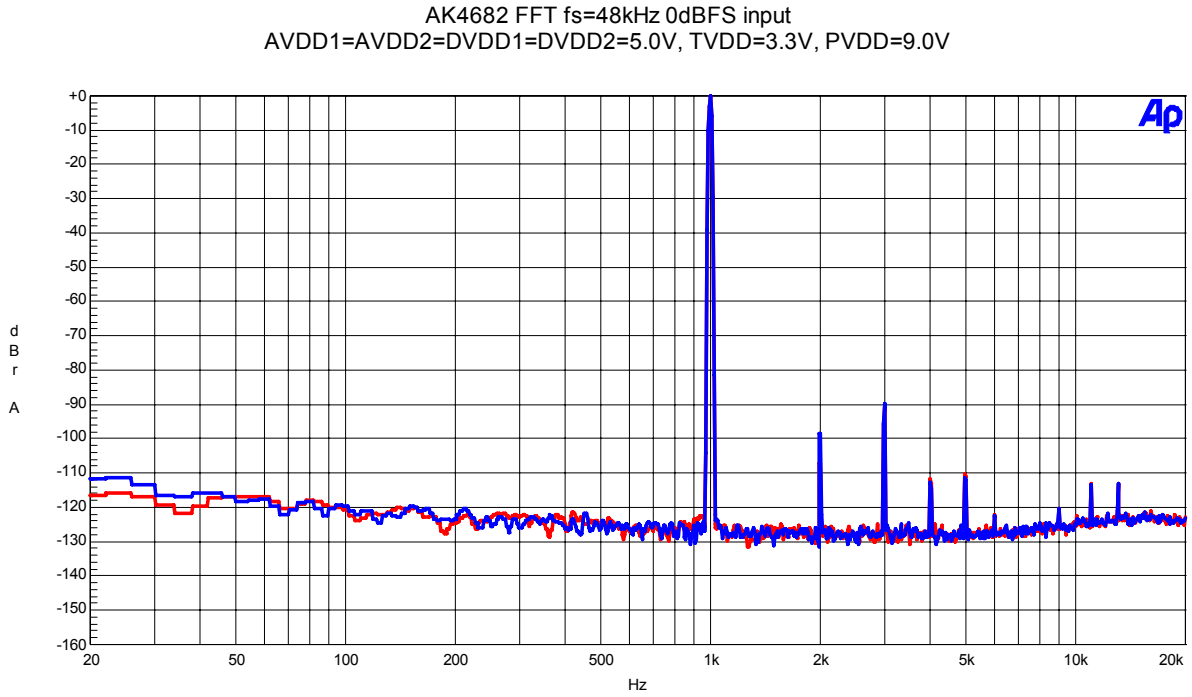


Figure 19. FFT(Input Frequency =1kHz, Input Level=0dBFS)

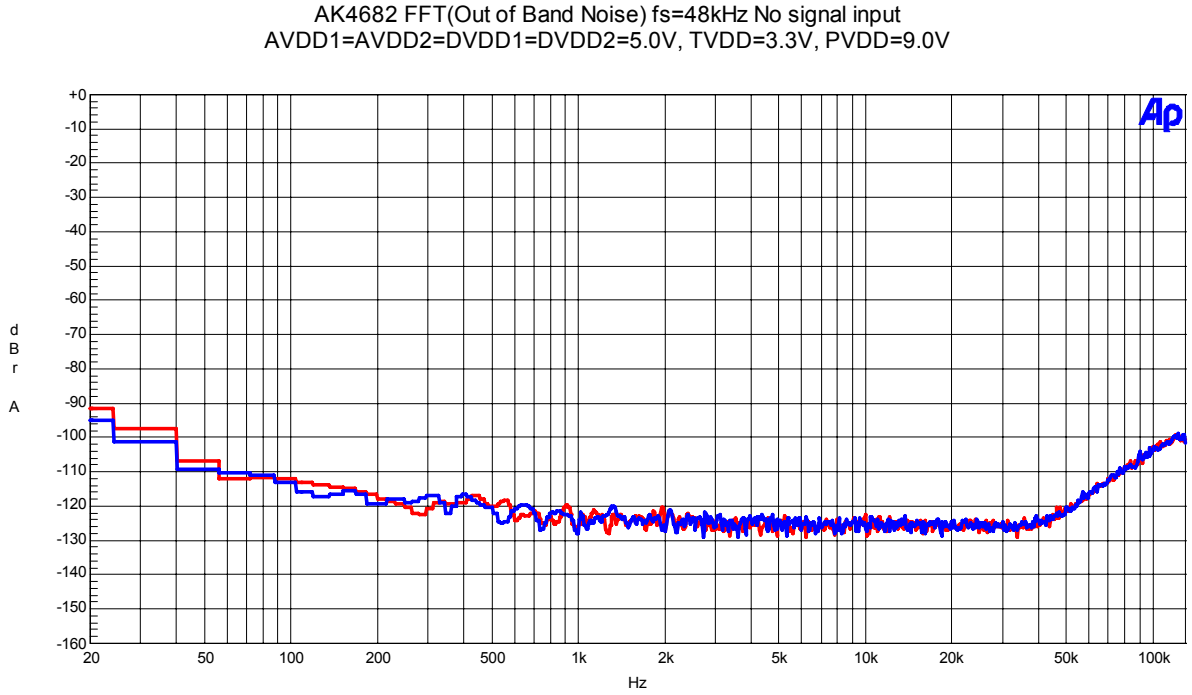


Figure 20. FFT(Input Frequency =1kHz, Input Level=0dBFS,Notch=on)

(DAC fs=48kHz)

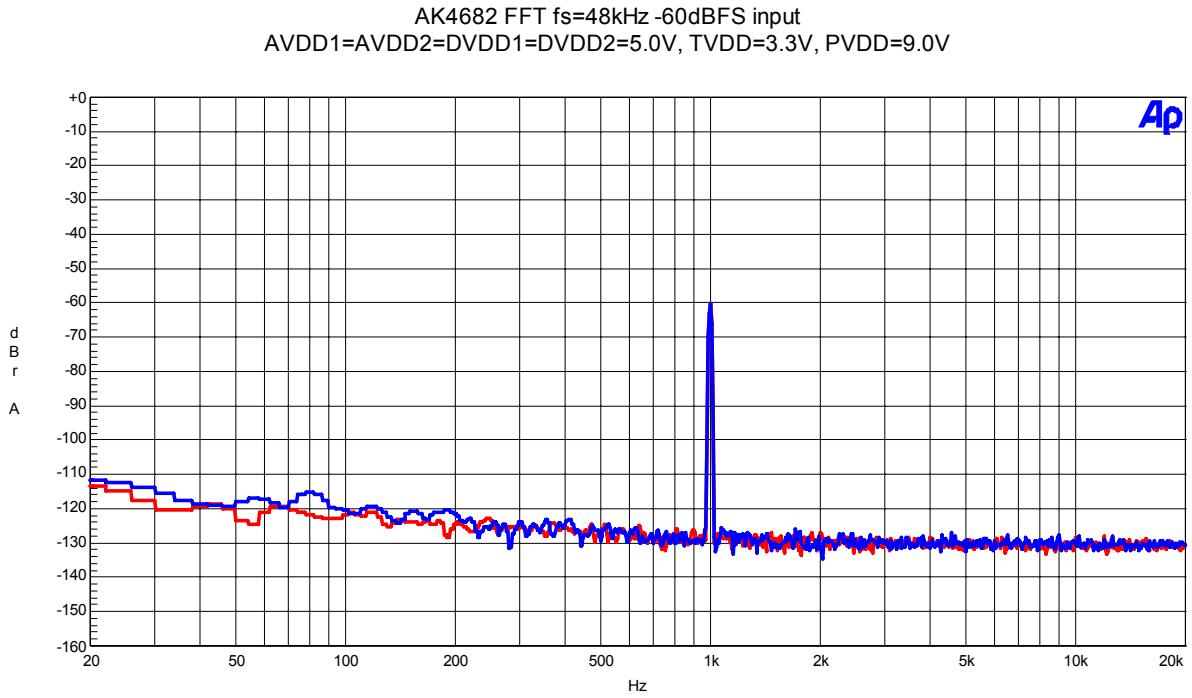


Figure 21. FFT(Input Frequency =1kHz, Input Level=-60dBFS)

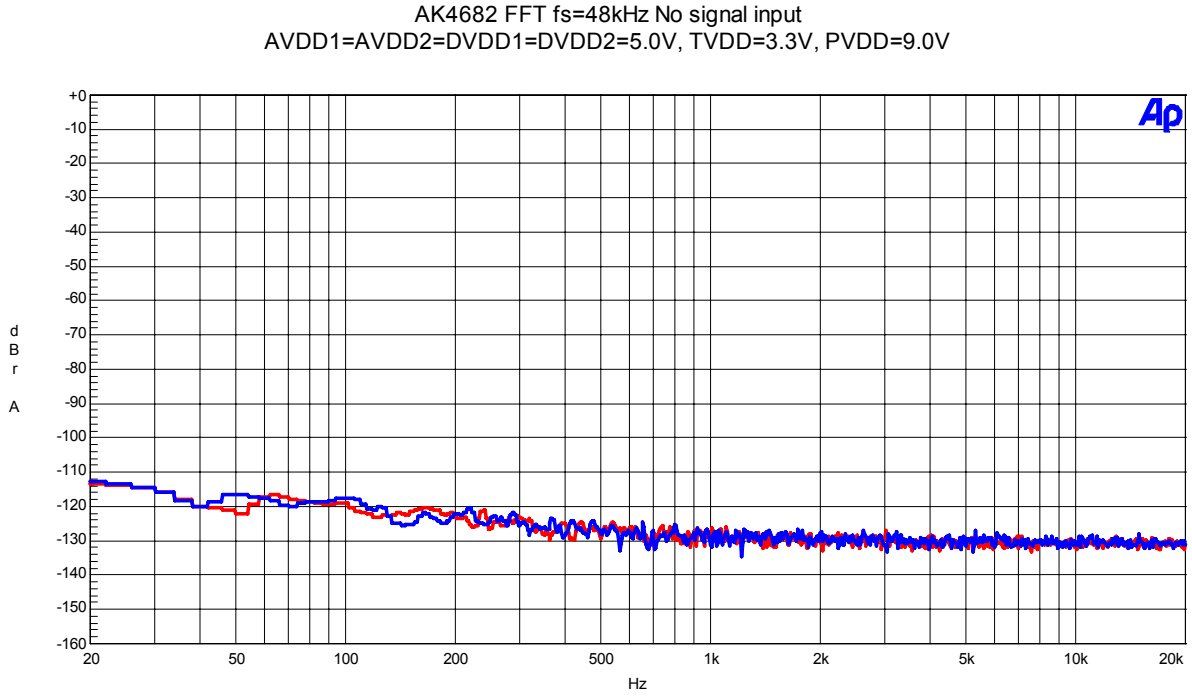


Figure 22. FFT(noise floor)

(DAC fs=48kHz)

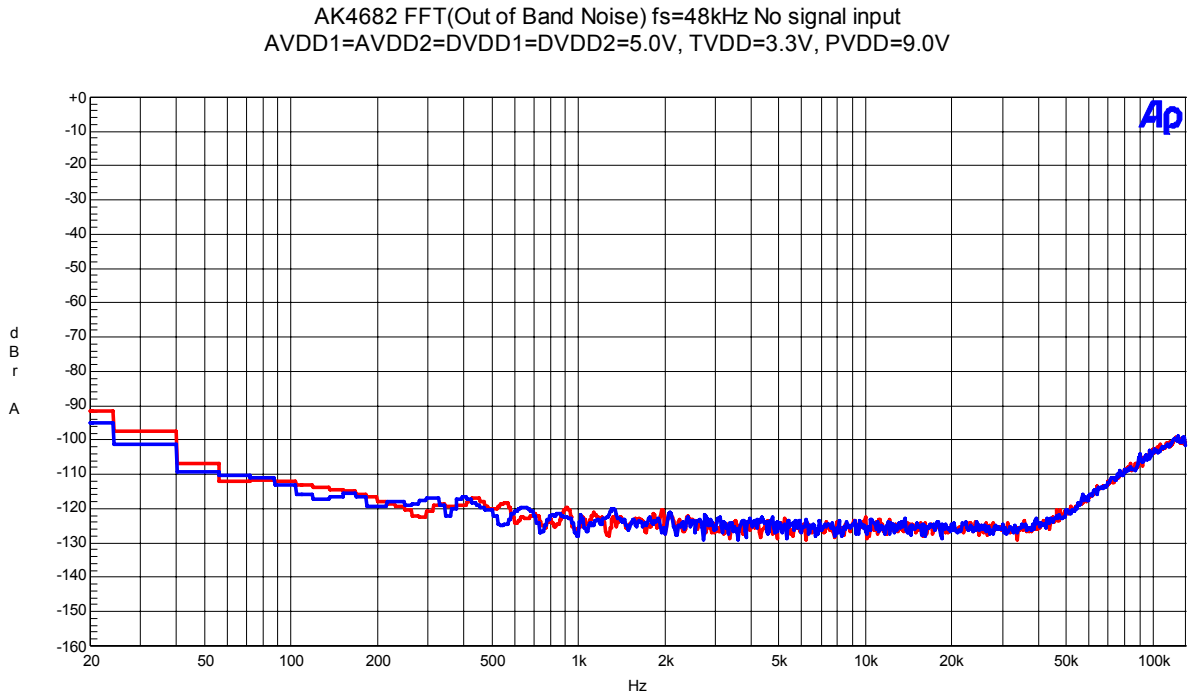


Figure 23. FFT(out-of-band noise)

AKM

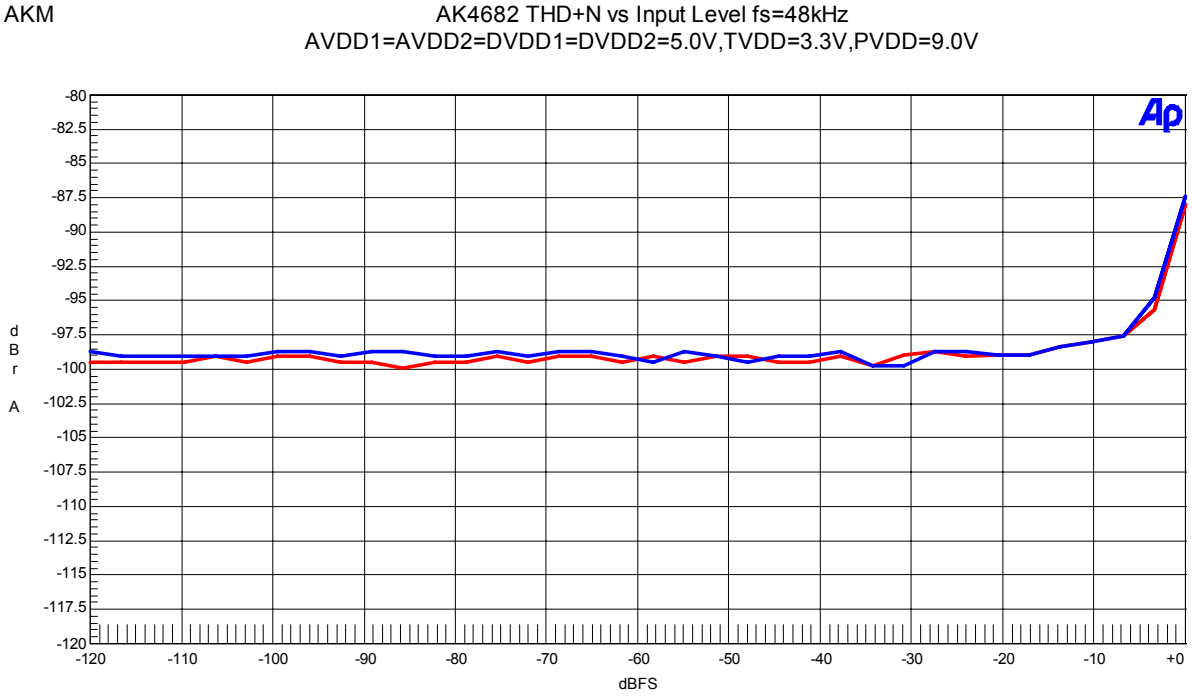


Figure 24. THD+N vs Input Level (Input Frequency =1kHz)

(DAC fs=48kHz)

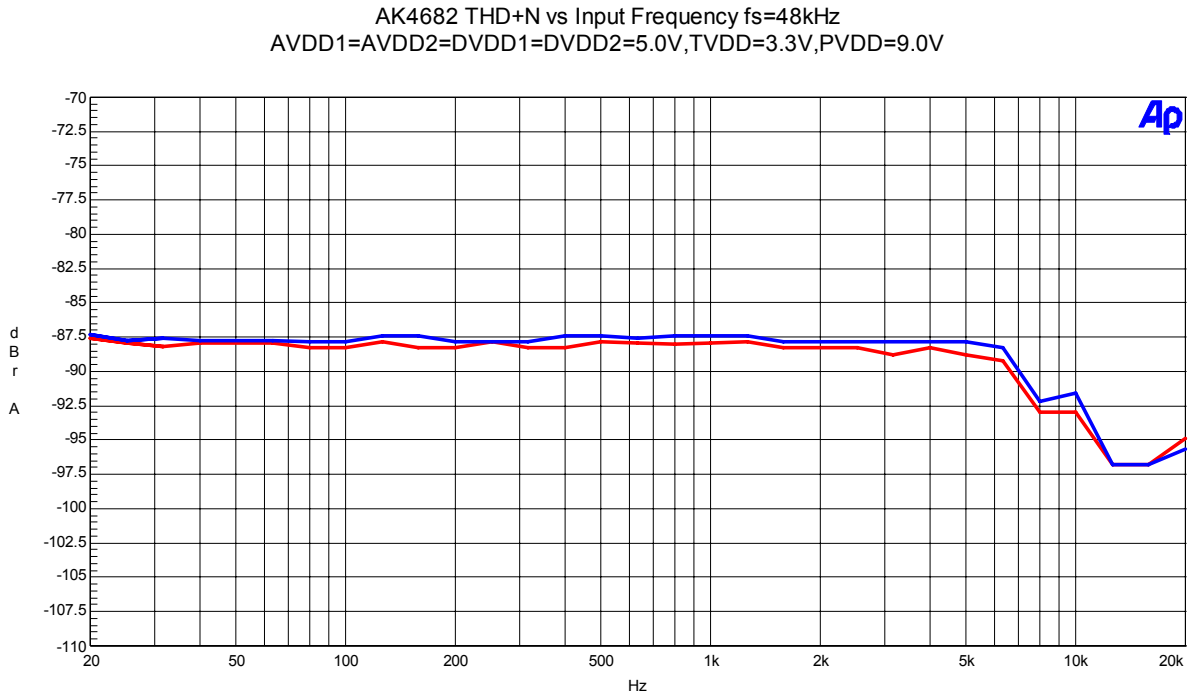


Figure 25. THD+N vs Input Frequency (Input Level=0dBFS)

AKM

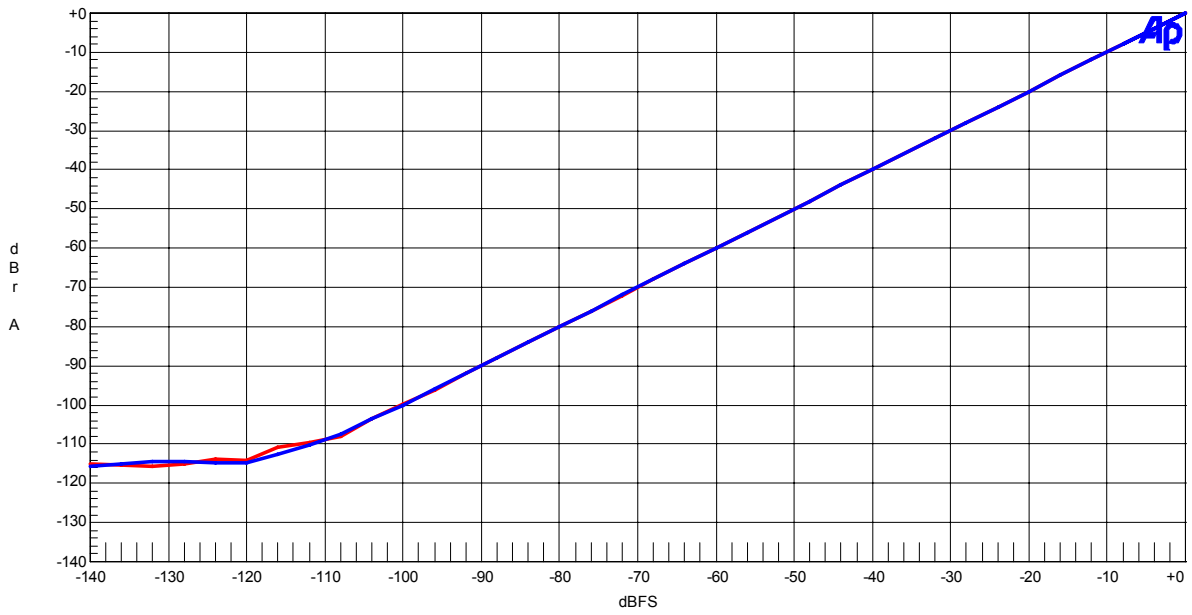


Figure 26. Linearity (Input Frequency =1kHz)

(DAC fs=48kHz)

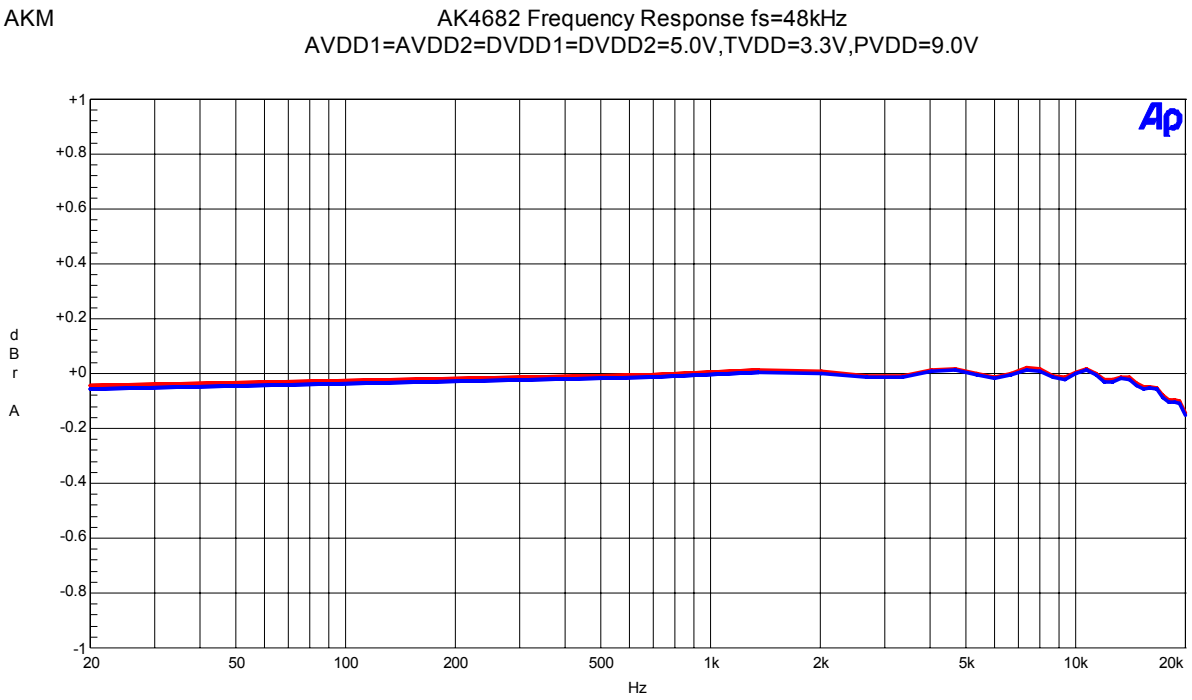


Figure 27. Frequency Response (Input Level=0dBFS)

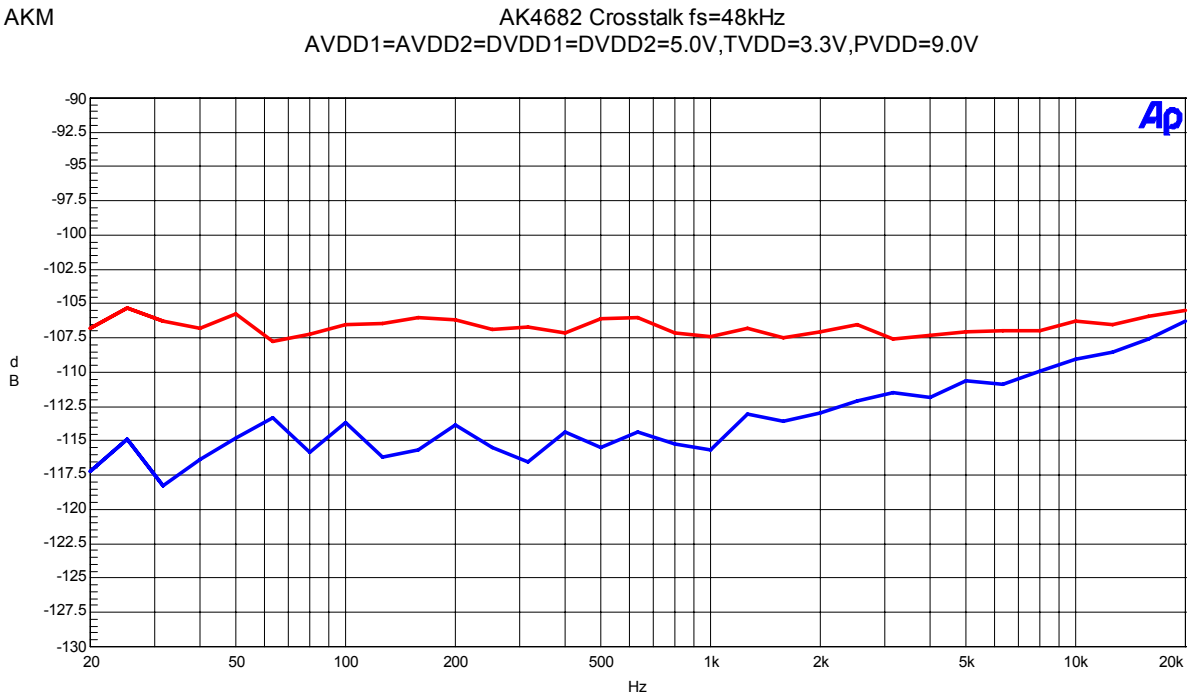


Figure 28. Cross-talk (Input Level=0dBFS)

(DAC fs=96kHz)

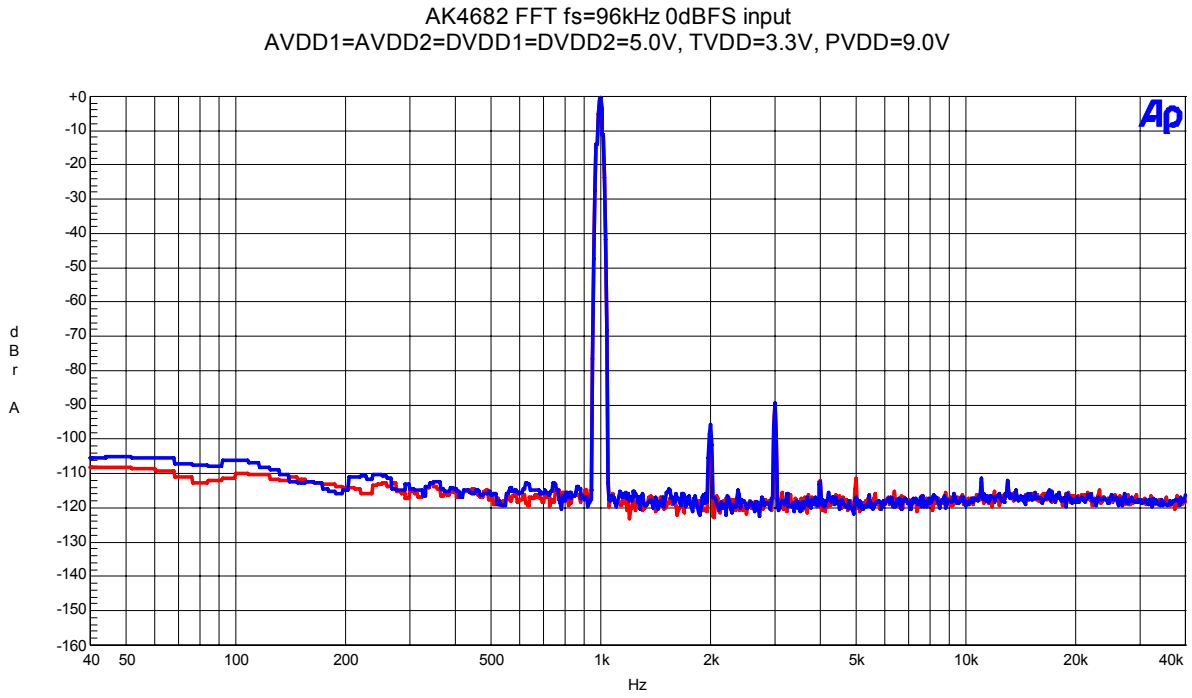


Figure 29. FFT(Input Frequency =1kHz, Input Level=0dBFS)

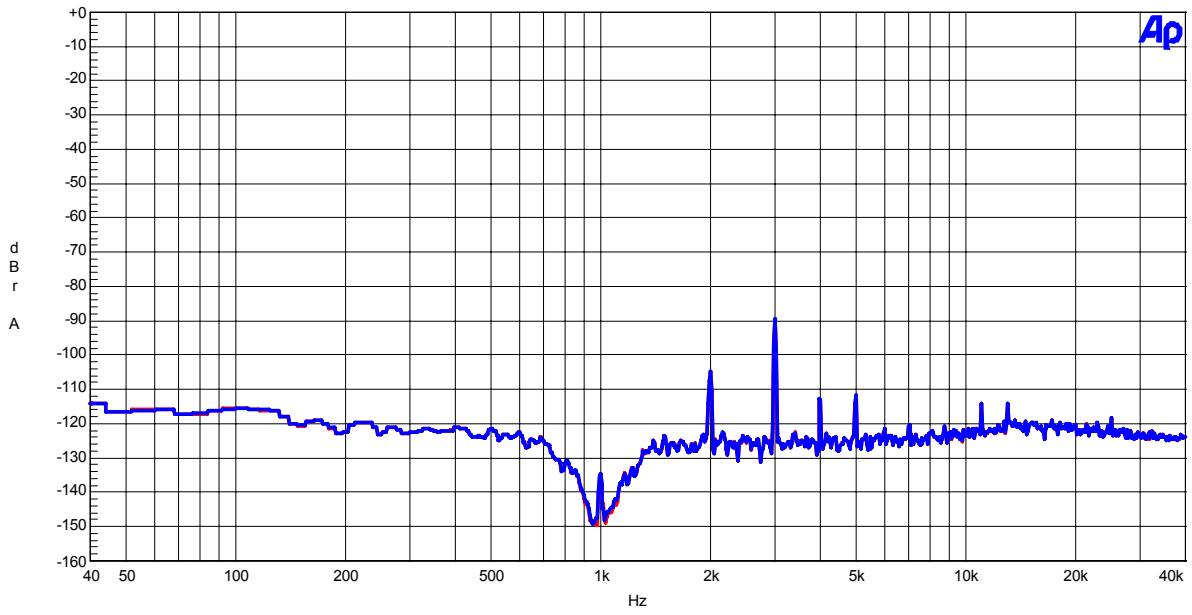


Figure 30. FFT(Input Frequency =1kHz, Input Level=0dBFS,Notch=on)

(DAC fs=96kHz)

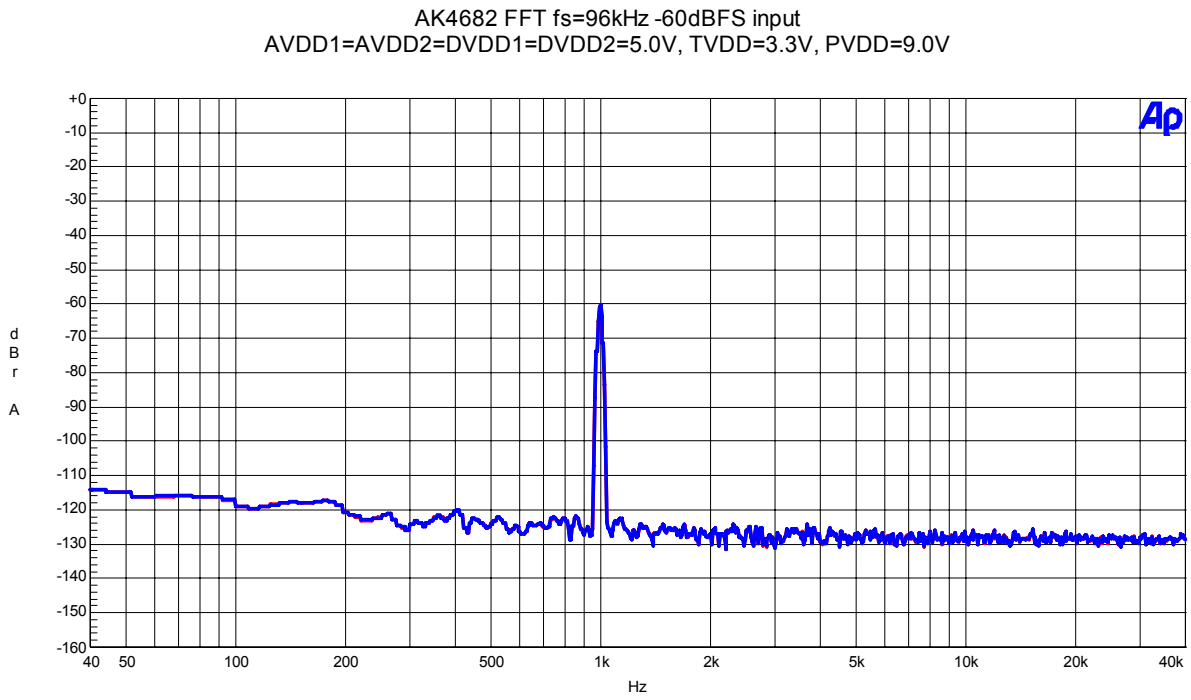


Figure 31. FFT(Input Frequency =1kHz, Input Level=-60dBFS)

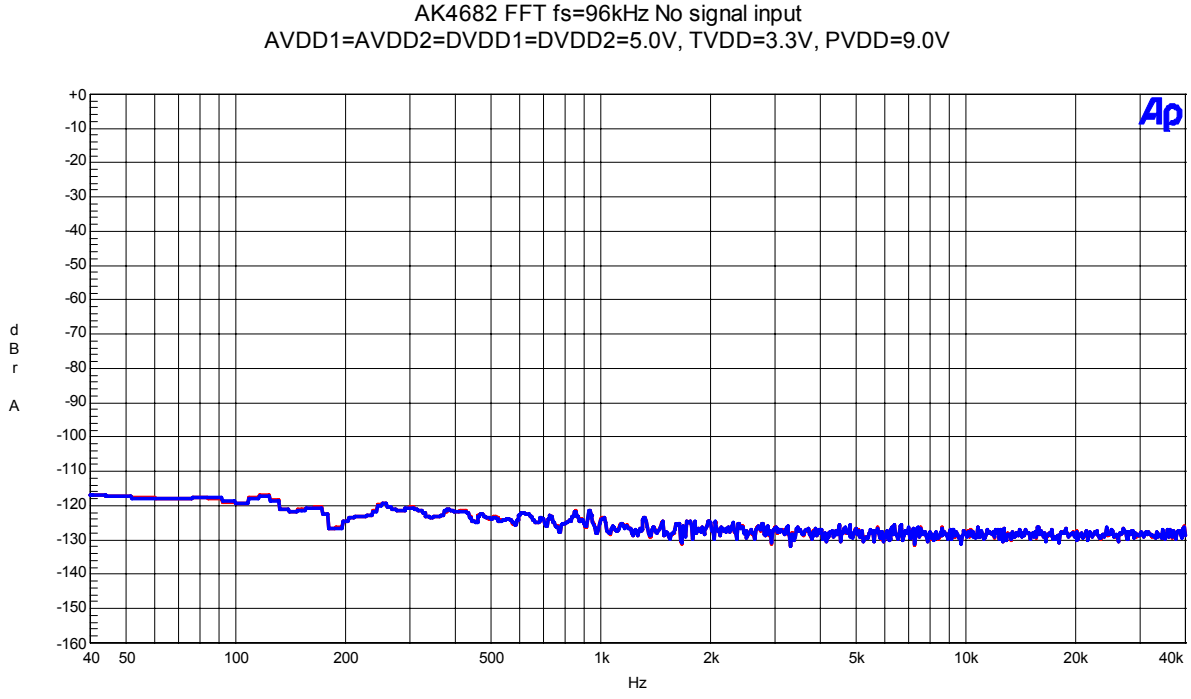
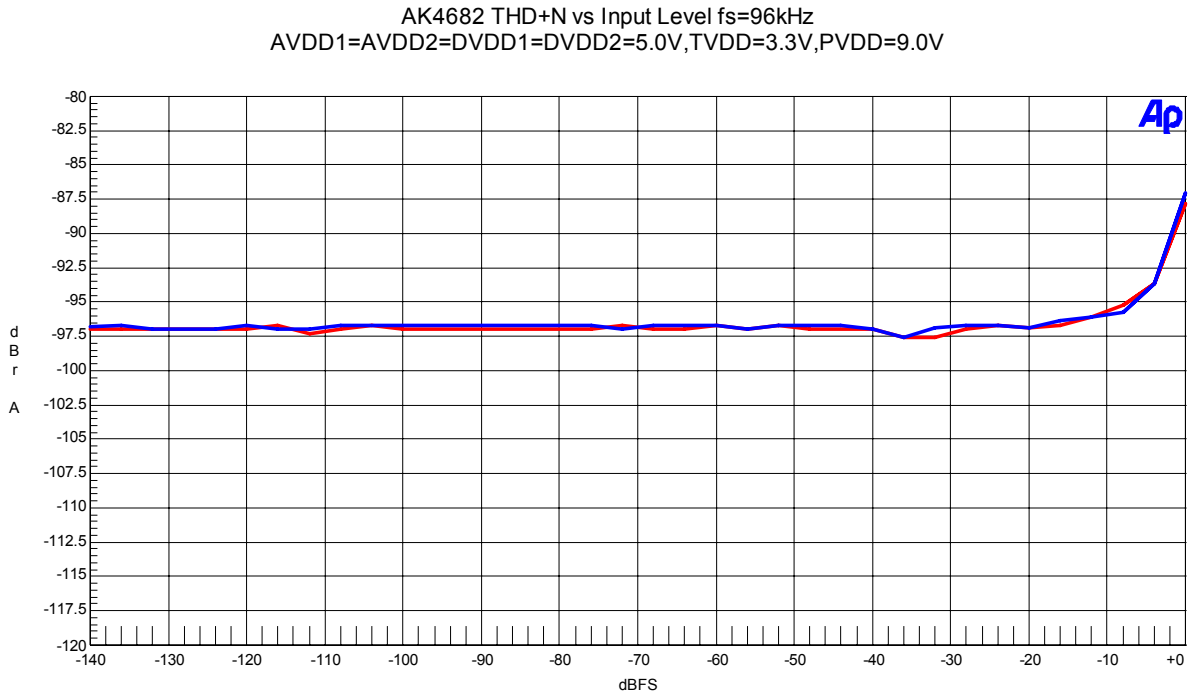


Figure 32. FFT(noise floor)

(DAC fs=96kHz)



FigureFigure 33. THD+N vs Input Level (Input Frequency =1kHz)

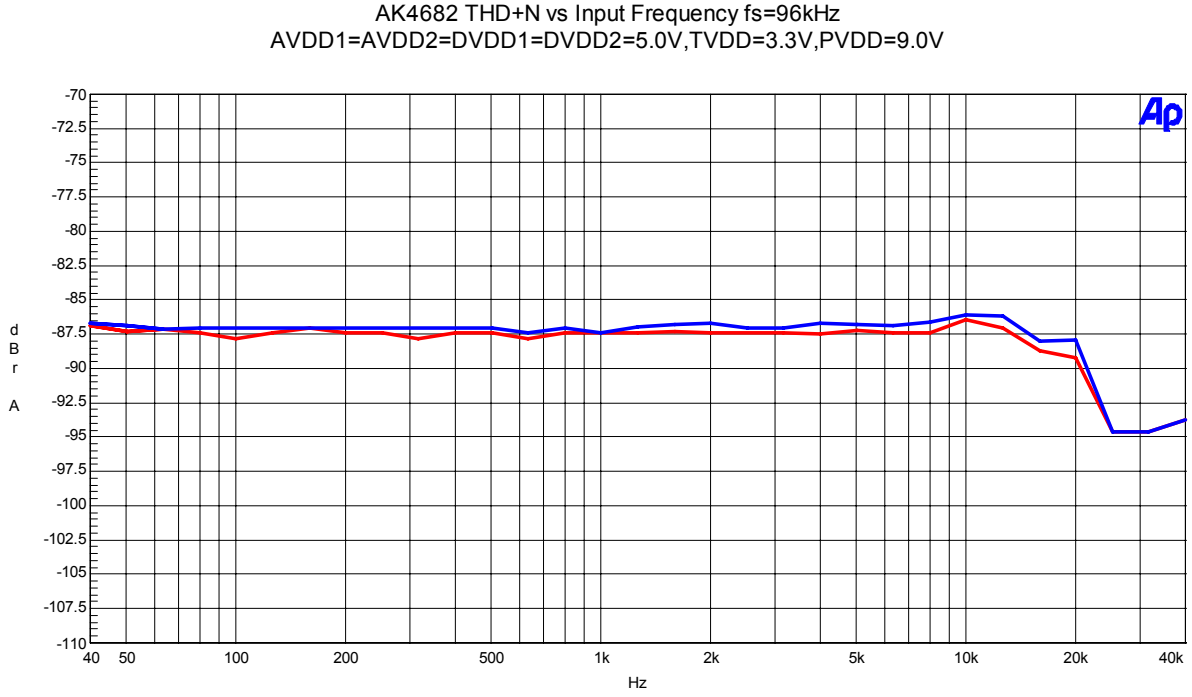


Figure 34. THD+N vs fin (Input Level=0dBFS)

(DAC fs=96kHz)

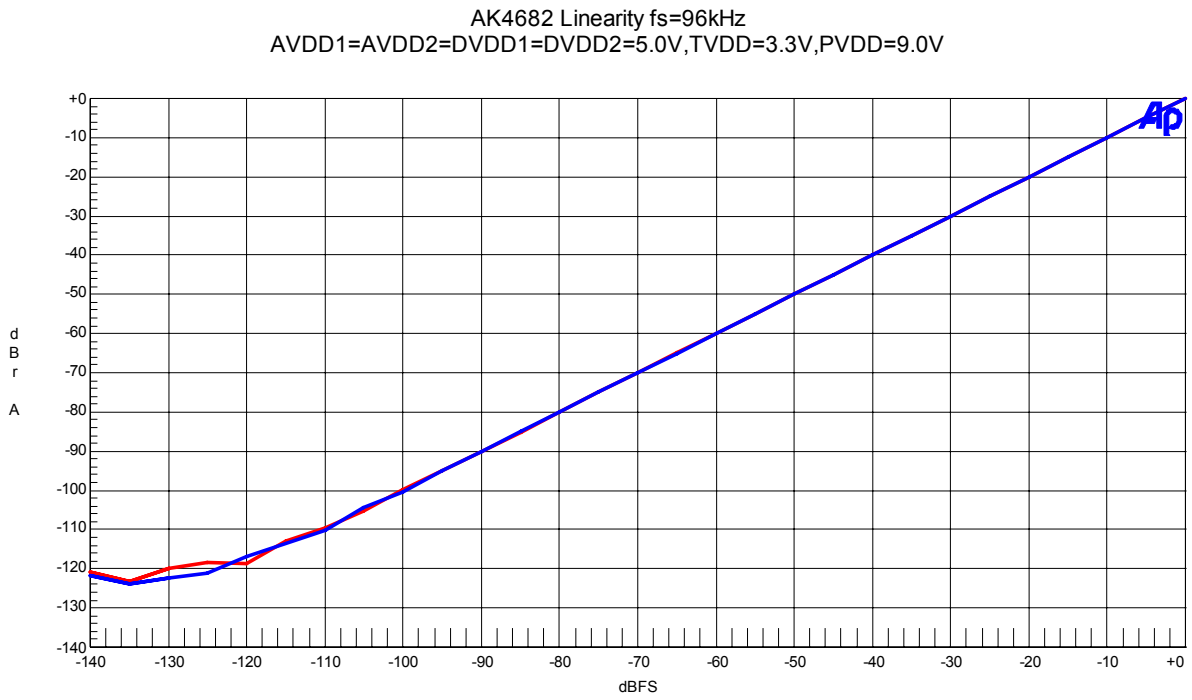


Figure 35. Linearity (Input Frequency =1kHz)

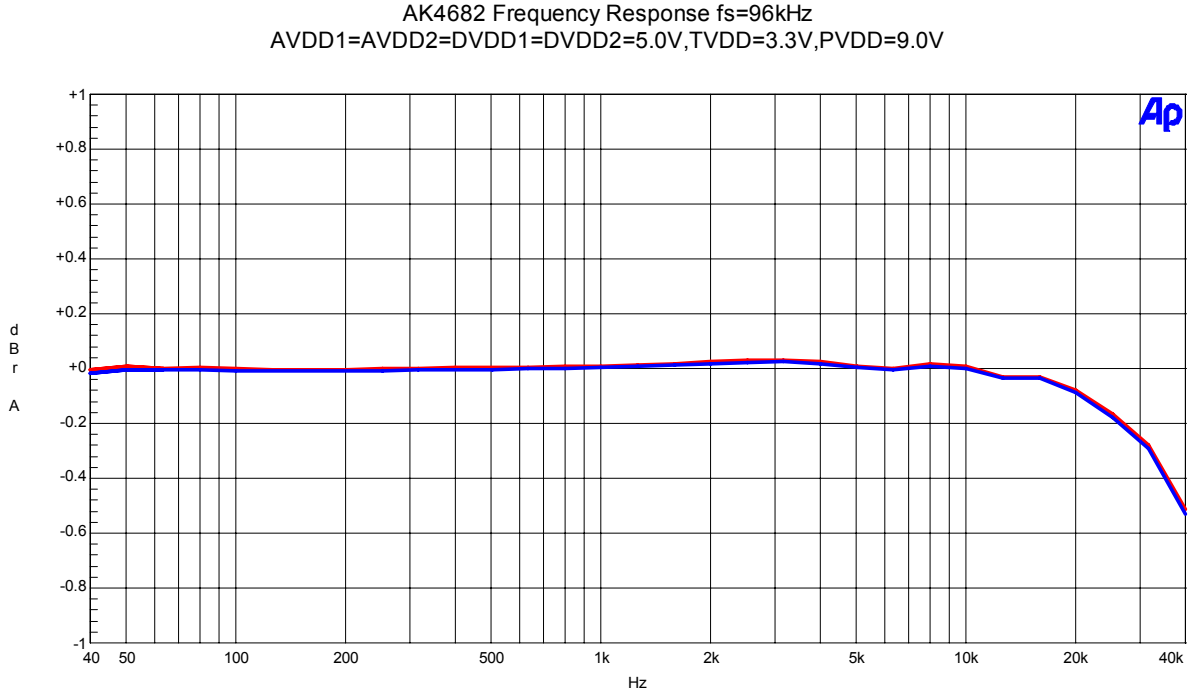


Figure 36. Frequency Response (Input Level=0dBFS)

(DAC fs=96kHz)

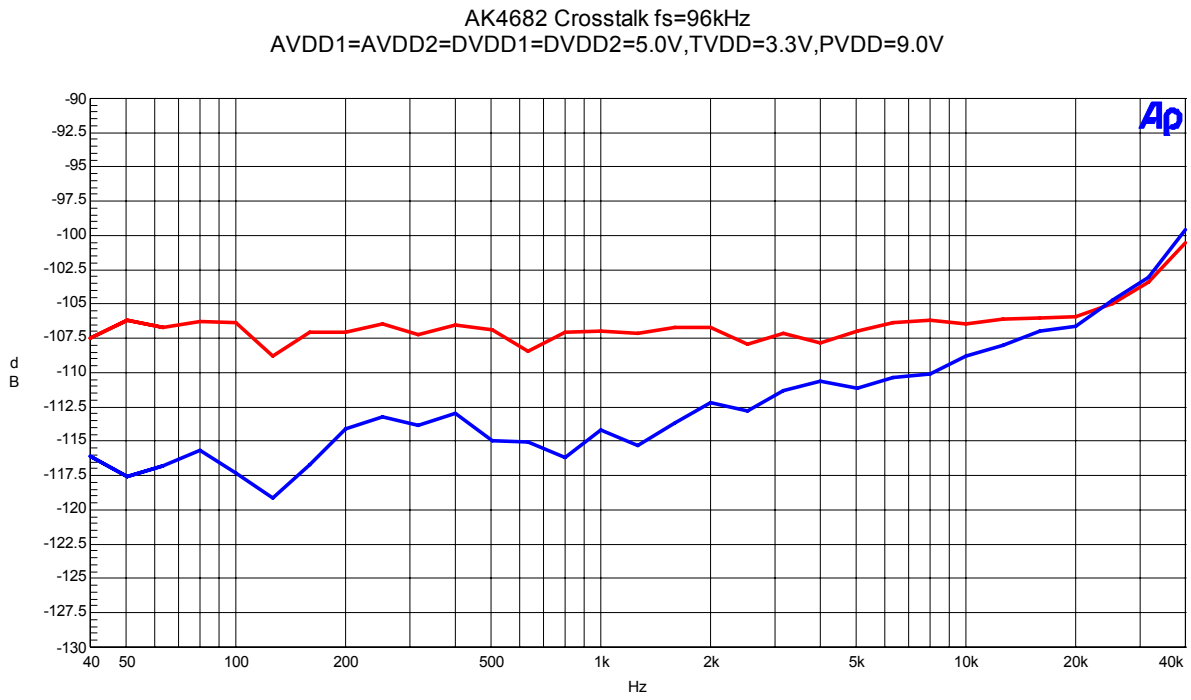


Figure 37. Cross-talk (Input Level=0dBFS)

(DAC fs=192kHz)

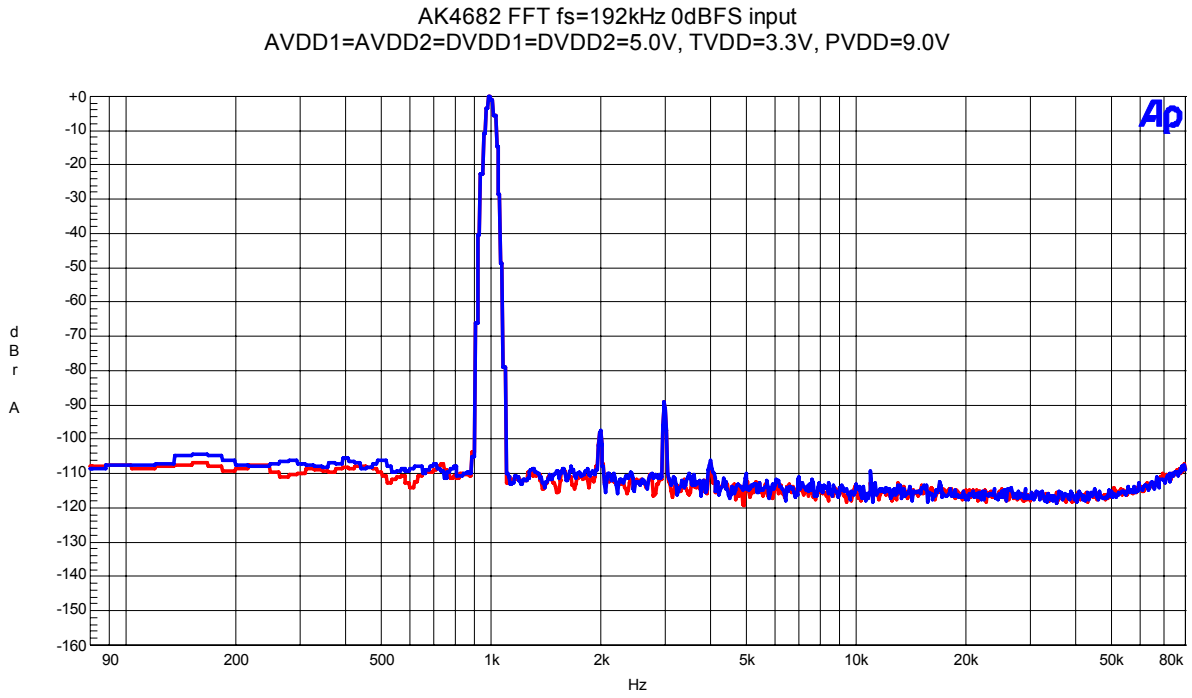


Figure 38. FFT(Input Frequency =1kHz, Input Level=0dBFS)

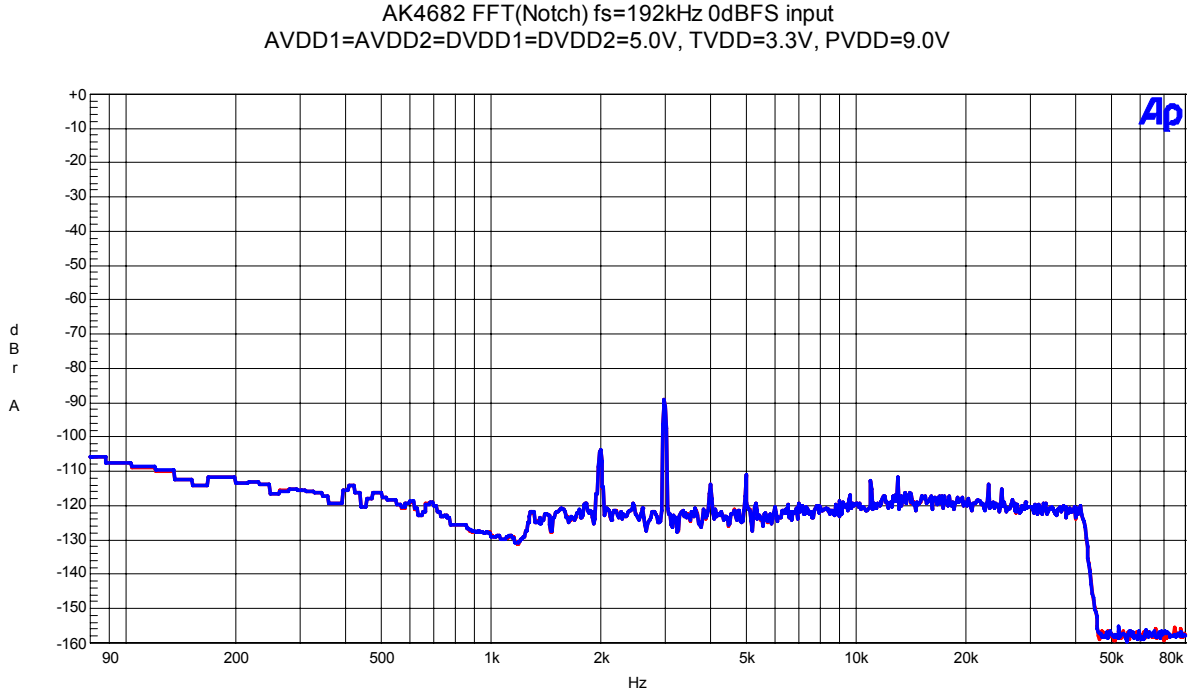


Figure 39. FFT(Input Frequency =1kHz, Input Level=0dBFS,Notch=on,40kHzLPF)

(DAC fs=192kHz)

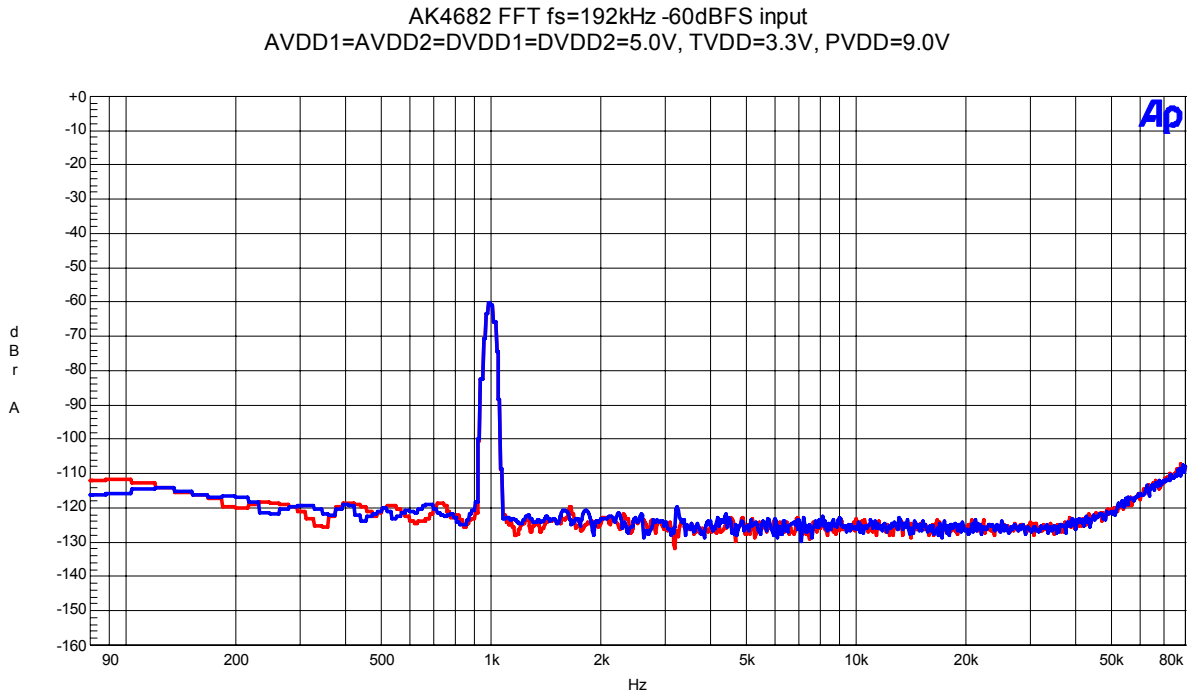


Figure 40. FFT(Input Frequency =1kHz, Input Level=-60dBFS)

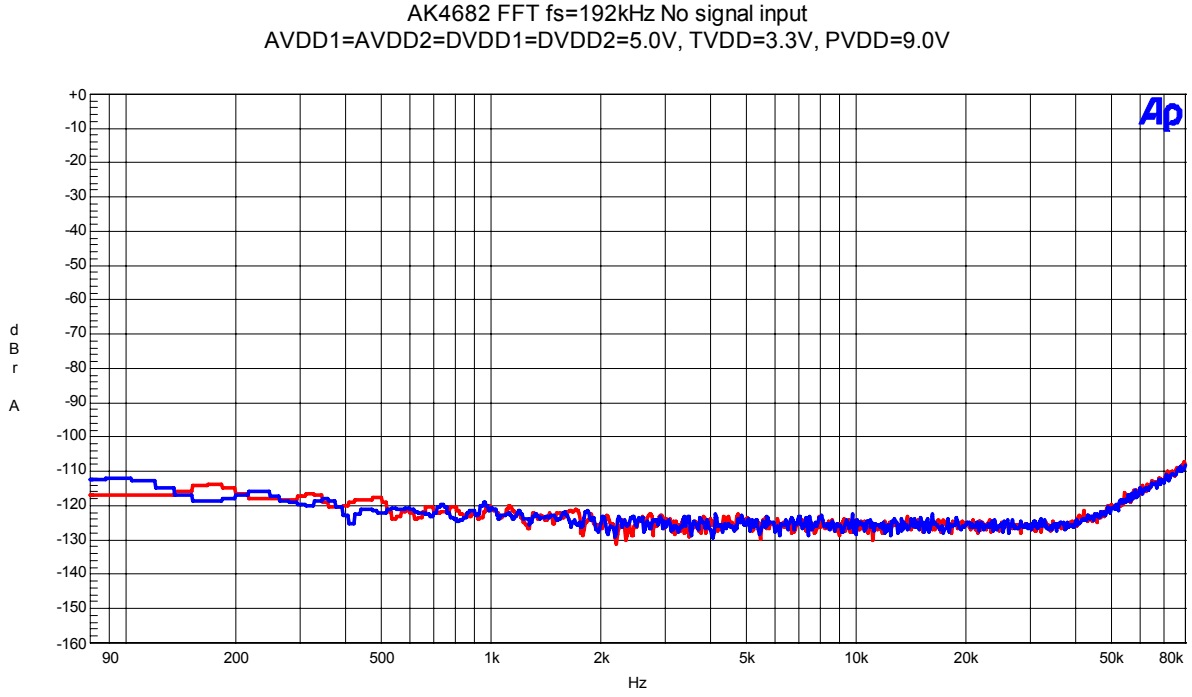


Figure 41. FFT(noise floor)

(DAC fs=192kHz)

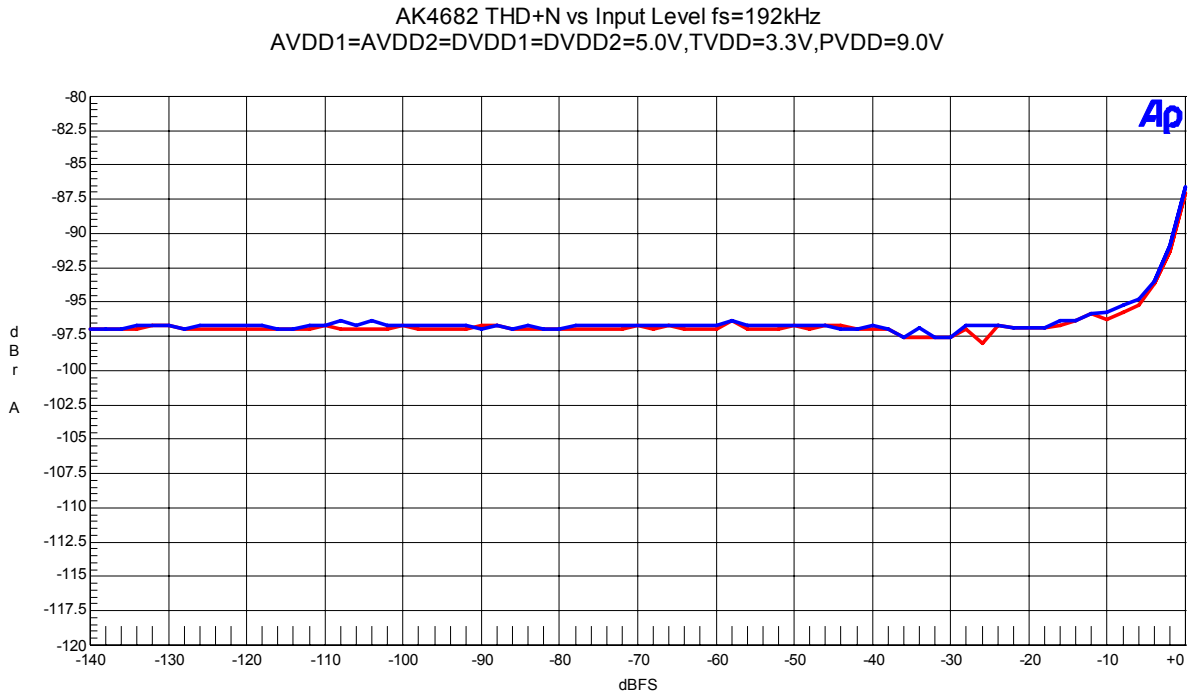


Figure 42. THD+N vs Input Level (Input Frequency =1kHz)

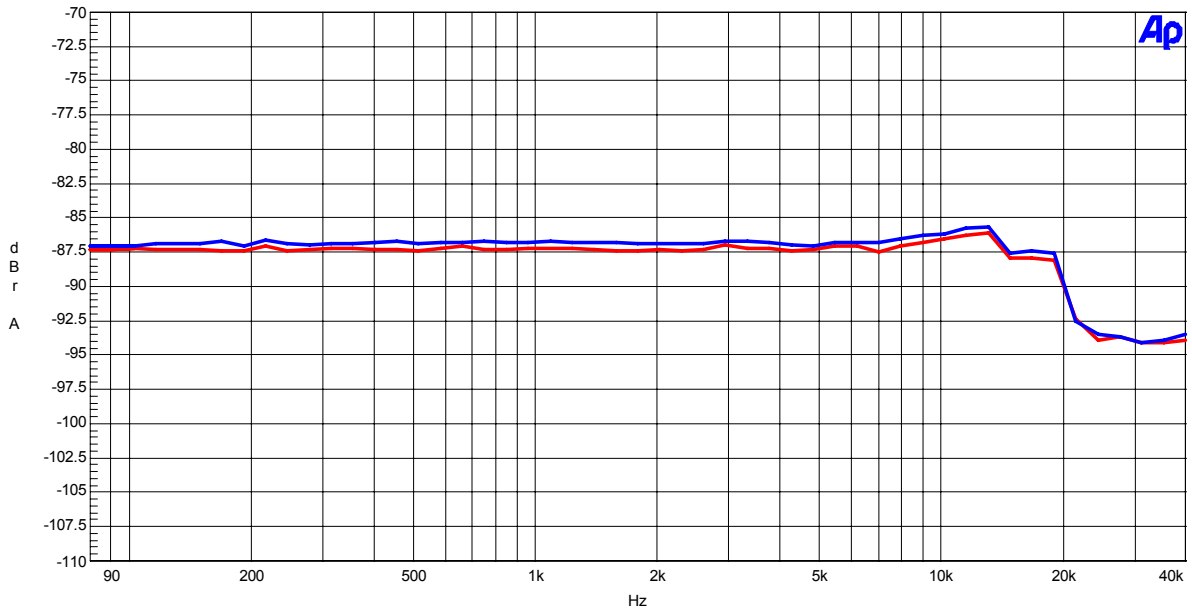


Figure 43. THD+N vs Input Frequency (Input Level=0dBFS)

(DAC fs=192kHz)

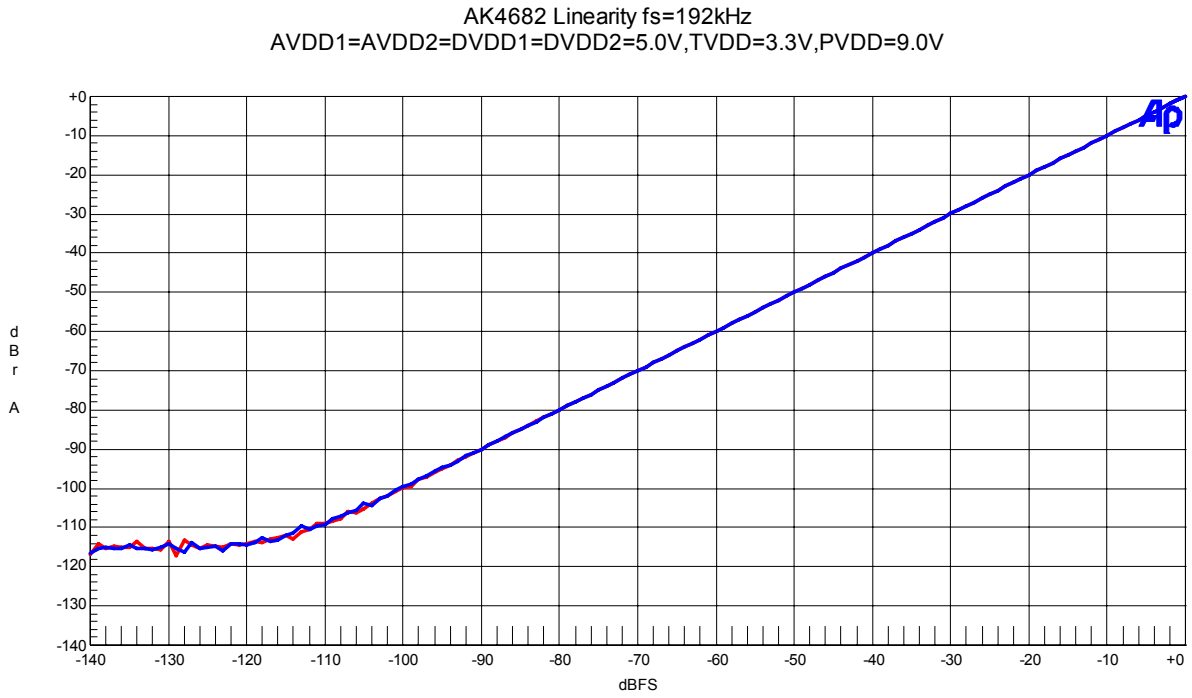


Figure 44. Linearity (f Input Frequency =1kHz)

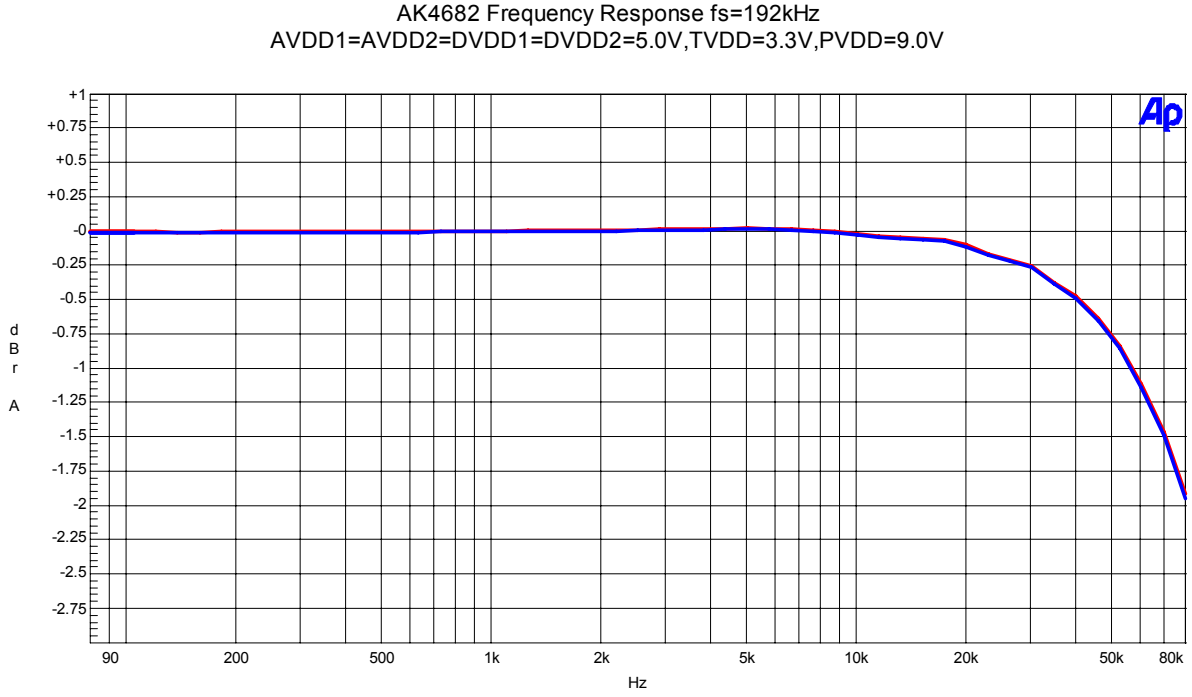


Figure 45. Frequency Response (Input Level=0dBFS)

(DAC fs=192kHz)

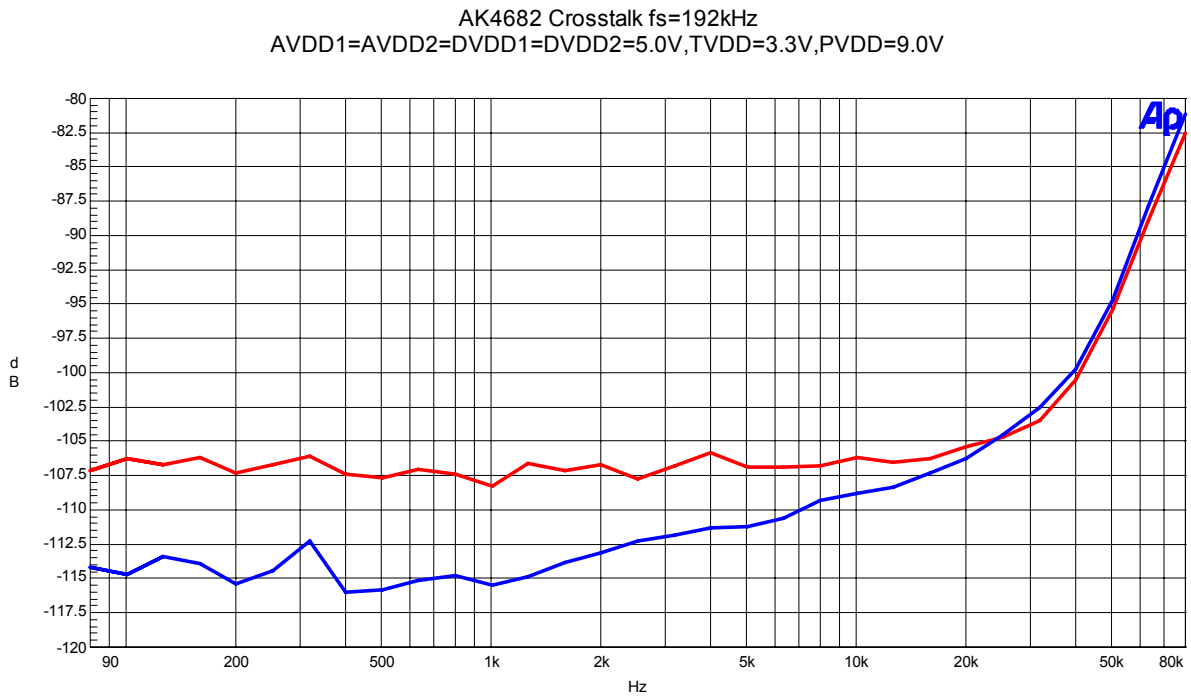
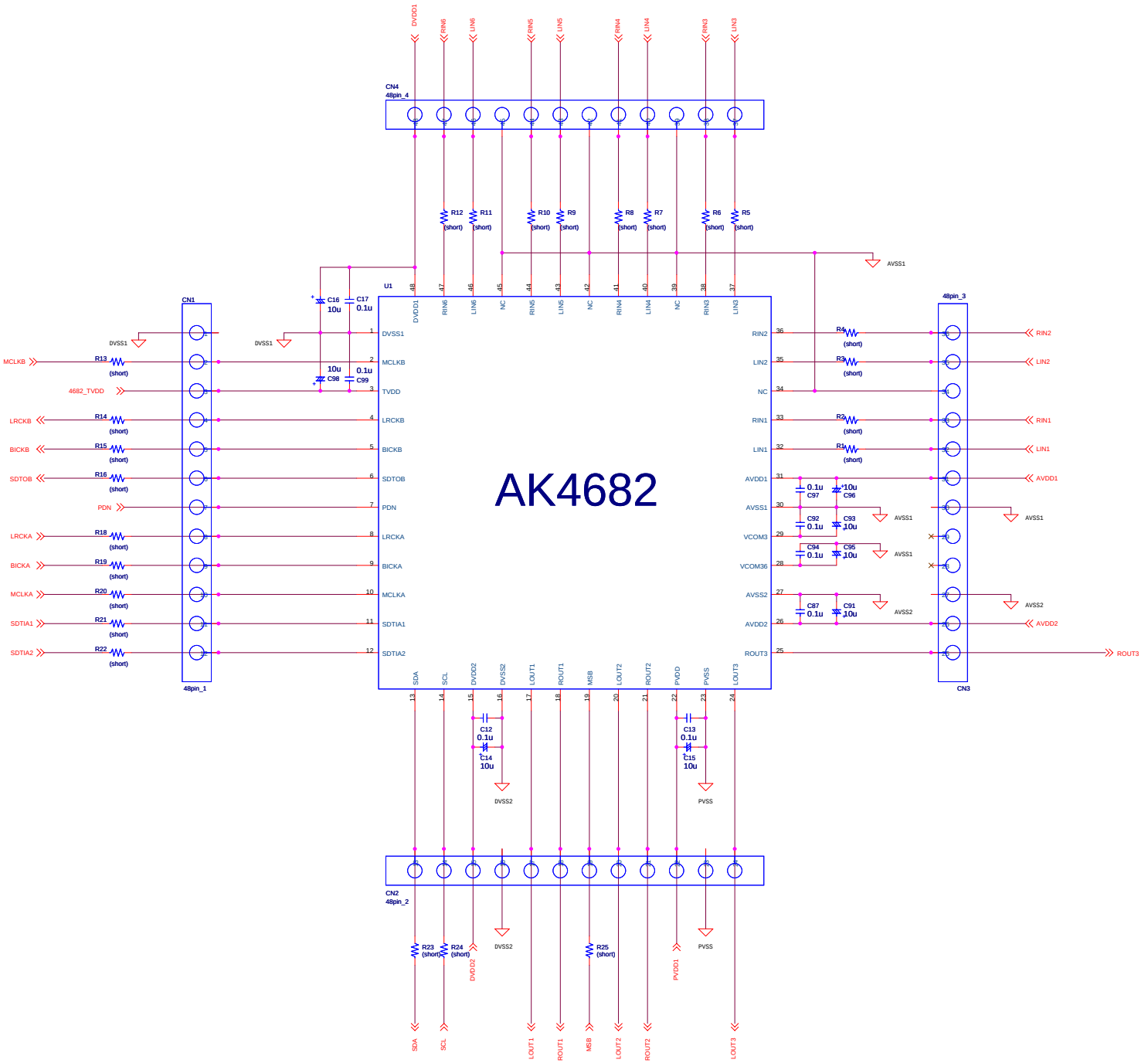


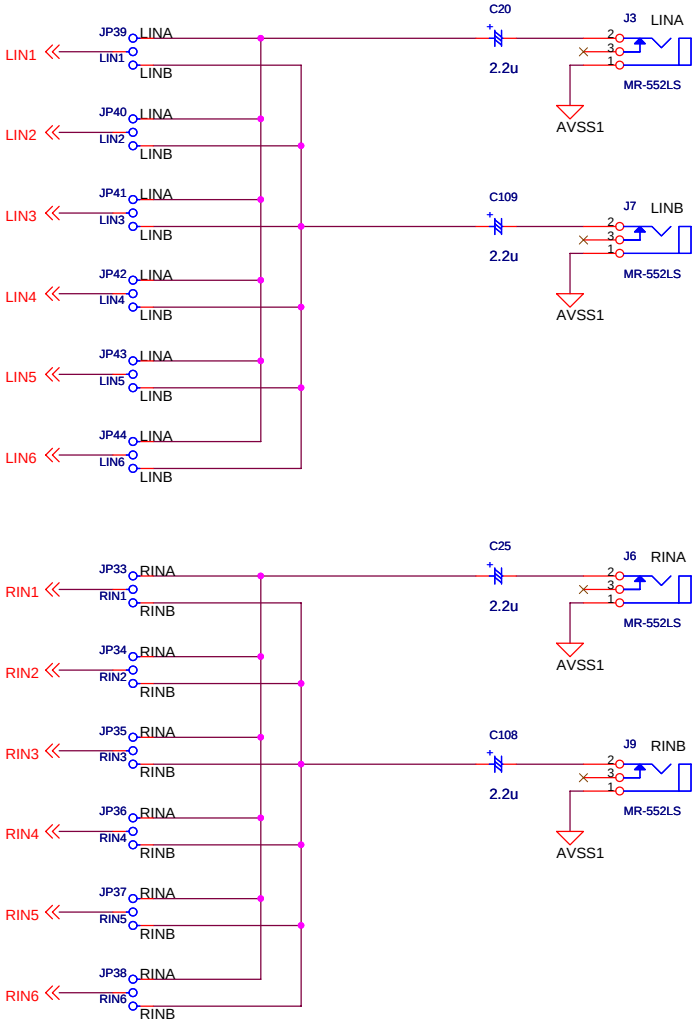
Figure 46. Cross-talk (Input Level=0dBFS

Revision History

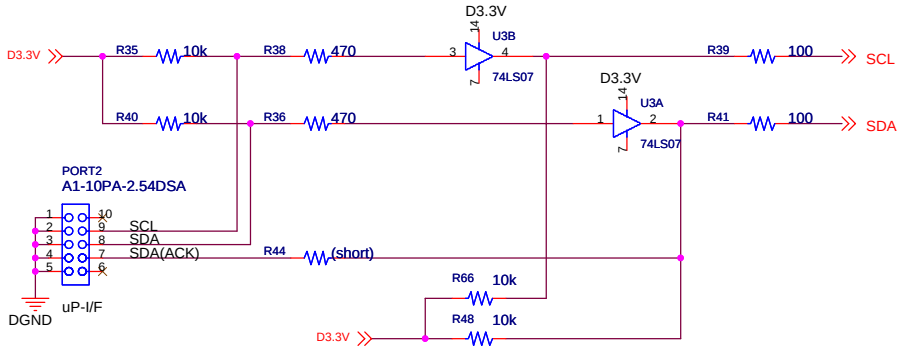
Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
07/02/19	KM086400	0	First Edition	

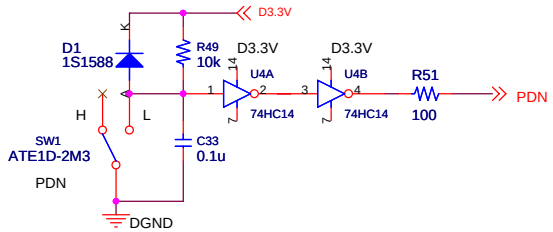


Title	AKD4682-A	
Size A2	Document Number AK4682	Rev 0
Date: Monday, November 20, 2006	Sheet 1 of 1	



Title	AKD4682-A	
Size A3	Document Number LIN/RIN	Rev 0
Date: Monday, September 11, 2006	Sheet 1 of 1	





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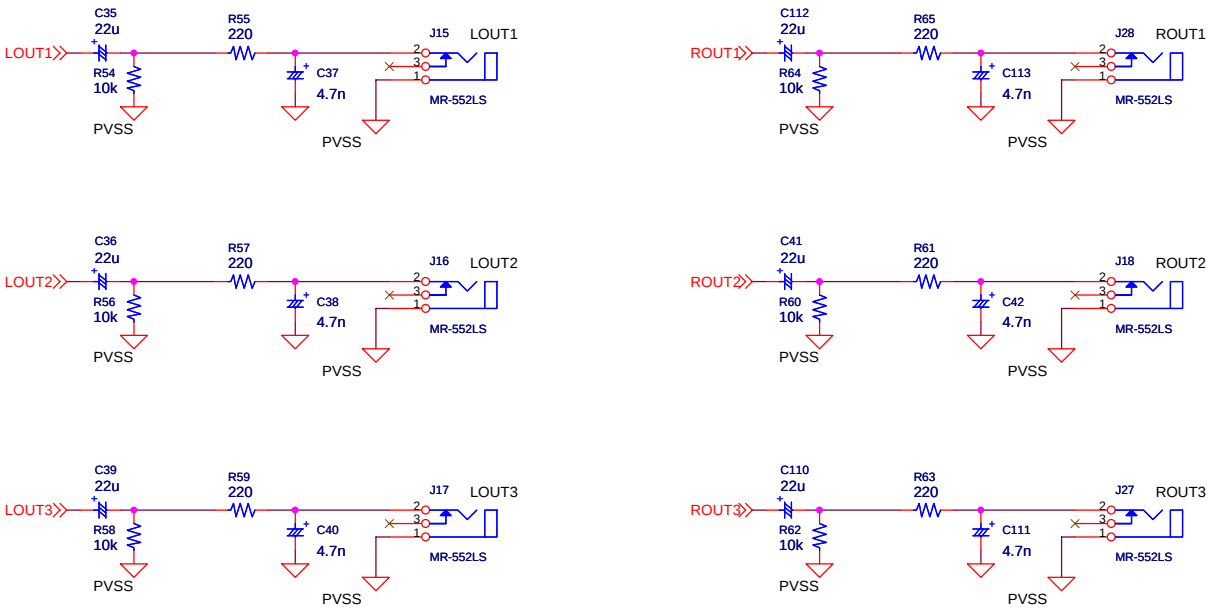

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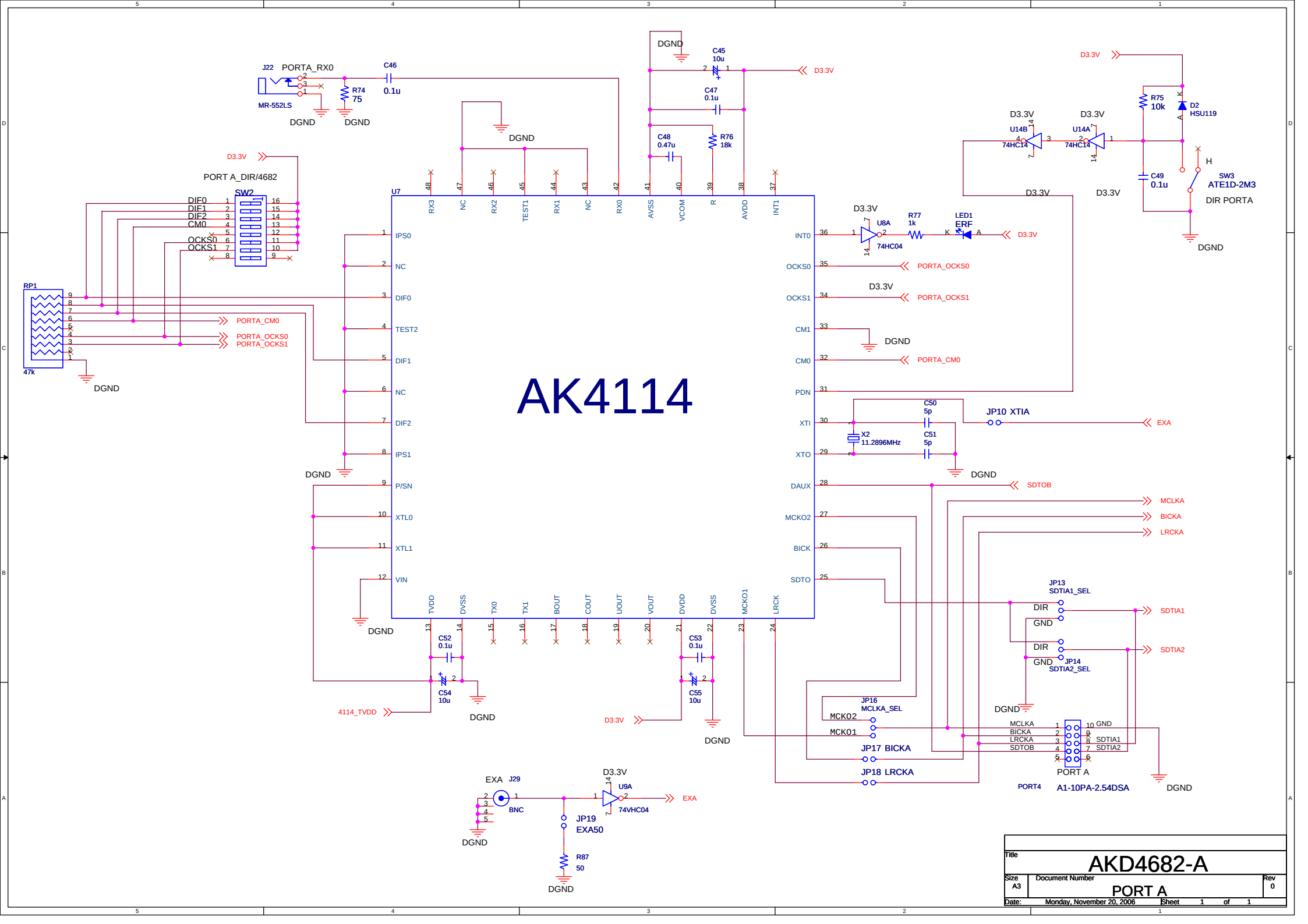

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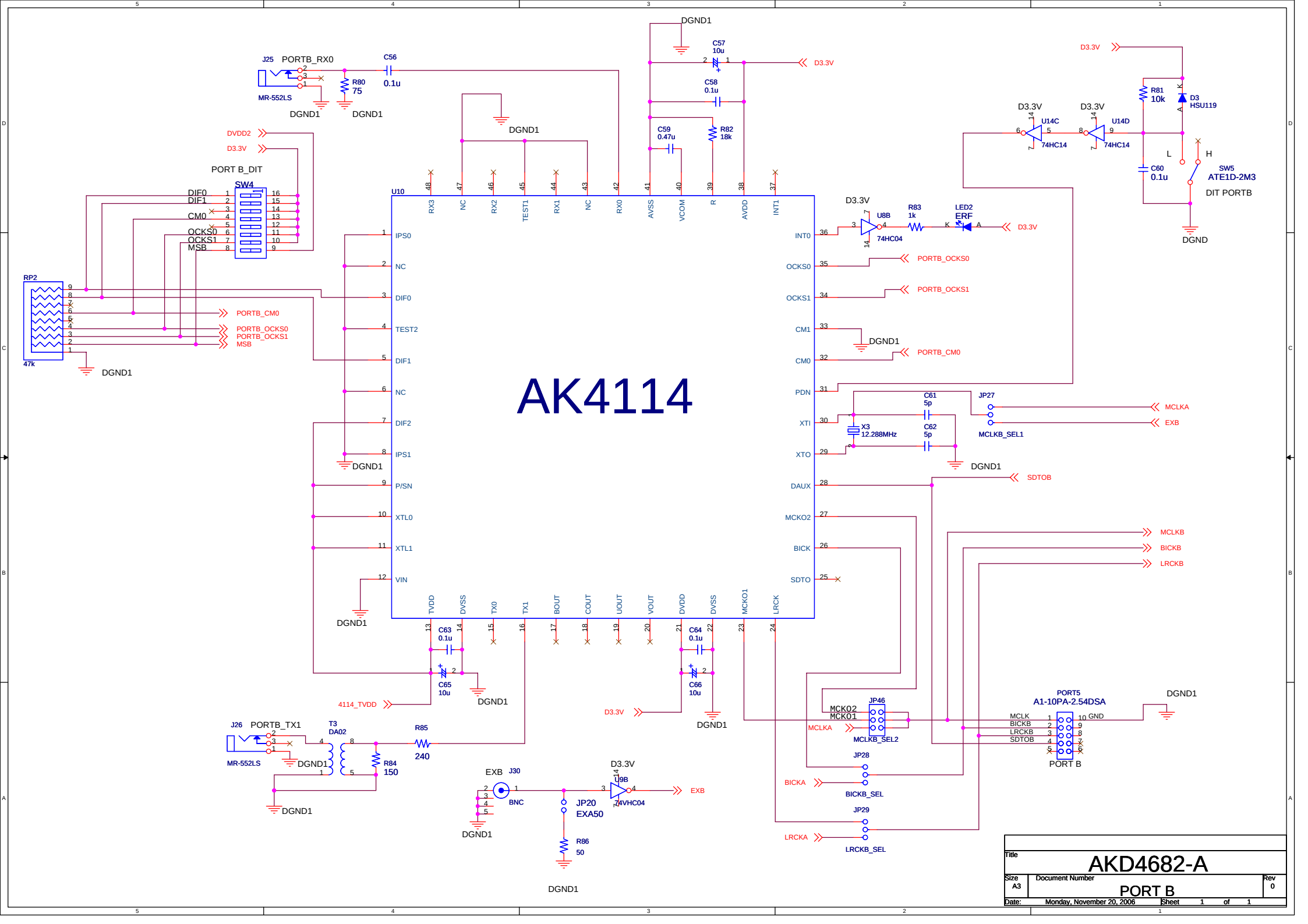

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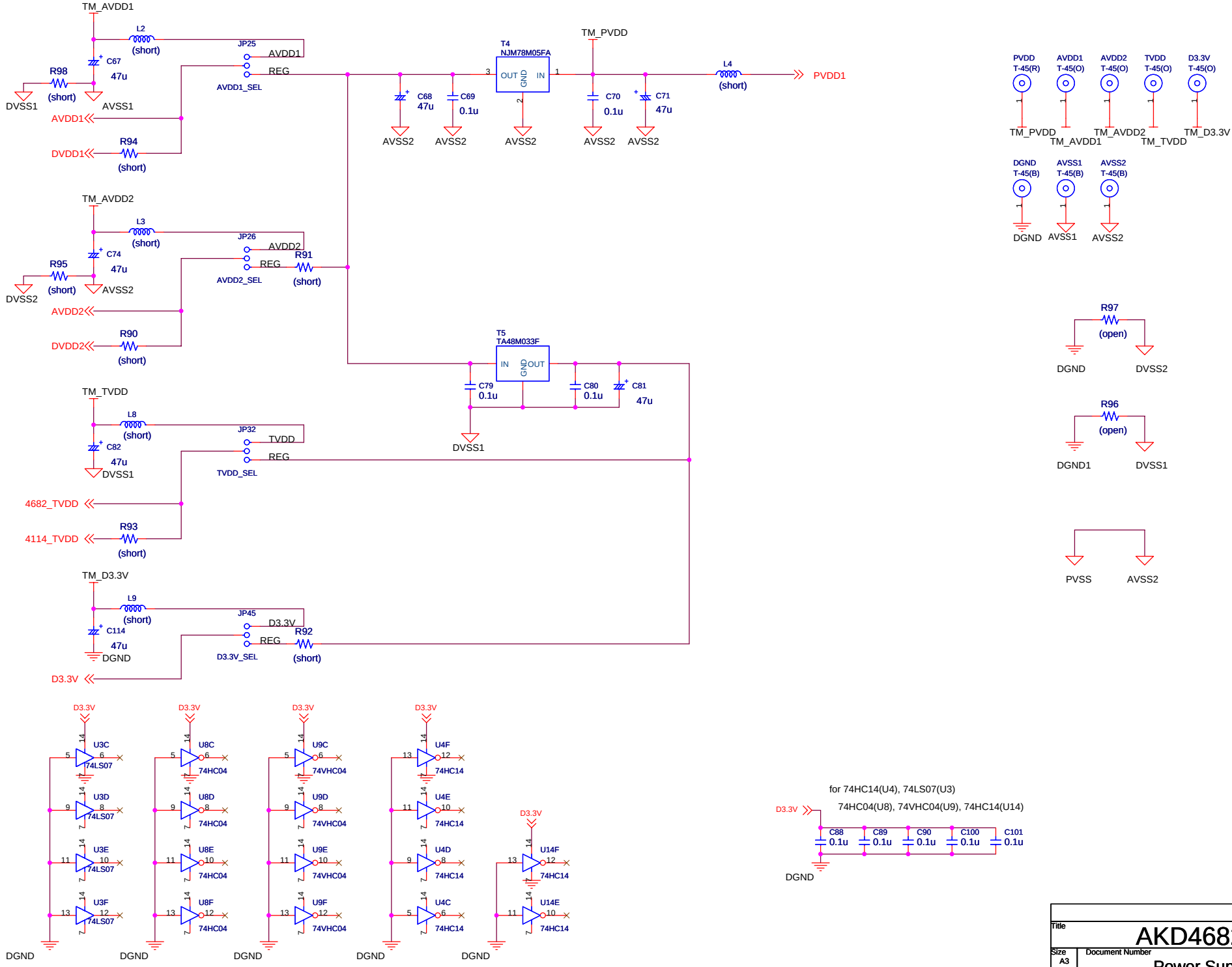
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IN
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47u
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R90
(short)
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C114
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(short)
D3.3V
PVDD
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(open)
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DGND
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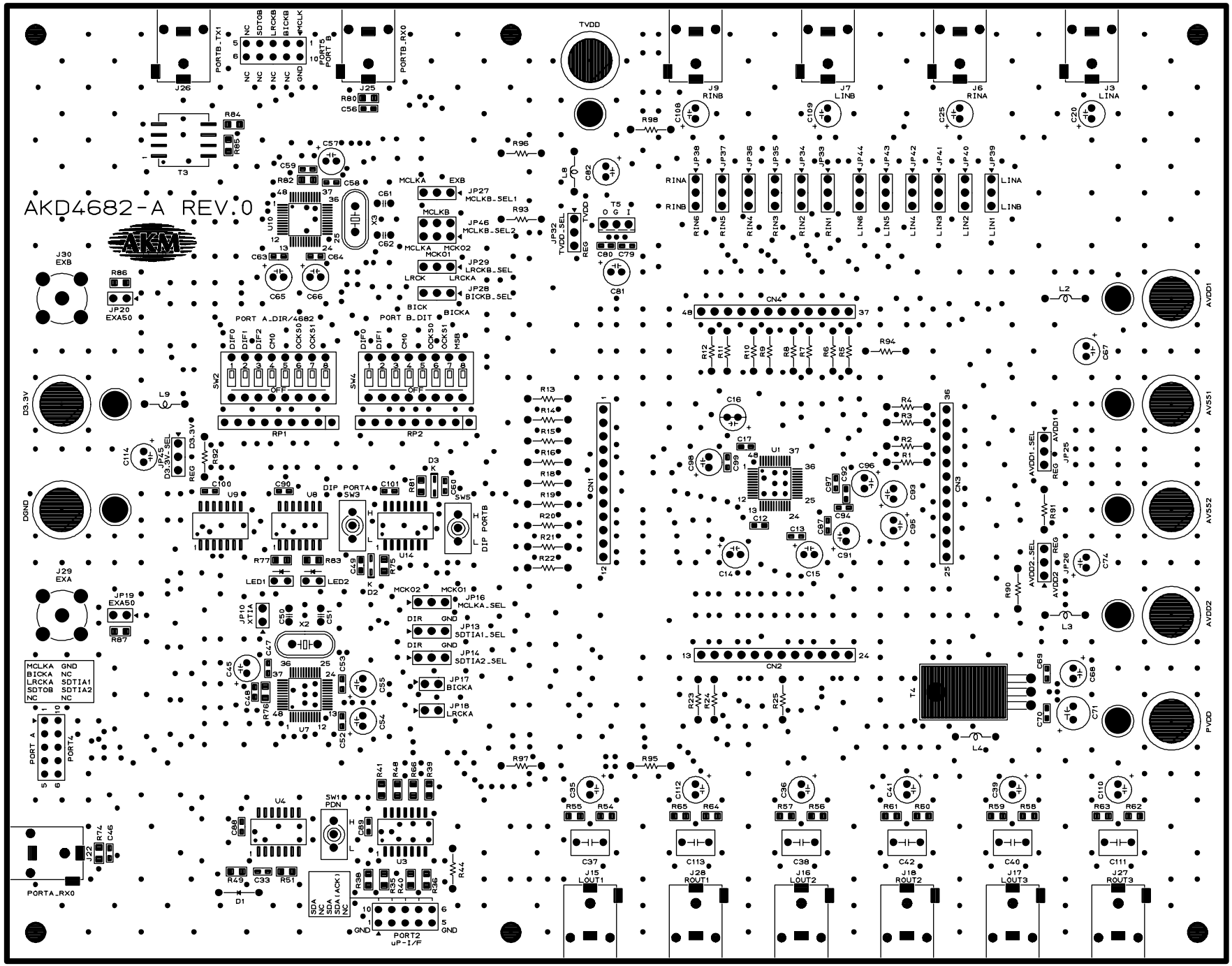

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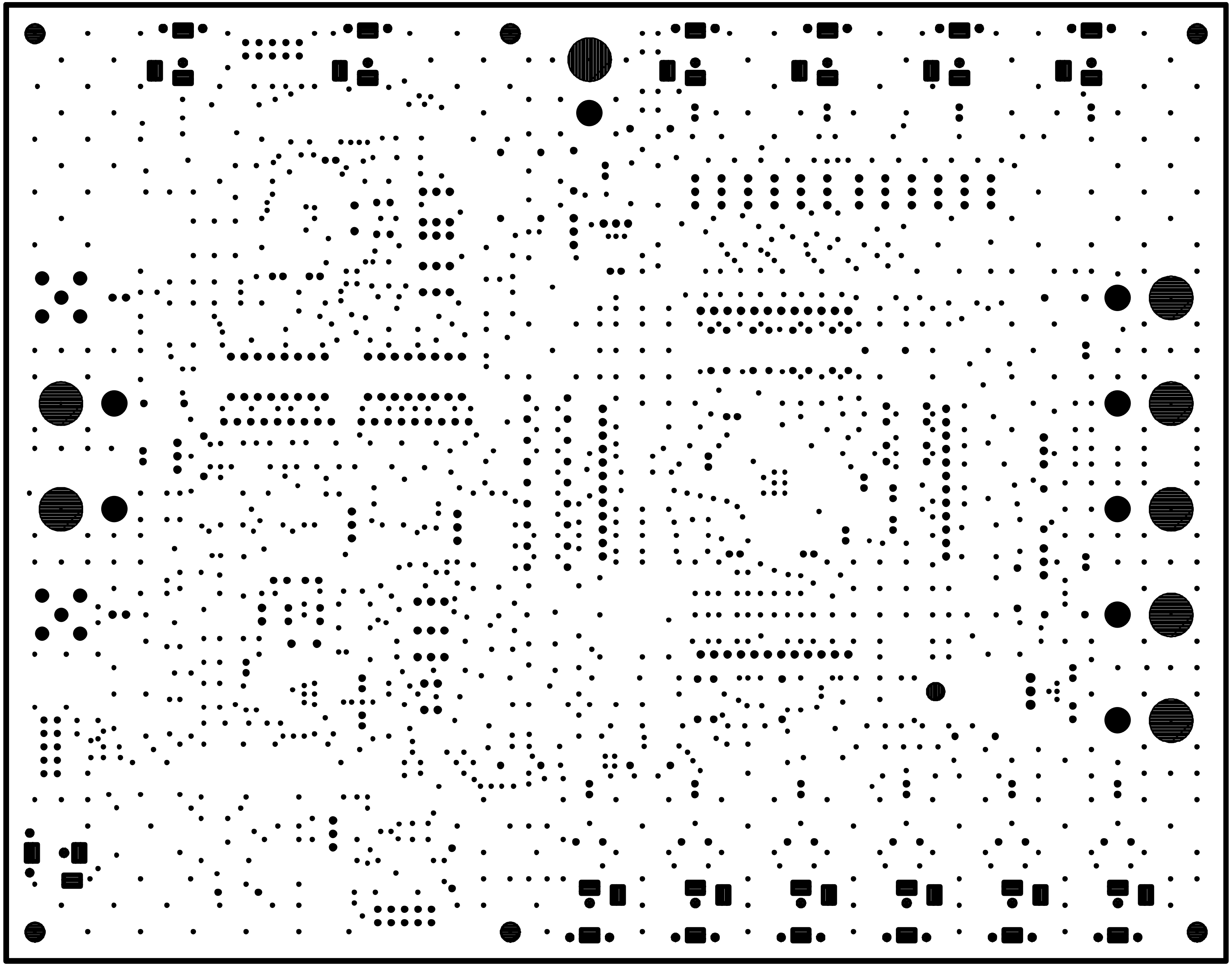

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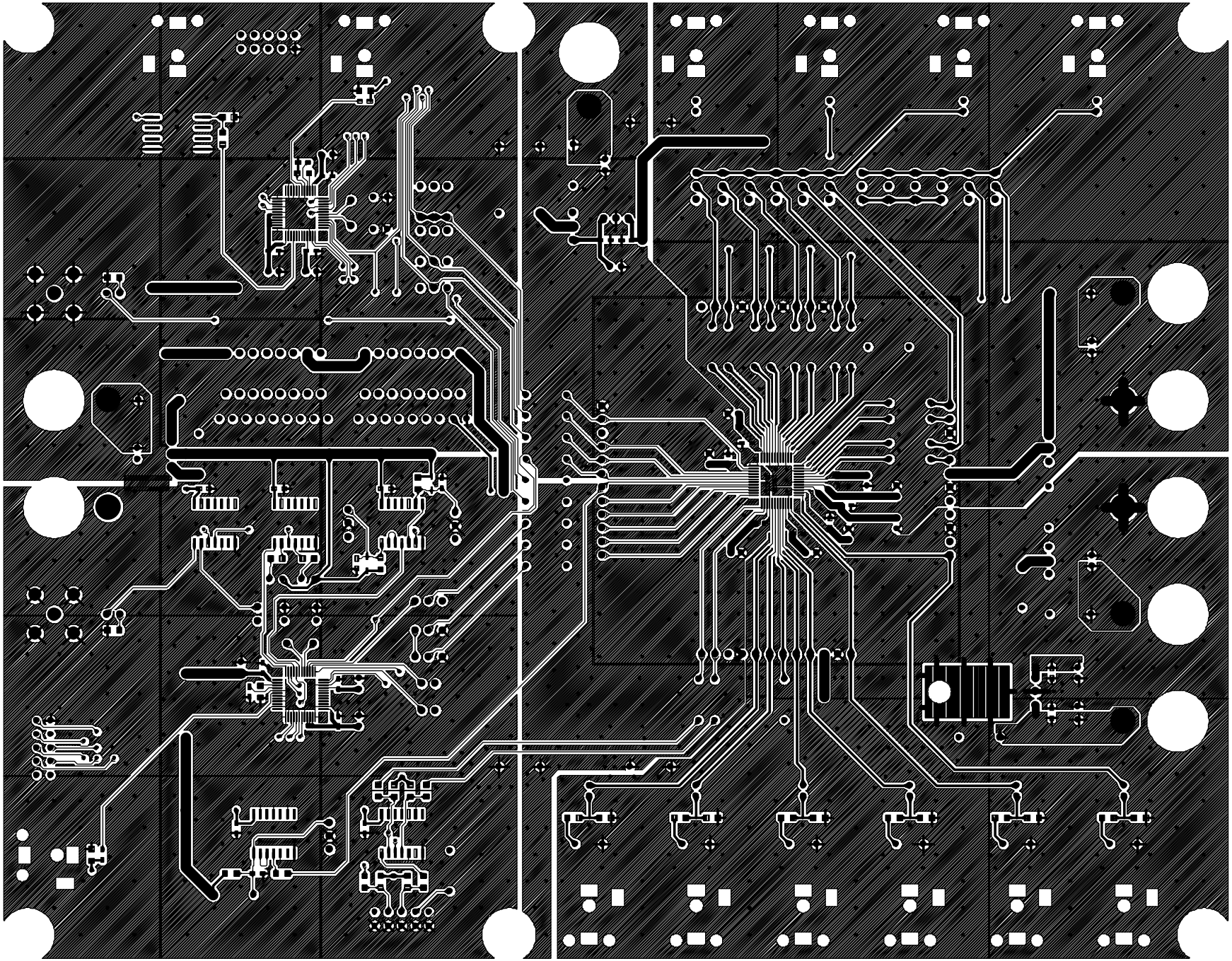

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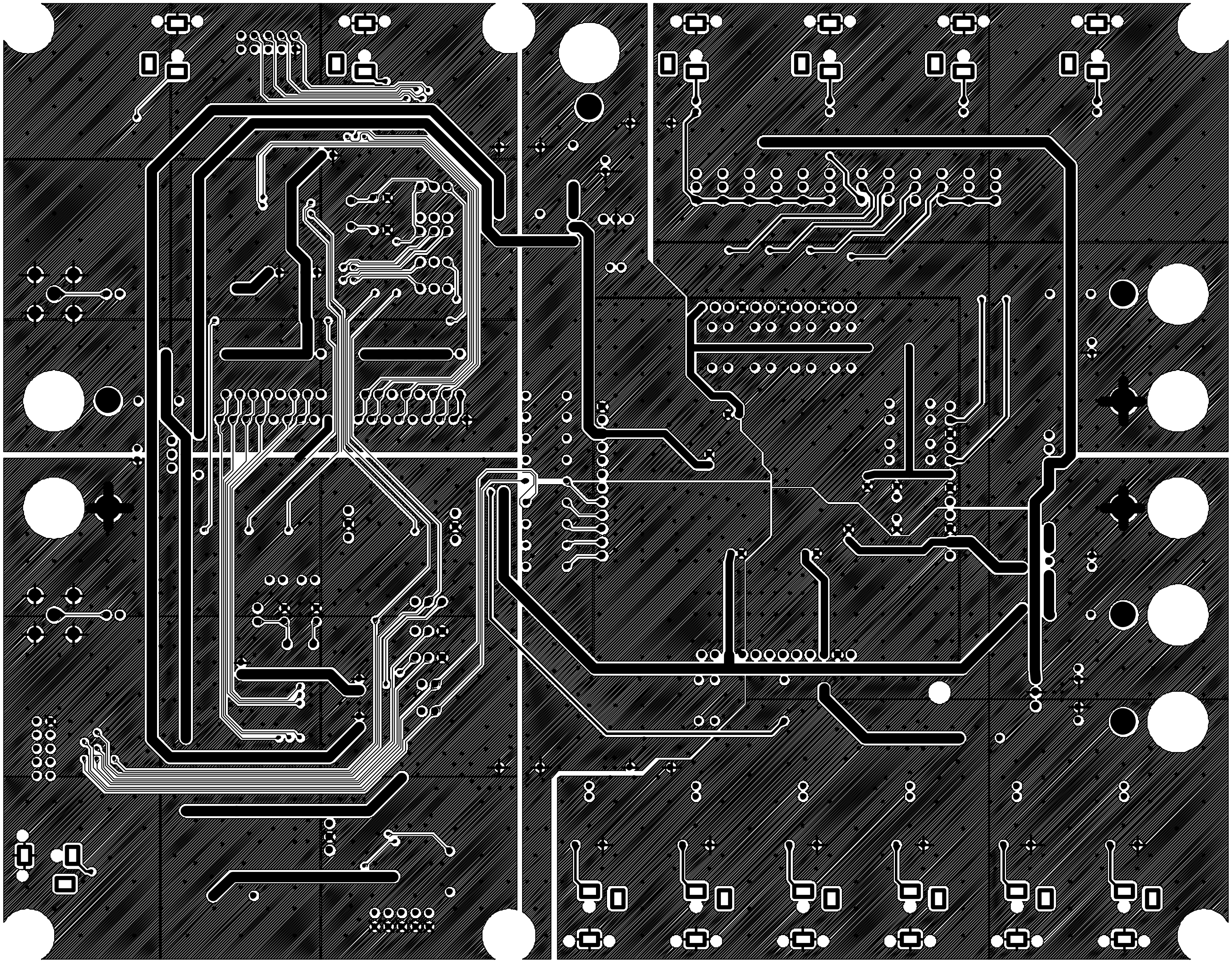

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