50 MHz to 6 GHz RF/IF Gain Block

ADL5542

FEATURES

Fixed gain of 20 dB
Operation up to 6 GHz
Input/output internally matched to 50 Ω
Integrated bias control circuit
Output IP3
- **46 dBm at 500 MHz**
- **40 dBm at 900 MHz**

Output 1 dB compression: 20.6 dB at 900 MHz
Noise figure of 3 dB at 900 MHz
Single 5 V power supply
Small footprint 8-lead LFCSP
Pin compatible with 15 dB gain ADL5541
1 kV ESD (Class 1C)

FUNCTIONAL BLOCK DIAGRAM

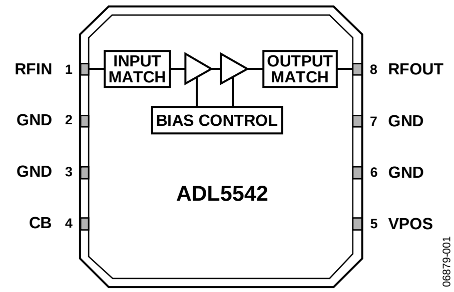

Figure 1.

GENERAL DESCRIPTION

The ADL5542 is a broadband 20 dB linear amplifier that operates at frequencies up to 6 GHz. The device can be used in a wide variety of CATV, cellular, and instrumentation equipment.

The ADL5542 provides a gain of 20 dB that is stable over frequency, temperature, power supply, and from device to device. The device is internally matched to 50 Ω with an input return loss of 10 dB or better, up to 6 GHz. Only input/output ac coupling capacitors, power supply decoupling capacitors, and an external inductor are required for operation.

The ADL5542 is fabricated on an InGaP HBT process and has an ESD rating of 1 kV (Class 1C). The device is packaged in a 3 mm × 3 mm LFCSP that uses an exposed paddle for excellent thermal impedance.

The ADL5542 consumes 93 mA on a single 5 V supply and is fully specified for operation from −40°C to +85°C.

A fully populated RoHS-compliant evaluation board is available.

The ADL5541 is a companion part that offers a gain of 15 dB in a pin-compatible package.

Rev. A

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REVISION HISTORY

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7/07—Revision 0: Initial Version

SPECIFICATIONS

VPOS = 5 V and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		50		6000	MHz
Gain (S21)	900 MHz		19.7		dB
Input Return Loss (S11)	Frequency 500 MHz to 5 GHz		−15		dB
Output Return Loss (S22)	Frequency 500 MHz to 5 GHz		−10		dB
Reverse Isolation (S12)			−22		dB
FREQUENCY = 100 MHz					
Gain			20.2		dB
Output 1 dB Compression Point			19.6		dBm
Output Third-Order Intercept	Δf = 1 MHz, output power (P_{OUT}) = 0 dBm per tone		38		dBm
Noise Figure			2.7		dB
FREQUENCY = 500 MHz					
Gain		18.4	19.5	20.8	dB
vs. Frequency	±50 MHz		±0.15		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.1		dB
vs. Supply	4.75 V to 5.25 V		±0.02		dB
Output 1 dB Compression Point			20.6		dBm
Output Third-Order Intercept	Δf = 1 MHz, output power (P_{OUT}) = 3 dBm per tone		46		dBm
Noise Figure			2.8	3.2	dB
FREQUENCY = 900 MHz					
Gain		19.2	19.7	20.8	dB
vs. Frequency	±50 MHz		±0.03		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.14		dB
vs. Supply	4.75 V to 5.25 V		±0.02		dB
Output 1 dB Compression Point			20.6		dBm
Output Third-Order Intercept	Δf = 1 MHz, output power (P_{OUT}) = 0 dBm per tone		40		dBm
Noise Figure			3.0	3.3	dB
FREQUENCY = 2000 MHz					
Gain		18	18.7	19.4	dB
vs. Frequency	±50 MHz		±0.05		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.23		dB
vs. Supply	4.75 V to 5.25 V		±0.04		dB
Output 1 dB Compression Point			18		dBm
Output Third-Order Intercept	Δf = 1 MHz, output power (P_{OUT}) = 0 dBm per tone		39		dBm
Noise Figure			3.2	3.6	dB
FREQUENCY = 2400 MHz					
Gain		17.7	18.3	18.9	dB
vs. Frequency	±50 MHz		±0.05		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.24		dB
vs. Supply	4.75 V to 5.25 V		±0.04		dB
Output 1 dB Compression Point			16.8		dBm
Output Third-Order Intercept	Δf = 1 MHz, output power (P_{OUT}) = 0 dBm per tone		38		dBm
Noise Figure			3.5	3.8	dB

Parameter	Conditions	Min	Typ	Max	Unit
FREQUENCY = 3500 MHz					
Gain		15.9	17.5	18.8	dB
vs. Frequency	±50 MHz		±0.04		dB
vs. Temperature	$-40°C \leq T_A \leq +85°C$		±0.31		dB
vs. Supply	4.75 V to 5.25 V		±0.04		dB
Output 1 dB Compression Point			13.7		dBm
Output Third-Order Intercept	Δf = 1 MHz, output power (P_{OUT}) = 0 dBm per tone		33		dBm
Noise Figure			3.7	4.3	dB
FREQUENCY = 5800 MHz					
Gain		11.2	12.7	14.4	dB
vs. Frequency	±50 MHz		±0.03		dB
vs. Temperature	$-40°C \leq T_A \leq +85°C$		±1.2		dB
vs. Supply	4.75 V to 5.25 V		±0.04		dB
Output 1 dB Compression Point			6.8		dBm
Output Third-Order Intercept	Δf = 1 MHz, output power (P_{OUT}) = 0 dBm per tone		24.2		dBm
Noise Figure			5.7	6.3	dB
POWER INTERFACE	Pin VPOS				
Supply Voltage (VPOS)		4.5	5	5.5	V
Supply Current			93	115	mA
vs. Temperature	$-40°C \leq T_A \leq +85°C$		±15		mA
Power Dissipation	VPOS = 5 V		0.5		W

TYPICAL SCATTERING PARAMETERS

VPOS = 5 V and T_A = 25°C, the effects of the test fixture have been de-embedded up to the pins of the device.

Table 2.

Freq. (MHz)	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)
50	−23.9427	−127.394	20.77572	+170.5022	−23.0076	+3.044077	−23.9476	−132.996
100	−29.6174	−153.6	20.51771	+170.3216	−22.6572	+1.38839	−32.4194	−124.454
500	−34.5211	+19.99577	20.23355	+152.6774	−22.5262	−10.9886	−26.2358	−129.115
900	−37.74	+147.4543	20.07428	+132.0556	−22.4939	−21.2573	−20.2616	−159.271
1000	−33.8877	+131.3191	20.07369	+127.0206	−22.4386	−23.7005	−20.323	−160.866
1500	−24.7749	−152.311	19.80607	+101.2591	−22.3087	−35.6482	−16.2712	+168.1644
2000	−17.038	+178.4399	19.5708	+76.03876	−21.9922	−48.9813	−12.759	+164.7149
2500	−9.60208	+153.1961	19.26227	+49.85321	−21.6433	−60.9072	−9.74244	+150.6577
3000	−8.00289	+128.6464	18.82098	+24.3132	−21.0921	−76.3162	−8.77595	+128.7323
3500	−7.91011	+103.6543	18.18117	−1.63173	−21.2002	−91.6973	−10.5739	+90.37487
4000	−12.816	+96.79933	17.38515	−26.2863	−20.7711	−103.208	−13.1628	+8.899607
4500	−17.625	+156.5961	17.57137	−52.0317	−20.0291	−120.789	−7.31571	−73.4032
5000	−12.8458	+173.0378	16.39804	−77.6904	−19.9498	−136.697	−6.22666	−106.102
5500	−10.9468	−154.419	15.13047	−102.402	−19.8825	−153.753	−9.89228	−111.644
6000	−5.69808	−150.164	13.48849	−125.082	−20.3196	−170.25	−10.7825	−57.0274

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage, VPOS	6.5 V
Input Power (re: 50 Ω)	10 dBm
Internal Power Dissipation (Paddle Soldered)	650 mW
θ_{JC} (Junction to Paddle)	28.5°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

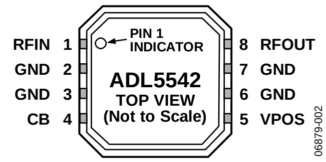

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RFIN	RF Input. Requires a dc blocking capacitor.
2, 3, 6, 7	GND	Ground. Connect these pins to a low impedance ground plane.
4	CB	Low Frequency Bypass. A 1 μF capacitor should be connected between this pin and ground.
5	VPOS	Power Supply for Bias Controller. Connect directly to external power supply.
8	RFOUT	RF Output and Supply Voltage. DC bias is provided to this pin through an inductor that is tied to the external power supply. RF path requires a dc blocking capacitor.
Exposed Paddle		Exposed Paddle. Internally connected to GND. Solder to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

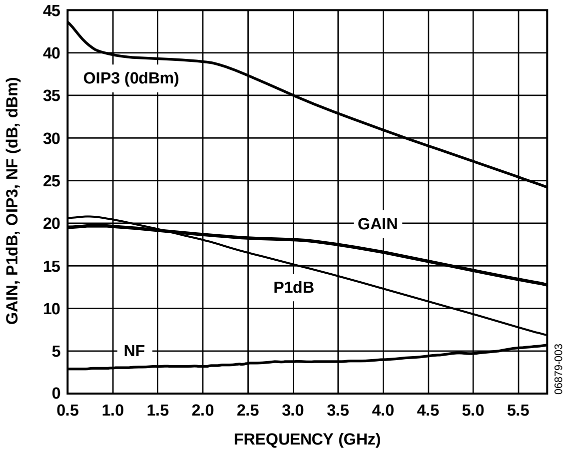

Figure 3. Gain, P1dB, OIP3, and Noise Figure vs. Frequency

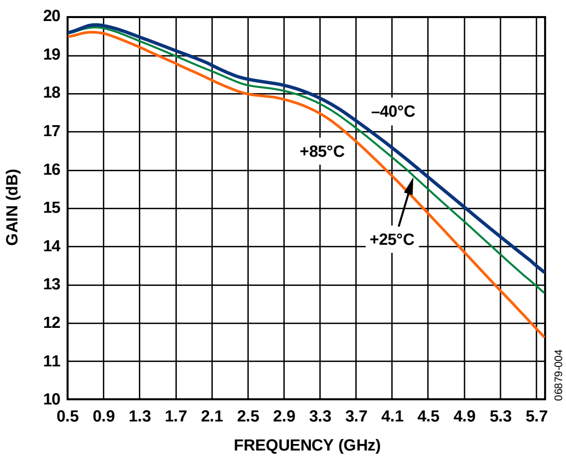

Figure 4. Gain vs. Frequency and Temperature

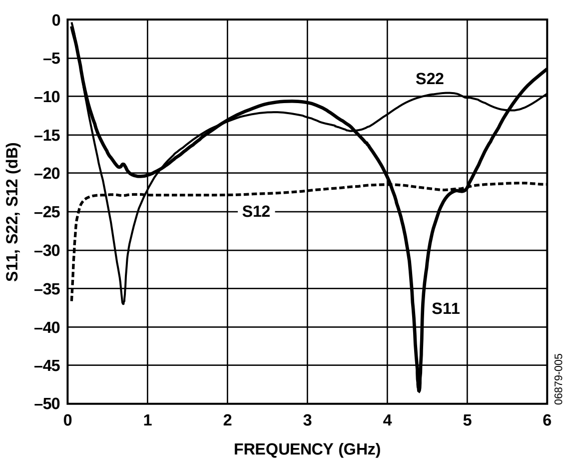

Figure 5. Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency

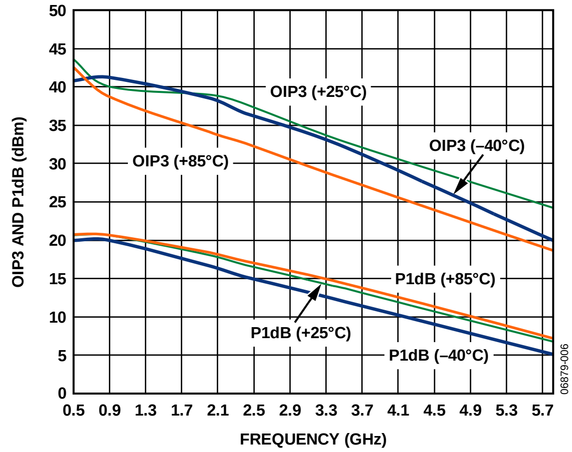

Figure 6. OIP3 and P1dB vs. Frequency and Temperature

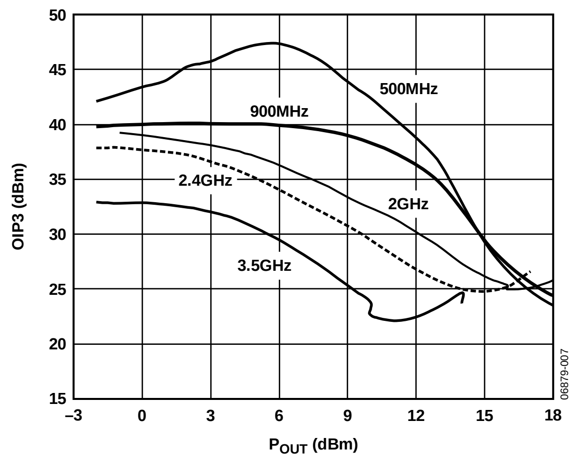

Figure 7. OIP3 vs. Output Power (P_{OUT}) and Frequency

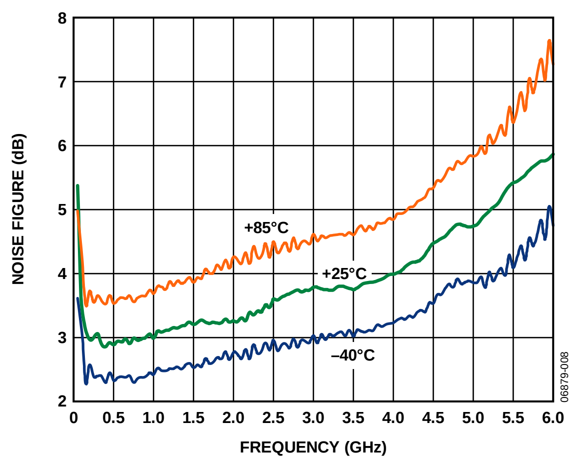

Figure 8. Noise Figure vs. Frequency and Temperature

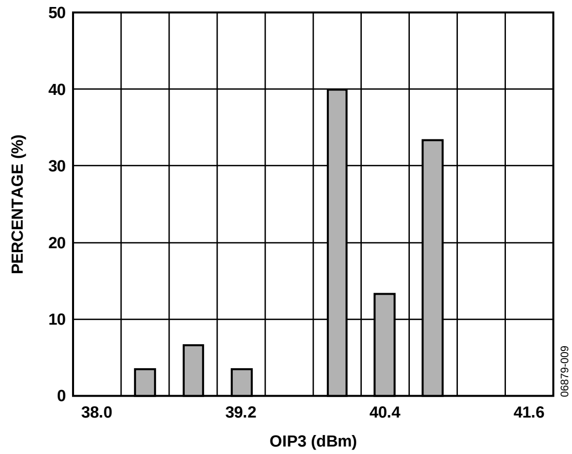

Figure 9. OIP3 Distribution at 900 MHz

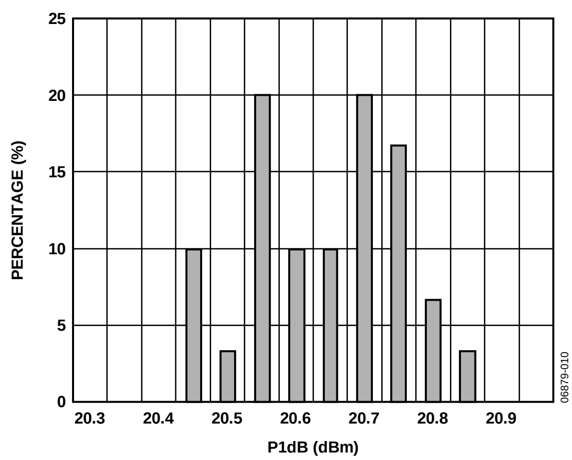

Figure 10. P1dB Distribution at 900 MHz

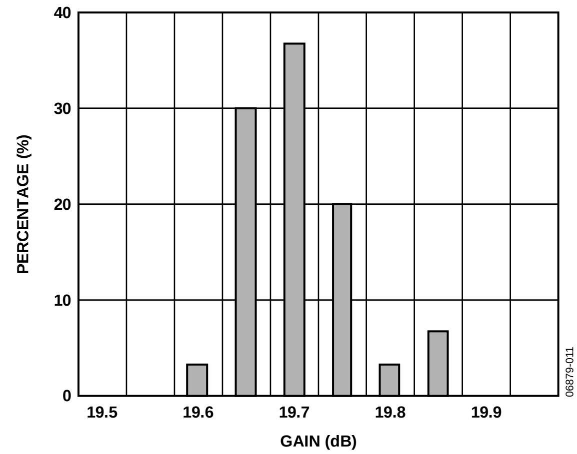

Figure 11. Gain Distribution at 900 MHz

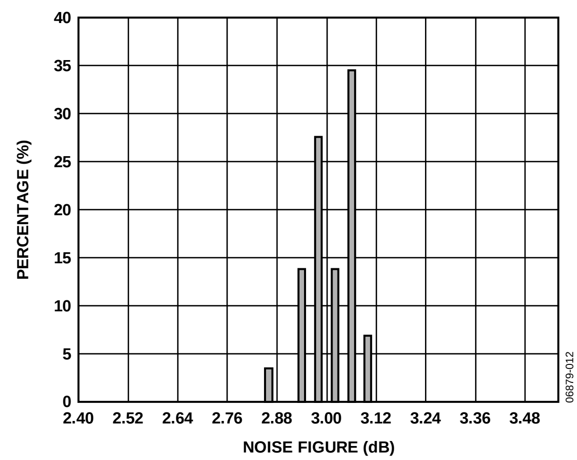

Figure 12. Noise Figure Distribution at 900 MHz

BASIC CONNECTIONS

The basic connections for operating the ADL5542 are shown in Figure 13. Recommended components are listed in Table 5. The input and output should be ac-coupled with appropriately sized capacitors (device characterization was performed with 33 pF capacitors). A 5 V dc bias is supplied to the amplifier via VPOS (Pin 5) and through a biasing inductor connected to RFOUT (Pin 8). The bias voltage should be decoupled using a 1 µF capacitor, a 1.2 nF capacitor, and two 68 pF capacitors.

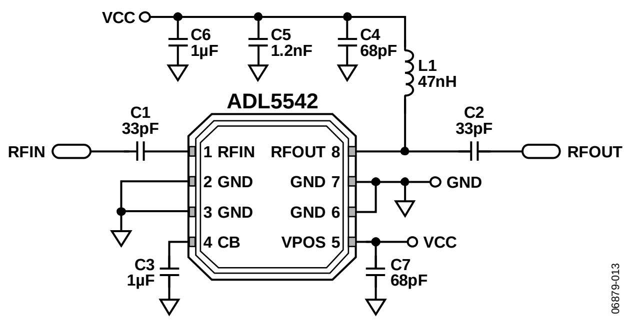

Figure 13. Basic Connections

For operation between 50 MHz and 500 MHz, a larger biasing choke and ac coupling capacitors are necessary (see Table 5). Figure 14 shows a plot of the input return loss, the output return loss, and the gain with these components. At 100 MHz, the ADL5542 achieves an OIP3 of 38 dBm (P_{OUT} = 0 dBm per tone). The noise figure performance for operation from 50 MHz to 500 MHz is shown in Figure 15. When operating below 50 MHz, the ADL5542 exhibits gain peaking, and the input and output match degrade significantly.

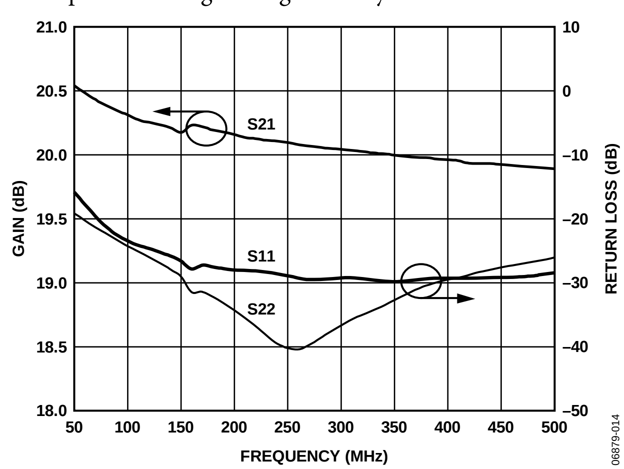

Figure 14. Input Return Loss (S11), Output Return Loss (S22), and Gain (S21) vs. Frequency

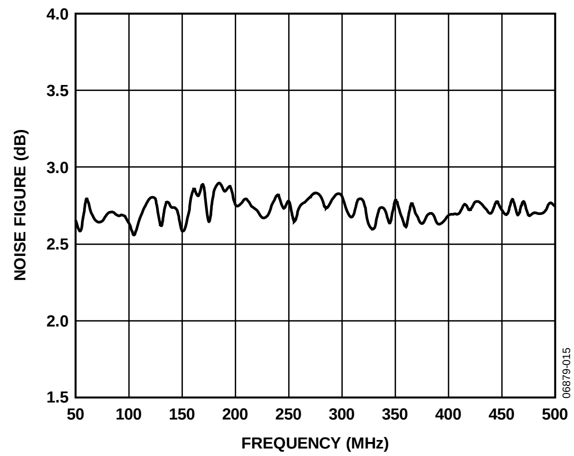

Figure 15. Noise Figure vs. Frequency

SOLDERING INFORMATION AND RECOMMENDED PCB LAND PATTERN

Figure 16 shows the recommended land pattern for the ADL5542. To minimize thermal impedance, the exposed paddle on the package underside should be soldered down to a ground plane along with Pin 2, Pin 3, Pin 6, and Pin 7. If multiple ground layers exist, they should be stitched together using vias (a minimum of five vias is recommended). For more information on land pattern design and layout, refer to Application Note AN-772, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP).*

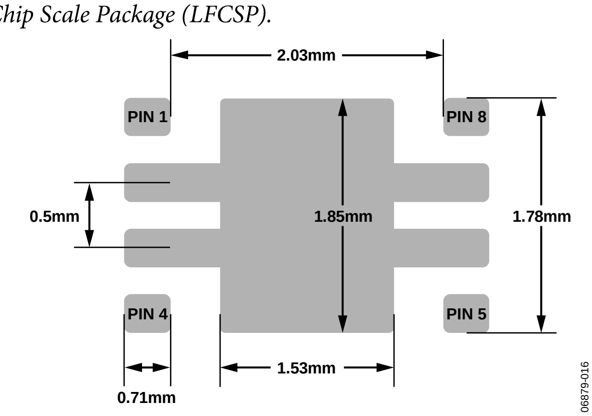

Figure 16. Recommended Land Pattern

Table 5. Recommended Components for Basic Connections

Frequency	C1	C2	C3	L1	C4	C5	C6	C7
50 MHz to 500 MHz	0.1 µF	0.1 µF	1 µF	470 nH (Coilcraft 0603LS-471NXJL_ or equivalent)	68 pF	1.2 nF	1 µF	68 pF
500 MHz to 6000 MHz	33 pF	33 pF	1 µF	47 nH (Coilcraft 0603CS-47NXJL_ or equivalent)	68 pF	1.2 nF	1 µF	68 pF

EVALUATION BOARD

Figure 19 shows the schematic for the ADL5542 evaluation board. The board is powered by a single 5 V supply.

The components used on the board are listed in Table 6. Power can be applied to the board through clip-on leads (VCC and GND) or through a 2-pin header (W1).

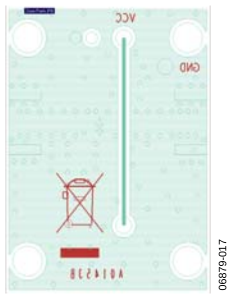

Figure 17. Evaluation Board Layout (Bottom)

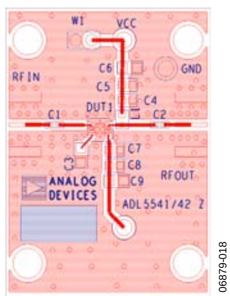

Figure 18. Evaluation Board Layout (Top)

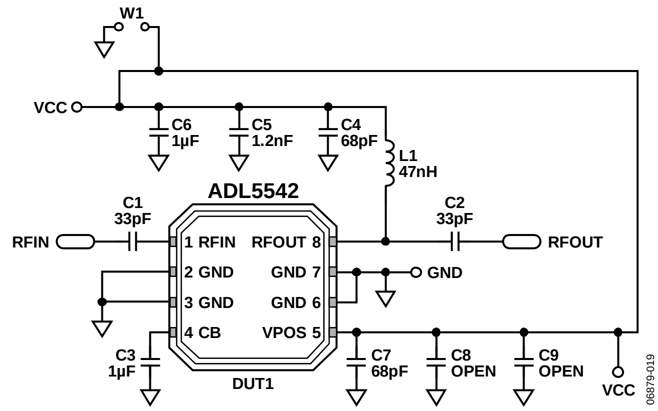

Figure 19. Evaluation Board Schematic

Table 6. Evaluation Board Configuration Options

Component	Function	Default Value
DUT1	Gain block	ADL5542
C1, C2	AC coupling capacitors	33 pF, 0402
C3	Low frequency bypass capacitor	1 µF, 0805
C4, C5, C6, C7, C8, C9	Power supply decoupling capacitors	C4, C7 = 68 pF, 0603
		C5 = 1.2 nF, 0603
		C6 = 1 µF, 0805
		C8, C9 = open
L1	DC bias inductor	47 nH, 0603 (Coilcraft 0603CS-47NXJL_ or equivalent)
VCC and GND	Clip-on terminals for power supply	
W1	2-pin header for connection of ground and supply via cable	

OUTLINE DIMENSIONS

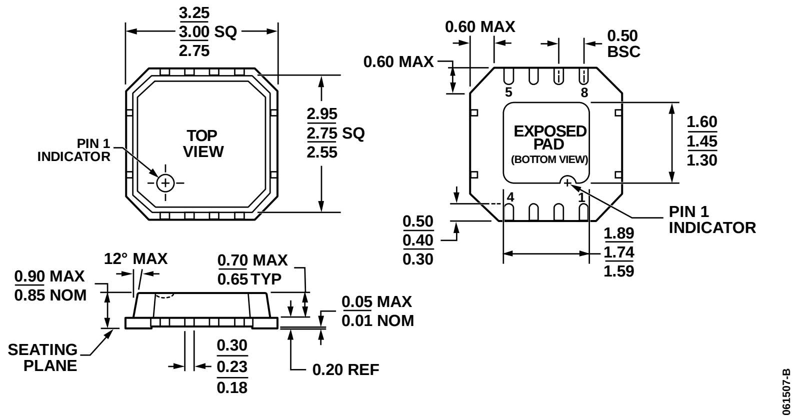

Figure 20. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
3 mm × 3 mm Body, Very Thin, Dual Lead
(CP-8-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADL5542ACPZ-R7[1]	–40°C to +85°C	8-Lead LFCSP_VD, Tape and Reel	CP-8-2	Q15
ADL5542-EVALZ[1]		Evaluation Board		

[1] Z = RoHS Compliant Part.