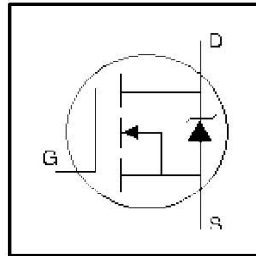


# IRFPC60LCPbF

## HEXFET® Power MOSFET

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30V  $V_{GS}$  Rating
- Reduced  $C_{iss}$ ,  $C_{oss}$ ,  $C_{rss}$
- Isolated Central Mounting Hole
- Dynamic  $dv/dt$  Rated
- Repetitive Avalanche Rated
- Lead-Free



$$V_{DSS} = 600V$$

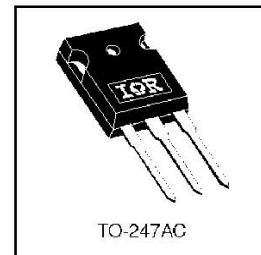
$$R_{DS(on)} = 0.40\Omega$$

$$I_D = 16A$$

### Description

This new series of Low Charge HEXFET Power MOSFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing advanced Hexfet technology the device improvements allow for reduced gate drive requirements, faster switching speeds and increased total system savings. These device improvements combined with the proven ruggedness and reliability of HEXFETs offer the designer a new standard in power transistors for switching applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.




### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	16	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	10	
$I_{DM}$	Pulsed Drain Current ①	64	
$P_D @ T_C = 25^\circ C$	Power Dissipation	280	W
	Linear Derating Factor	2.2	W/°C
$V_{GS}$	Gate-to-Source Voltage	±30	V
$E_{AS}$	Single Pulse Avalanche Energy ②	1000	mJ
$I_{AR}$	Avalanche Current ①	16	A
$E_{AR}$	Repetitive Avalanche Energy ①	28	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ ③	3.0	V/ns
$T_J$	Operating Junction and	-55 to +150	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf·in (1.1N·m)	

### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	—	

## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	600	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.63	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(ON)</sub>	Static Drain-to-Source On-Resistance	—	—	0.40	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 9.6A ①
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	11	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 9.6A
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> = 600V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 480V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
Q <sub>g</sub>	Total Gate Charge	—	—	120	nC	I <sub>D</sub> = 16A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	29		V <sub>DS</sub> = 360V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	48		V <sub>GS</sub> = 10V, See Fig. 6 and 13 ②
t <sub>d(on)</sub>	Turn-On Delay Time	—	17	—	ns	V <sub>DD</sub> = 300V
t <sub>r</sub>	Rise Time	—	57	—		I <sub>D</sub> = 16A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	43	—		R <sub>G</sub> = 4.3Ω
t <sub>f</sub>	Fall Time	—	38	—		R <sub>D</sub> = 18Ω, See Fig. 10 ③
L <sub>D</sub>	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	13	—		
C <sub>iss</sub>	Input Capacitance	—	3500	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	400	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	39	—		f = 1.0MHz, See Fig. 5

## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	16	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	64		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.8	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 16A, V <sub>GS</sub> = 0V ②
t <sub>rr</sub>	Reverse Recovery Time	—	650	980	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 16A
Q <sub>rr</sub>	Reverse Recovery Charge	—	6.0	9.0	μC	di/dt = 100A/μs ③
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

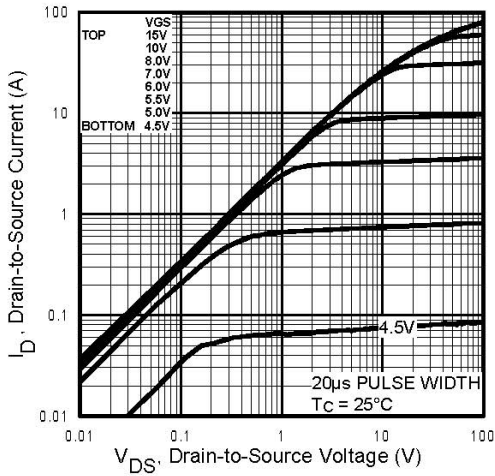
### Notes:

① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )

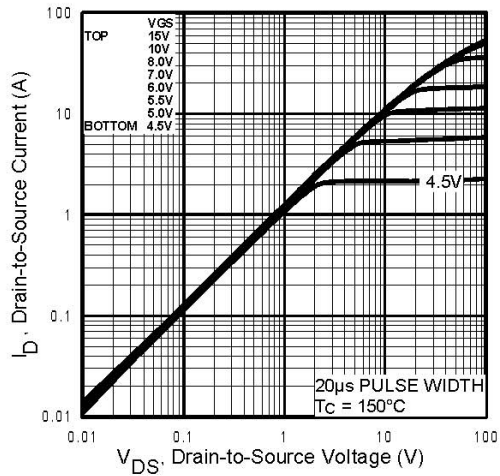
② I<sub>SD</sub> ≤ 16A, di/dt ≤ 140A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 150°C

③ V<sub>DD</sub> = 25V, starting T<sub>J</sub> = 25°C, L = 7.2mH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 16A. (See Figure 12)

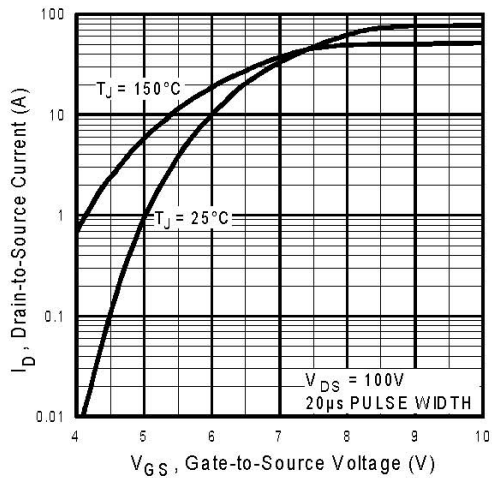
④ Pulse width ≤ 300μs; duty cycle ≤ 2%.



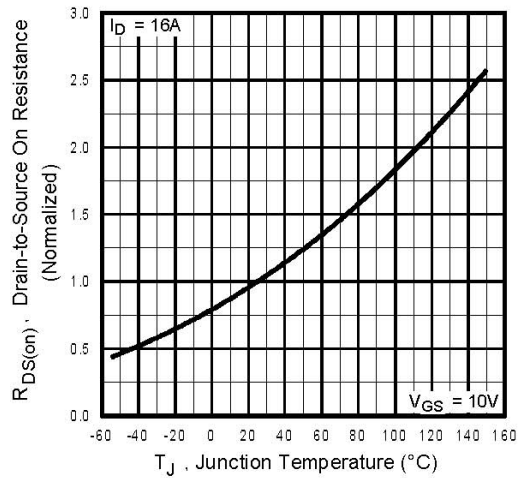
**Fig 1.** Typical Output Characteristics,  
 $T_C = 25^\circ\text{C}$



**Fig 2.** Typical Output Characteristics,  
 $T_C = 150^\circ\text{C}$

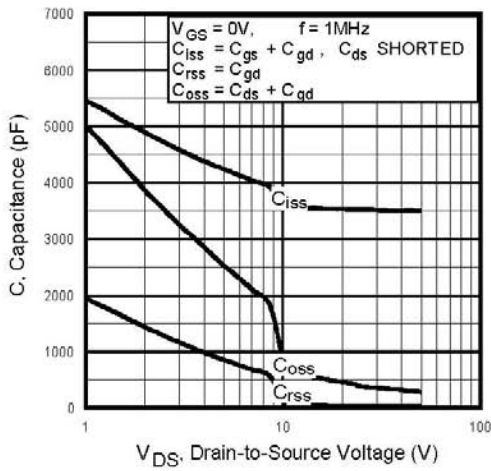


**Fig 3.** Typical Transfer Characteristics

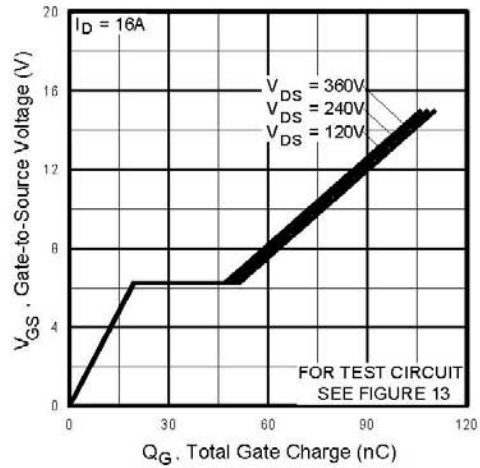


**Fig 4.** Normalized On-Resistance  
Vs. Temperature

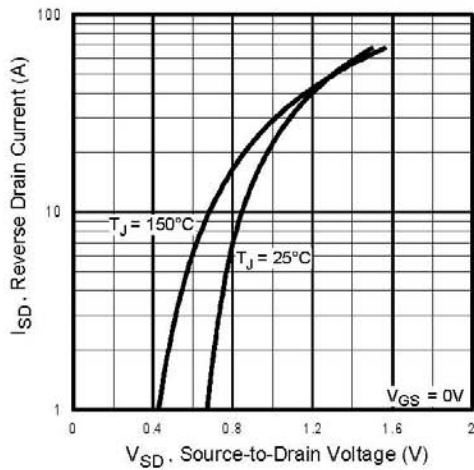
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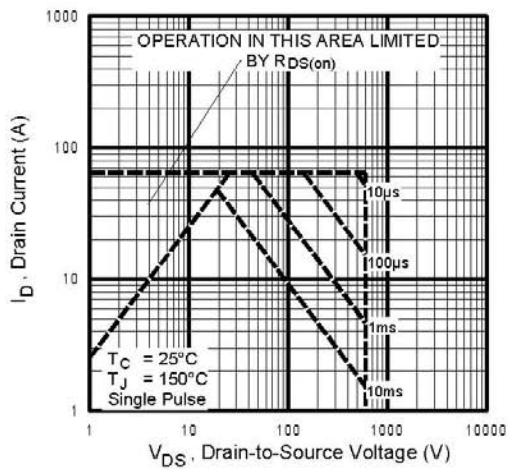
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



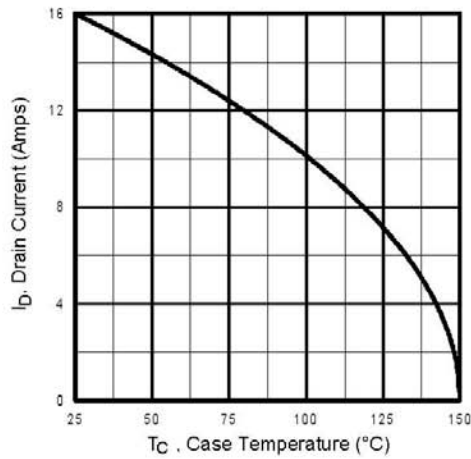
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



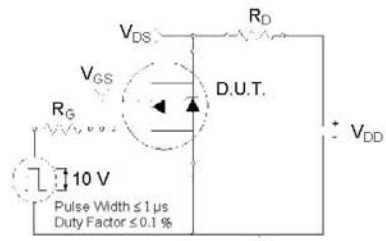
**Fig 7.** Typical Source-Drain Diode Forward Voltage



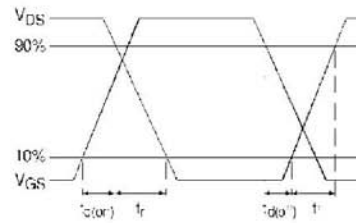
**Fig 8.** Maximum Safe Operating Area



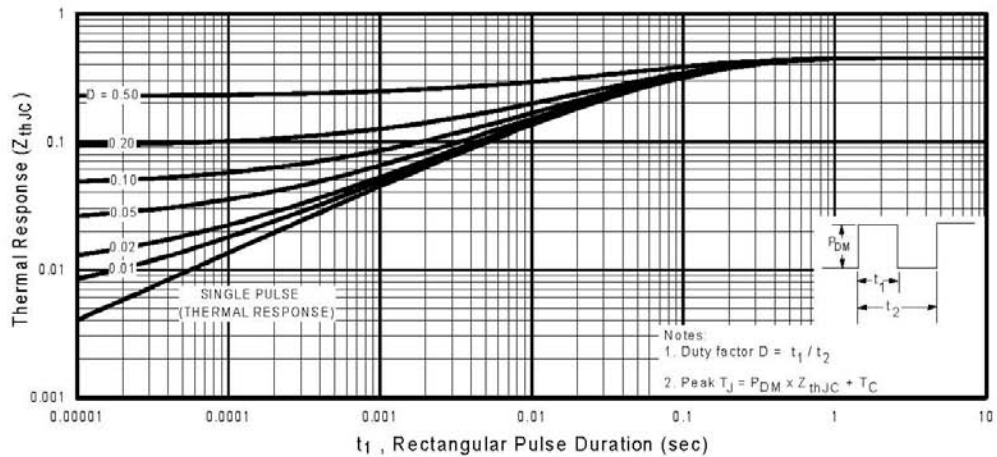
**Fig 9.** Maximum Drain Current Vs. Case Temperature



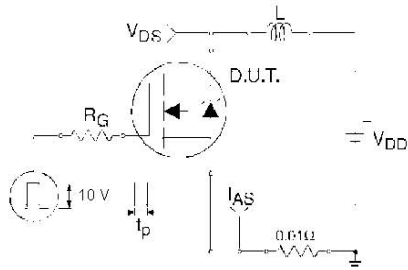
**Fig 10a.** Switching Time Test Circuit



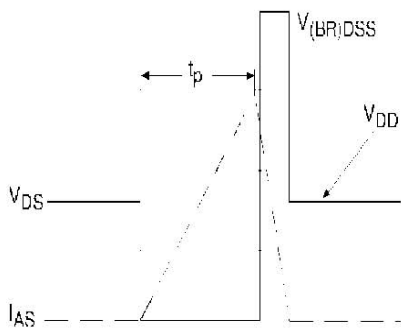
**Fig 10b.** Switching Time Waveforms



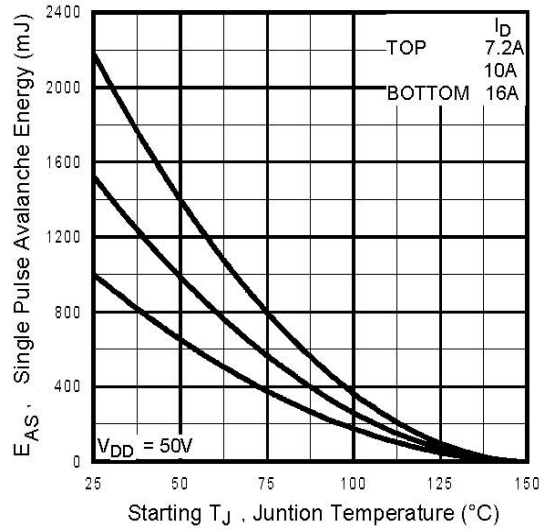
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



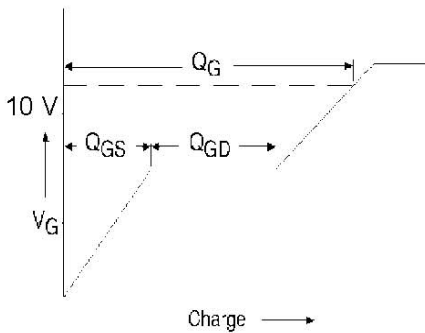
**Fig 12a.** Unclamped Inductive Test Circuit



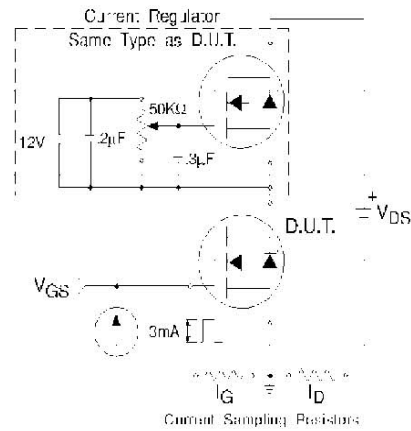
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

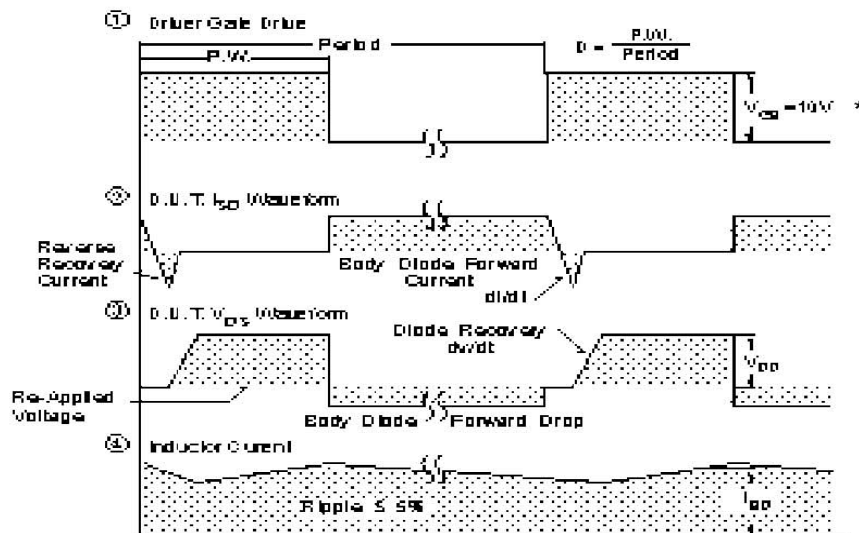
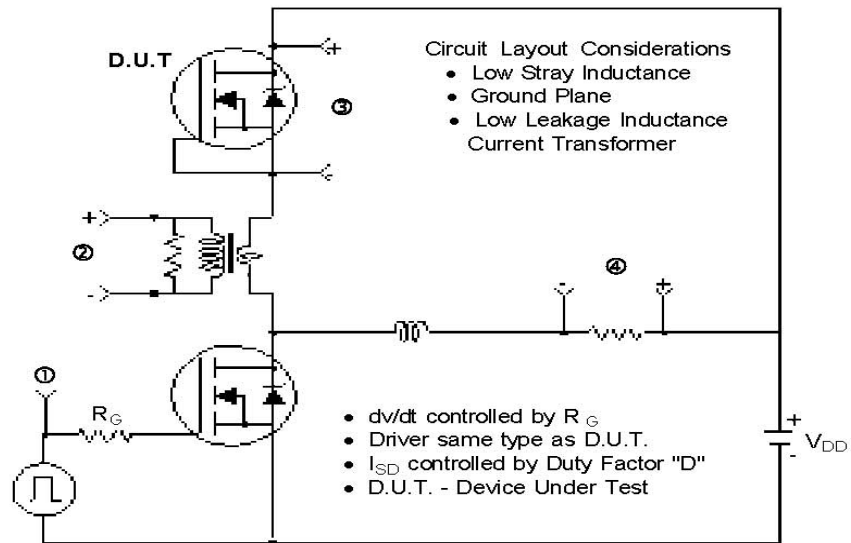


**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



\*  $V_{GS} = 5V$  for Logic Level Devices

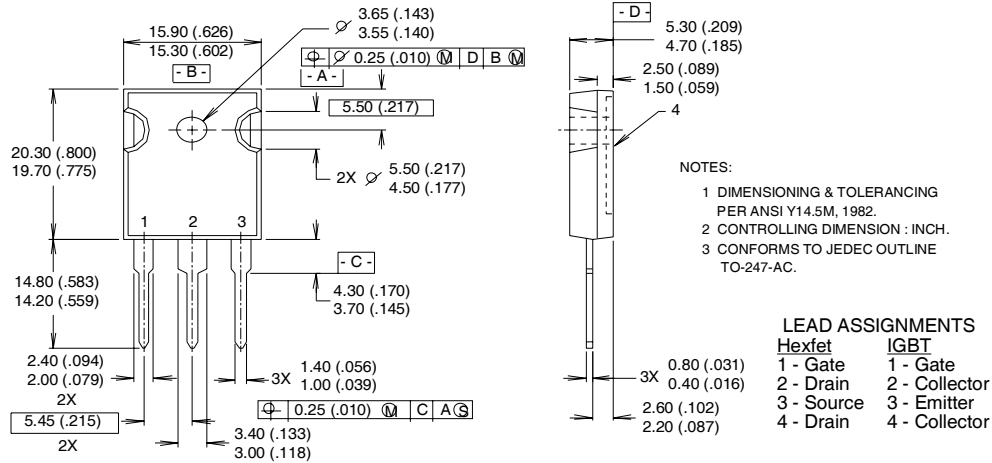
**Fig 14.** For N-Channel HEXFETS

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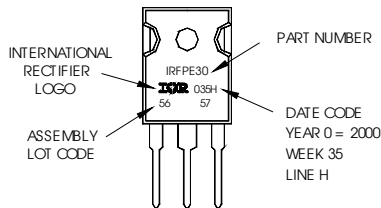
## TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



## TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30  
WITH ASSEMBLY  
LOT CODE 5657  
ASSEMBLED ON WW 35, 2000  
IN THE ASSEMBLY LINE "H"  
**Note:** "P" in assembly line  
position indicates "Lead-Free"



Data and specifications subject to change without notice.



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TAC Fax: (310) 252-7903

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Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>