

SMPS MOSFET IRFP450NPbF

HEXFET® Power MOSFET

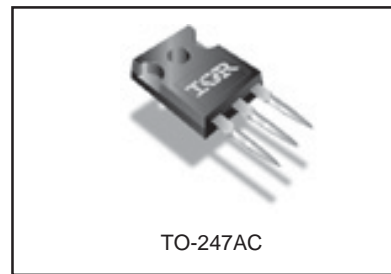
Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Lead-Free

V_{DSS}	R_{ds(on)} max	I_D
500V	0.37Ω	14A

Benefits

- Low Gate Charge Q_g results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective Coss Specified (See AN 1001)



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	14	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	8.8	
I _{DM}	Pulsed Drain Current ①	56	
P _D @ T _C = 25°C	Power Dissipation	200	W
	Linear Derating Factor	1.6	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ②	5.0	V/ns
T _J	Operating Junction and	-55 to + 150	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Typical SMPS Topologies

- Two transistor Forward
- Half Bridge and Full Bridge
- PFC Boost

Notes ① through ⑤ are on page 8

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.59	—		$V/^\circ\text{C}$ Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.37	Ω	$V_{GS} = 10V, I_D = 8.4A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 500V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 400V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	7.9	—	—	S	$V_{DS} = 50V, I_D = 8.4A$
Q_g	Total Gate Charge	—	—	77	nC	$I_D = 14A$
Q_{gs}	Gate-to-Source Charge	—	—	26		$V_{DS} = 400V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	34		$V_{GS} = 10V$, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	20	—	ns	$V_{DD} = 250V$
t_r	Rise Time	—	63	—		$I_D = 14A$
$t_{d(off)}$	Turn-Off Delay Time	—	29	—		$R_G = 6.2\Omega$
t_f	Fall Time	—	25	—		$V_{GS} = 10V$, See Fig. 10 ④
C_{iss}	Input Capacitance	—	2260	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	210	—		$V_{DS} = 25V$
C_{riss}	Reverse Transfer Capacitance	—	14	—		$f = 1.0\text{MHz}$, See Fig. 5
C_{oss}	Output Capacitance	—	2410	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	59	—		$V_{GS} = 0V, V_{DS} = 400V, f = 1.0\text{MHz}$
$C_{oss\ eff.}$	Effective Output Capacitance	—	110	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V$ ⑤

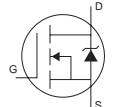
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	170	mJ
I_{AR}	Avalanche Current①	—	14	A
E_{AR}	Repetitive Avalanche Energy①	—	20	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.64	$^\circ\text{C/W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	14	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	56		
V_{SD}	Diode Forward Voltage	—	—	1.4	V	$T_J = 25^\circ\text{C}, I_S = 14A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	430	650	ns	$T_J = 25^\circ\text{C}, I_F = 14A$
Q_{rr}	Reverse Recovery Charge	—	3.7	5.6	μC	$di/dt = 100A/\mu\text{s}$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

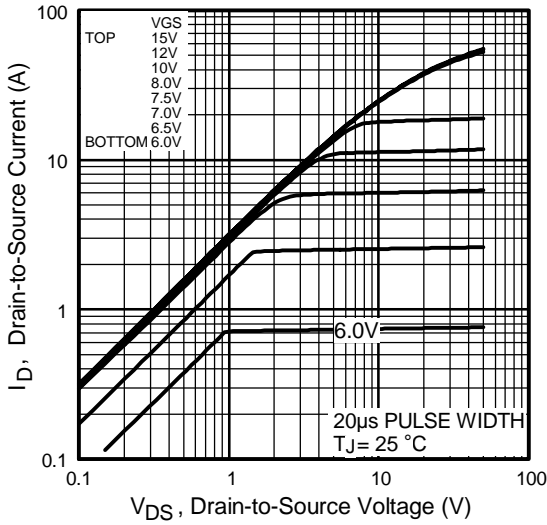


Fig 1. Typical Output Characteristics

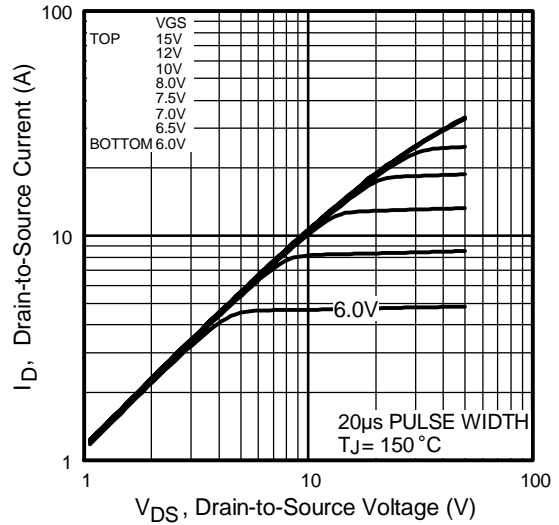


Fig 2. Typical Output Characteristics

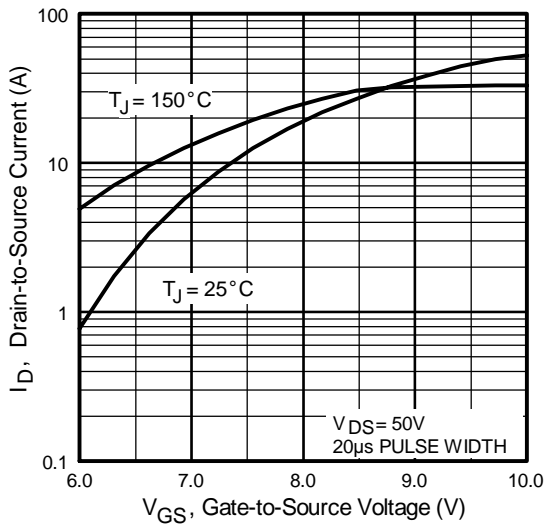


Fig 3. Typical Transfer Characteristics

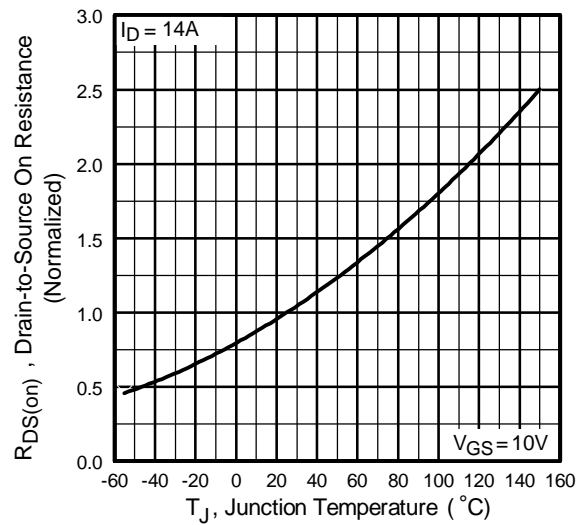


Fig 4. Normalized On-Resistance Vs. Temperature

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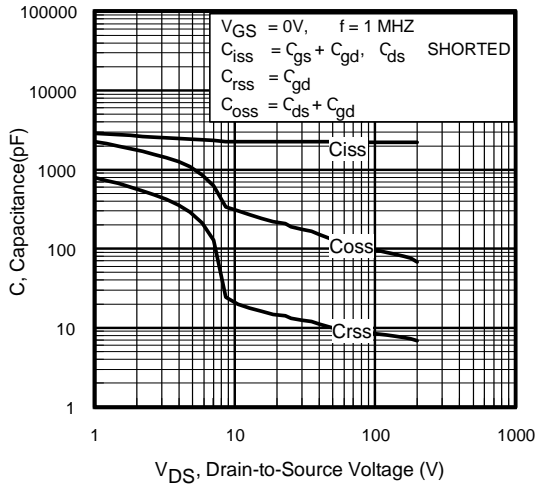


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

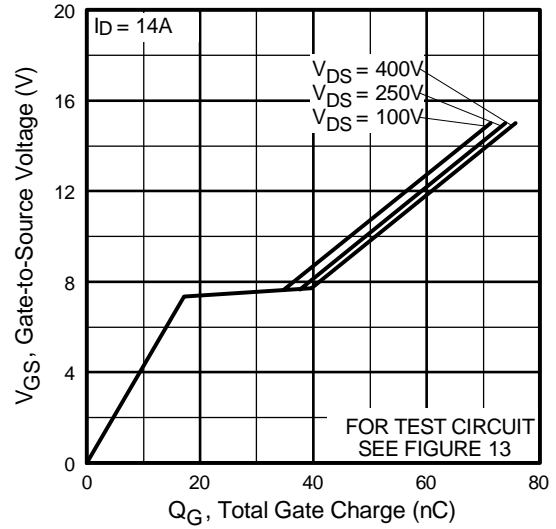


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

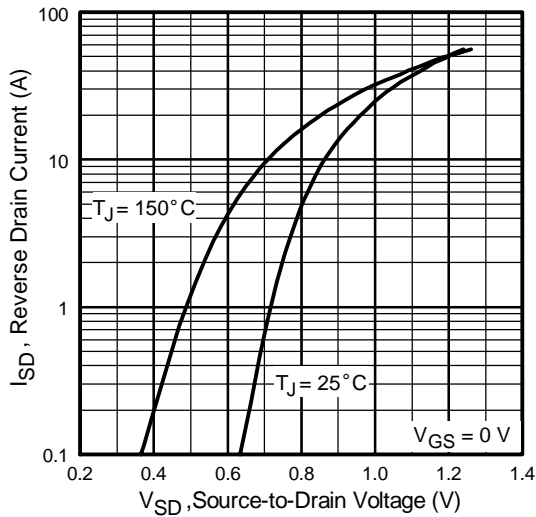


Fig 7. Typical Source-Drain Diode Forward Voltage

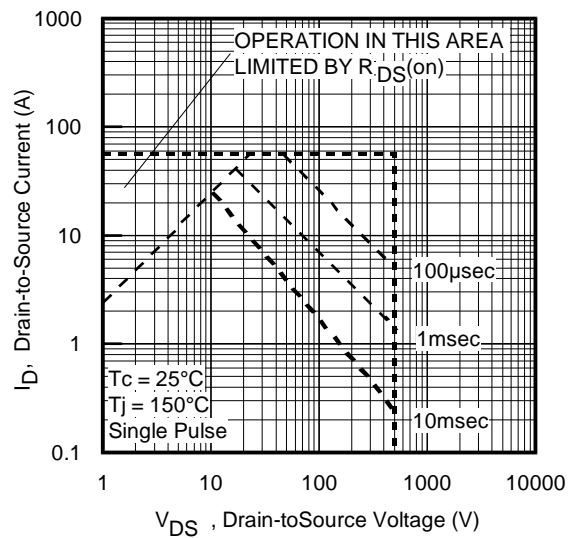


Fig 8. Maximum Safe Operating Area

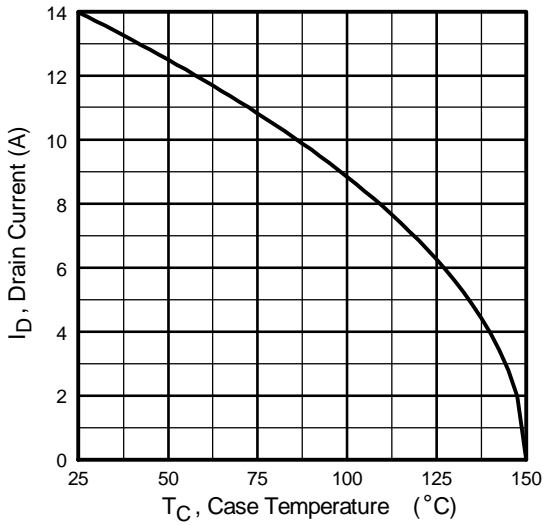


Fig 9. Maximum Drain Current Vs. Case Temperature

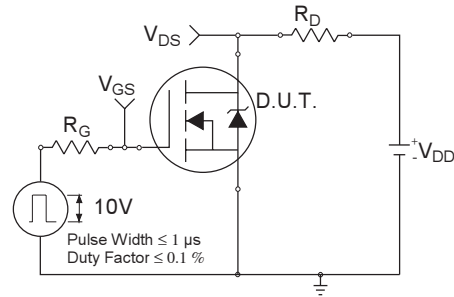


Fig 10a. Switching Time Test Circuit

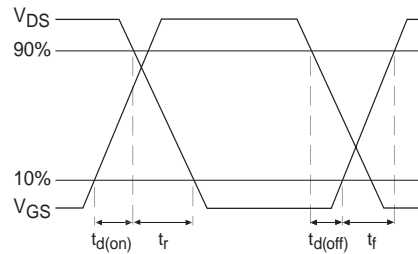


Fig 10b. Switching Time Waveforms

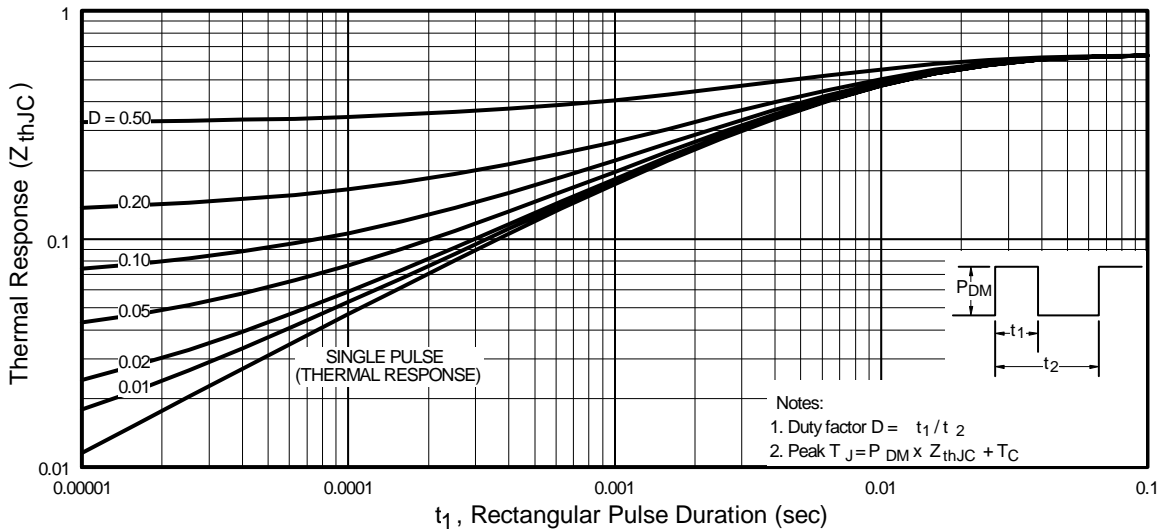


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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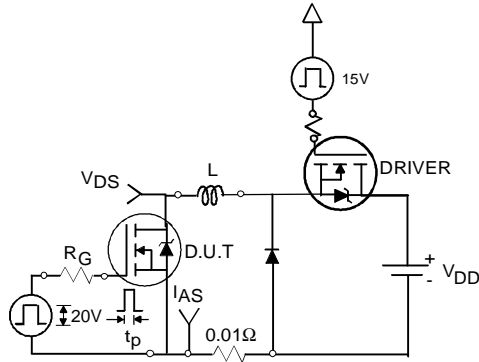


Fig 12a. Unclamped Inductive Test Circuit

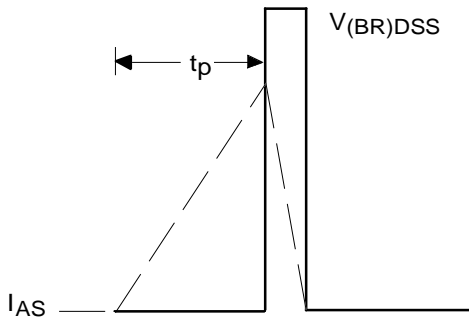


Fig 12b. Unclamped Inductive Waveforms

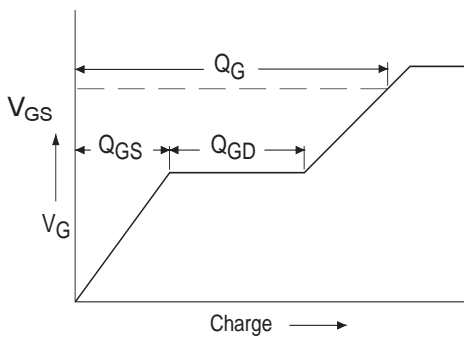


Fig 13a. Basic Gate Charge Waveform

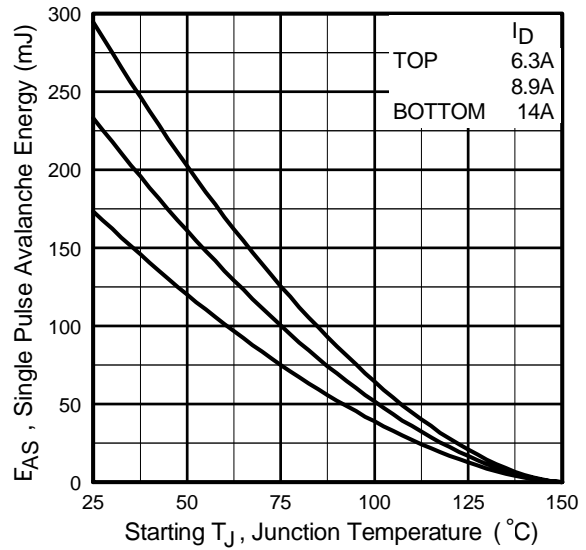


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

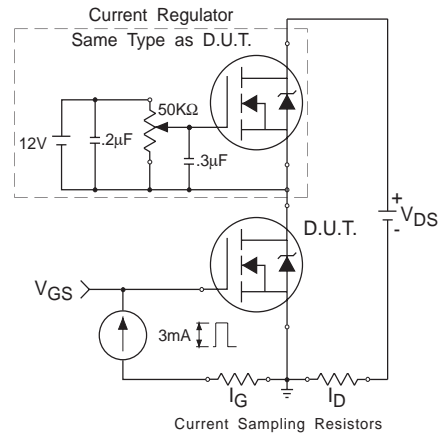
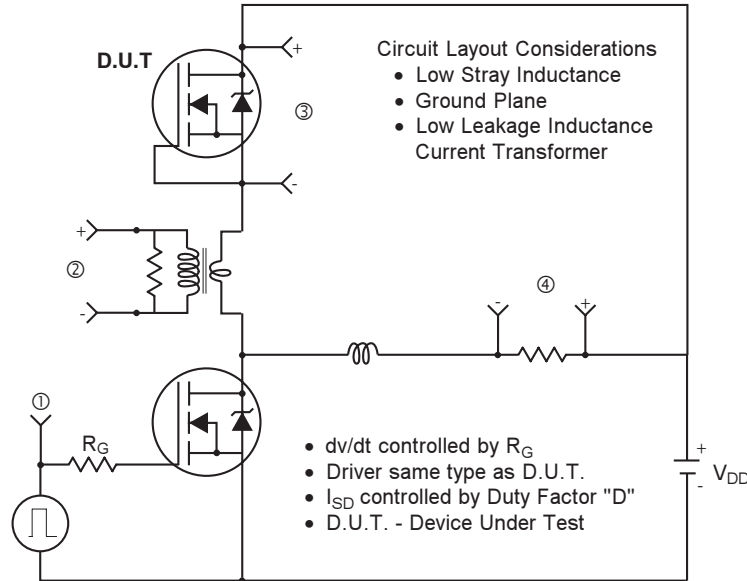


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



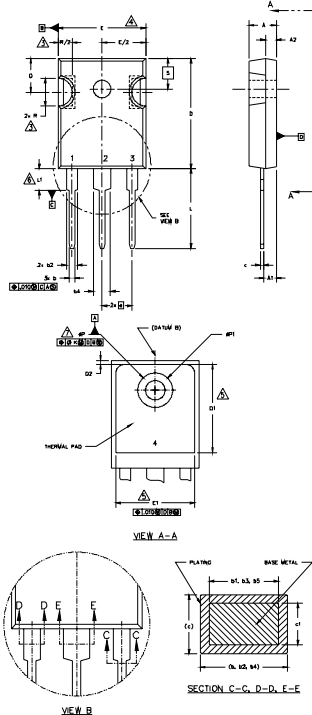
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

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TO-247AC Package Outline Dimensions are shown in millimeters (inches)



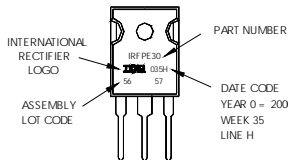
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
- CONTOUR OF SLOT OPTIONAL.
- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
- LEAD FINISH UNCONTROLLED IN L1.
- ϕP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154" [3.91]
- OUTLINE CONFORMS TO JEDEC OUTLINE TO-247 WITH THE EXCEPTION OF DIMENSION c.

SYMBOL	DIMENSIONS				NOTES	
	INCHES		MILLIMETERS			
A	.185	.209	4.65	5.31		
A1	.087	.102	2.21	2.59		
A2	.059	.098	1.50	2.49		
b	.039	.055	0.99	1.40		LEAD ASSIGNMENTS
b1	.039	.053	0.99	1.35		HEXFET
b2	.065	.094	1.65	2.39		1.- GATE
b3	.065	.092	1.65	2.37		2.- DRAIN
b4	.102	.135	2.59	3.43		3.- SOURCE
b5	.102	.133	2.59	3.38		4.- DRAIN
c	.015	.034	0.38	0.86		
c1	.015	.030	0.38	0.76		
D	.776	.815	19.71	20.70	4	IGBTs, CoPACK
D1	.515	-	13.08	-	5	1.- GATE
D2	.020	.030	0.51	0.76		2.- COLLECTOR
E	.602	.625	15.29	15.87	4	3.- EMITTER
E1	.540	-	13.72	-		4.- COLLECTOR
e	.215 BSC		5.46 BSC			
ϕk	.010		2.54			
L	.559	.634	14.20	16.10		DIODES
L1	.146	.169	3.71	4.29		1.- ANODE/OPEN
N	.140		3.56 BSC			2.- CATHODE
ϕP	.140	.144	3.56	3.66		3.- ANODE
$\phi P1$	-	.275	-	6.98		
Q	.209	.224	5.31	5.69		
R	.178	.216	4.52	5.49		
S	.217 BSC		5.51 BSC			

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFP30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"
Note: "P" in assembly line
position indicates "Lead-Free"



Notes:

- Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- Starting $T_J = 25^\circ\text{C}$, $L = 1.7\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 14\text{A}$. (See Figure 12)
- $I_{SD} \leq 14\text{A}$, $di/dt \leq 510\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$
- Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}

Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site,

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