



# C8051F236

## 8K Flash, 1.25K RAM, 48-Pin MCU

PRELIMINARY

### ANALOG PERIPHERALS

#### Two Comparators

- Programmable Hysteresis
- Configurable to Generate Interrupts or Reset

#### VDD Monitor and Brown-out Detector

#### ON-CHIP JTAG DEBUG

- On-Chip Debug Circuitry Facilitates Full Speed, Non-Intrusive In-System Debug (No Emulator Required!)
- Provides Breakpoints, Single Stepping, Watchpoints, Stack Monitor
- Inspect/Modify Memory and Registers
- Superior Performance to Emulation Systems Using ICE-Chips, Target Pods, and Sockets
- Low Cost, Complete Development Kit

#### SUPPLY VOLTAGE .....2.7V to 3.6V

- Typical Operating Current: 9mA @ 25MHz
- Typical Stop Mode Current: <0.1uA

#### Temperature Range: -40°C to +85°C

#### 48-Pin TQFP Package

### 8051-COMPATIBLE µC Core

- Pipelined Instruction Architecture; Executes 70% of Instructions in 1 or 2 System Clocks
- Up to **25MIPS** Throughput with 25MHz Clock
- Expanded Interrupt Handler

#### MEMORY

- 1280 Bytes Internal Data RAM (256 + 1k)
- 8k Bytes FLASH; In-System Programmable in 512 byte Sectors

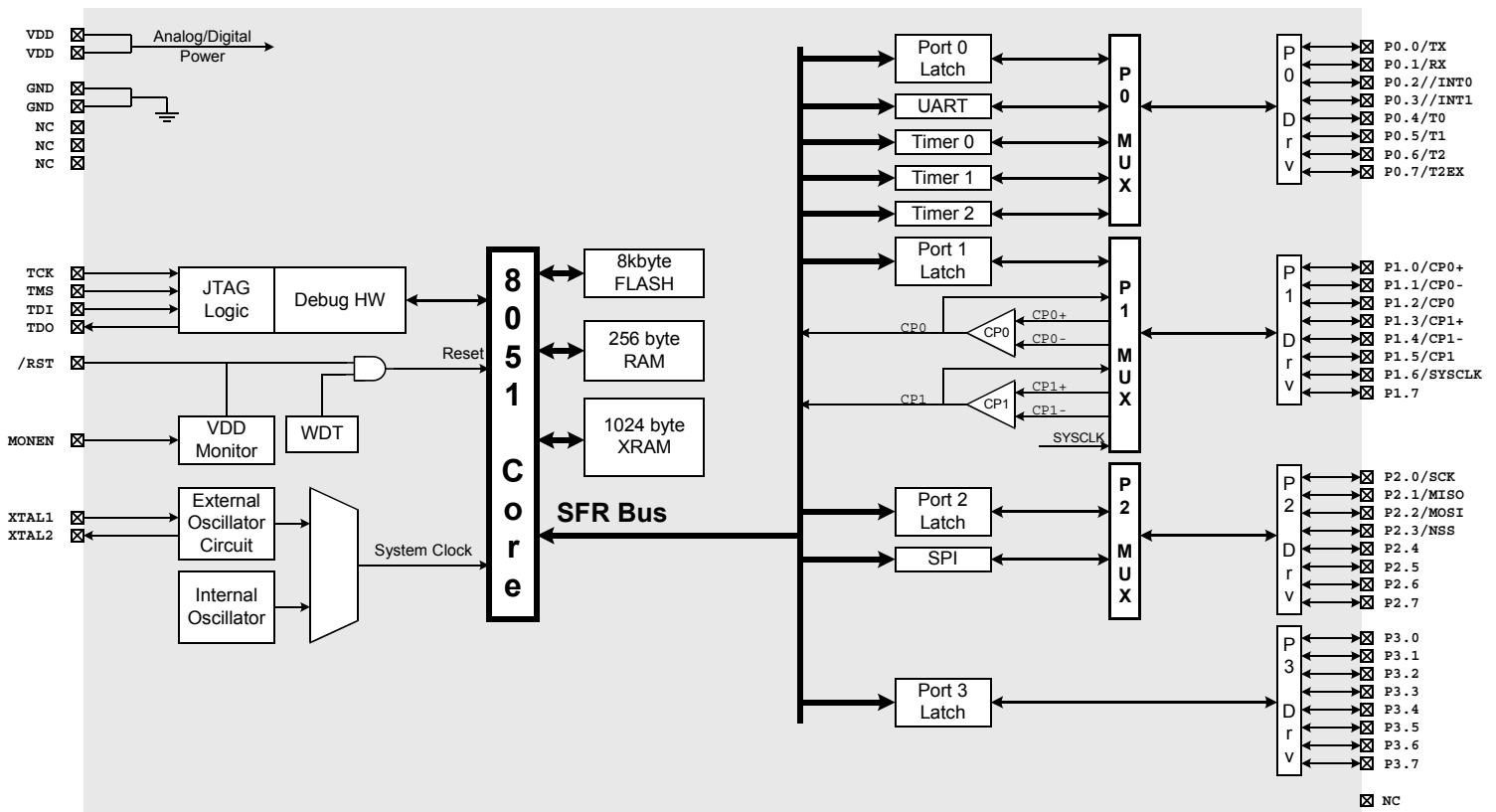
#### DIGITAL PERIPHERALS

- 32 Port I/O; All are 5V tolerant
- Hardware SPI™ and UART Serial Ports Available Concurrently
- Three 16-bit Counter/Timers
- Dedicated Watch-Dog Timer
- Bi-directional Reset

#### CLOCK SOURCES

- Internal Programmable Oscillator: 2-to-16MHz
- External Oscillator: Crystal, RC, C, or Clock
- Can Switch Between Clock Sources on-the-fly; Useful in Power Saving Modes

SPI is a trademark of Motorola, Inc.





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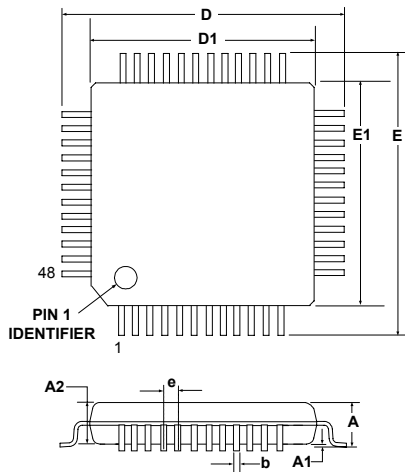
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PRELIMINARY

SELECTED ELECTRICAL SPECIFICATIONS  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = 2.7\text{V}$  unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>GLOBAL CHARACTERISTICS</b>					
Supply Voltage		2.7		3.6	V
Supply Current (CPU active)	Clock=25MHz		9		mA
	Clock=1MHz		0.4		mA
	Clock=32kHz; VDD Monitor Disabled		11		$\mu\text{A}$
Supply Current (shutdown)	Oscillator not running; VDD Monitor Enabled		10		$\mu\text{A}$
	Oscillator not running; VDD Monitor Disabled		0.1		$\mu\text{A}$
Clock Frequency Range		DC		25	MHz
<b>COMPARATORS</b>					
Supply Current	(each comparator)		1.5		$\mu\text{A}$
Response Time	$(\text{CP}+) - (\text{CP}-) = 100\text{mV}$		4.0		$\mu\text{s}$

## PACKAGE INFORMATION



	MIN (mm)	NOM (mm)	MAX (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
D	-	9.00	-
D1	-	7.00	-
e	-	0.50	-
E	-	9.00	-
E1	-	7.00	-

## C8051F226DK DEVELOPMENT KIT

