REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
INIT	INITIAL RELEASE	98-03-18	
A	CONVERSION OF WSD (SHORT FORM) TO WSD (FULL FORM)	98-12-21	

CAUTION

THIS ITEM IS SENSITIVE TO ELECTROSTATIC DISCHARGE (ESD).

WHITE SANDS DRAWING

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
2 PLACES ±
3 PLACES ±

PREPARED BY Lawrence S.N. Wang — **DATE (YR-MO-DA)** 98-12-21

CHECKED BY Roger Sloan 99/01/08

ENGINEER M. Klein Martha A Klein 99/01/19

DRAWING APPROVAL John H. O'kuma John H O'Kuma

DESIGN APPROVAL Jim Nicklaus 99/01/19

Semiconductor Discrete Device, P-Channel Power MOS Field Effect Transistor

SIZE	CAGE CODE	
A	09WF0	W98M9640

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing describes a commercially available microcircuit with radiation tolerance.

1.1.1 **RTA** this drawing contains a radiation tolerance assured item and/or processes. All changes to items or processes and all proposed substitutions of items identified as RTA on the drawing, must be evaluated and approved by the Radiation Tolerance Assured Supply And Support Center (RTASSC), Directorate For Applied Technology, Test And Simulation (DATTS), White Sands Missile Range, (WSMR).

1.1.2 Only the item described on this drawing when procured from the vendor(s) listed hereon is approved for use in the application(s) specified hereon. A substitute item shall not be used without prior approval by the RTASSC.

1.2 Part or Identification Number (PIN). The complete part number shall be as shown in the following example.

W98 M9640	01	E	U	X
Drawing number	Device Type	Device Class	Case Outline	Lead Finish

1.3 Drawing Number. The drawing number consists of three pieces of information as follows:

W98 = Indicates White Sands drawing, year 1998.
M = Radiation Tolerance Designator (3000 rads(Si)).
9640 = Semiconductor discrete device, P-channel power MOS field effect transistor

1.4 Device Type. The device type shall identify the circuit function as follows:

Device Type	Generic #	Circuit Function	Switchin on/off time(typ.); Frequency(Test Condition)
01	9640	P-channel power MOSFET	57 ns / 77 ns; 1.0 MHz

1.5 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
E	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A

1.6 Case Outline. The case outline is as designated in MIL-STD-1835 as follows:

Outline letter	Terminals	Package Style
U	4	TO-263AB, see Figure 1, Surface Mount

1.7 Lead Finish. The lead finish is as specified in the purchase order (X indicates acceptable lead finishes per manufacturers specification).

1.8 Operating Temperature. The operating temperature range of this device is -55°C to +150°C.

2.0 Salient characteristics.

2.1 Maximum operating conditions. The maximum operating conditions shall be as specified in Table I.

2..2 Electrical performance characteristics:
2.2.1 The electrical performance characteristics shall be as specified in Table II.
2.2.2 The Typical characteristics diagrams shall be as specified in diagrams in Figure 2.
2.2.3 Radiation Tolerance Assurance(RTA) data for electrical performance characteristics shall be as specified in Table III.

2.3 Design and construction. Microcircuits supplied to this WSD shall be as specified herein and on Figure 1.

2.4 Marking. Microcircuits supplied to this WSD shall be marked with the manufacturer's standard commercial PIN.

3.0 Regulatory requirements. This section is not utilized in this WSD.

TABLE I. Maximum operating conditions.

Continuous drain current I_D, V_{GS} @ 10 V, T_C = 25°C T_C = 100°C	 -11 A -6.8 A
Pulse drain current I_{DM} 1/	-44 A
Power dissipation P_D @ T_C = 25°C (PCB Mount)	125 W 3.0 W
Linear derating factor (PCB Mount)	1.0 W/°C 0.025 W/°C
Gate-to-Source voltage V_{GS}	±20 V
Single pulse avalanche energy E_{AS} 2/	700 mJ
Avalanche current I_{AR} 1/	-11 A
Repetitive avalanche energy E_{AS} 1/	13 mJ
Peak diode recovery dv/dt 3/	5.0 V/ns
Operating junction temperature T_J	-55°C to +150°C
Storage temperature T_{STG}	-55°C to +150°C
Soldering temperature for 10 seconds	300°C (1.6mm from case)

For notes 1/, 3/ and 2/, see footnotes of TABLE II.

TABLE II. Electrical Performance Characteristics.

Test	Symbol	Conditions T_J = +25°C unless otherwise specified	Group A subgroups	Limits			Units
				Min	Typ	Max	
Drain-to-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	Room	-200			V
Breakdown voltage temperature coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = -1 mA			-0.20		V/°C
Static drain-to-source on resistance	$R_{(DS)ON}$	V_{GS} = -10 V, I_D = 6.6 A 4/				0.50	Ω
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		-2.0		-4.0	V
Forward transconductance	g_{fs}	V_{DS} = -50 V, I_D = 6.6 A 4/		4.1			S
Drain-to-source leakage current	I_{DSS}	V_{DS} = -200 V, V_{GS} = 0 V				-100	µA
		V_{DS} = -160 V, V_{GS} = 0 V	Max.			-500	
Gate-to-source forward leakage current	I_{GSS}	V_{GS} = -20 V	Room			-100	nA
Gate-to-source reverse leakage current		V_{GS} = 20 V				100	
Total gate charge	Q_g	I_D = -11 A				44	nC
Gate-to-source charge	Q_{gs}	V_{DS} = -160 V				7.1	
Gate-to-drain (Miller) charge	Q_{gd}	V_{GS} = -10 V (see Figures 3.6 and 3.13) 4/				27	
Turn-on delay time	$t_{d(ON)}$	V_{DD} = -100 V			14		ns
Rise time	t_r	I_D = -11 A			43		
Turn-off delay time	$t_{d(off)}$	R_G = 9.1 Ω			39		
Fall time	t_f	R_G = 8.6 Ω (see Figure 2.10) 4/			38		
Internal drain inductance	L_D	Between lead, 6 mm (0.25in) from			4.5		nH
Internal source inductance	L_S	package and center of die contact 5A/			7.5		
Input capacitance	C_{ISS}	V_{GS} = 0 V			1200		pF
Output capacitance	C_{OSS}	V_{DS} = -25 V			370		
Reverse transfer capacitance	C_{rSS}	f = 1.0 MHz (see Figure 2.5)			81		

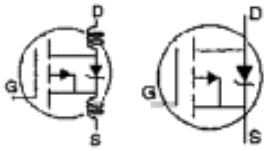
See footnotes at end of table.

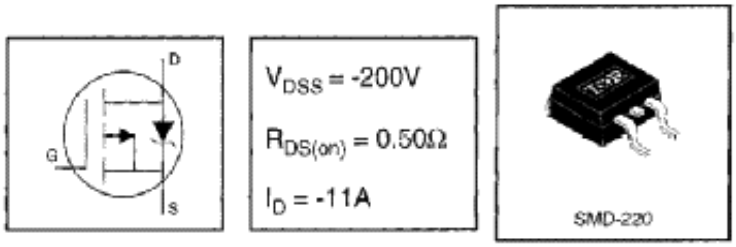
TABLE II. Electrical performance characteristics- Continued.

Test	Symbol	Conditions T_J = +25°C unless otherwise specified	Group A subgroups	Limits			Units
				Min	Typ	Max	
Source-Drain Ratings :							
Continuous source current (body diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode 5B/	Room			-11	A
Pulsed source current (body diode)	I_{SM}					-44	
Diode forward voltage	V_{SD}	I_S = -11 A, V_{GS} = 0 V 4/				-5.0	V
Reverse recovery time	t_{rr}	I_F = -11 A, di/dt = 100 A/µs 4/			250	300	ns
Reverse recovery charge	Q_{rr}				2.9	3.6	µC
Forward turn-on time	t_{on}	turn-on is dominated by L_S + L_D		intrinsic turn-on is neglible			

1/ Repetitive rating; pulse width limited by max. Junction temperature (see Figure 2.11)
2/ VDD = -50 V, starting TJ = +25°C, L = 8.7 mH, RG = 25 Ω, IAS = -11 A (see Figure 2.12).
3/ I_{SD} ≤ -11 A, di/dt ≤ 150 A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ +150°C.
4/ Pulse width ≤ 300 µs; duty cycle ≤ 2%.

Insert A. Insert B.

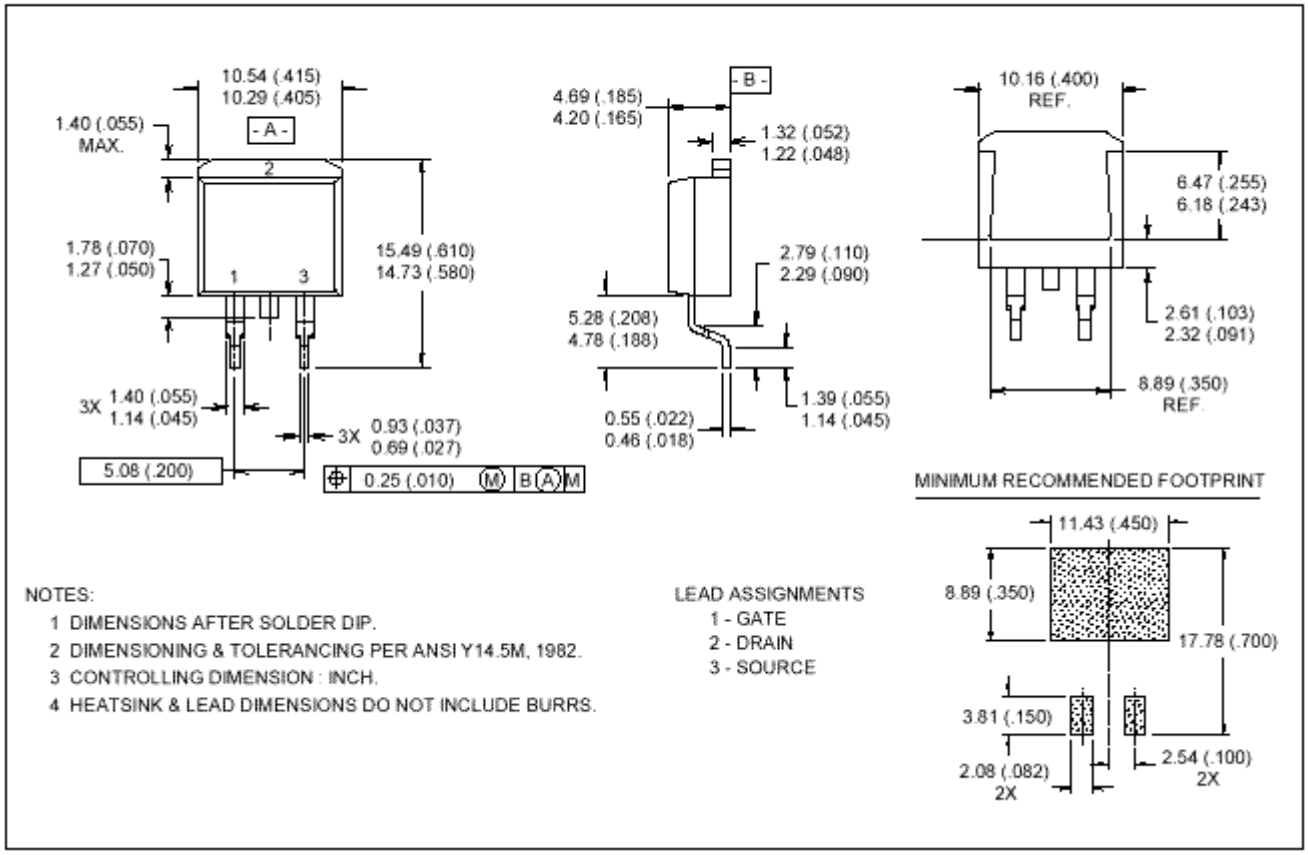




Terminal connections

HEXFET TO-263AB Outline

Dimensions are shown in millimeters (inches)

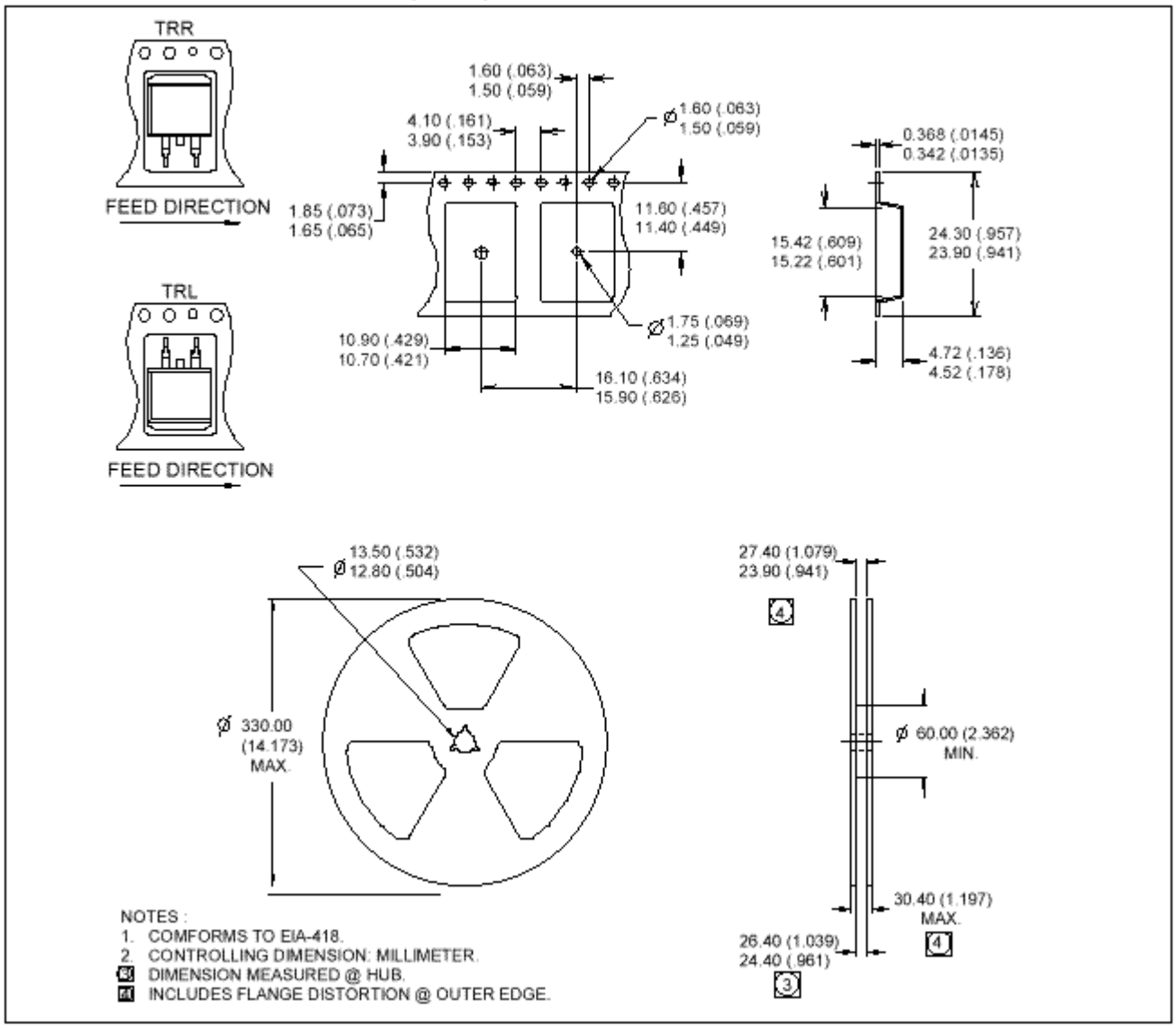


Package Outline

Figure 1. Design and construction.

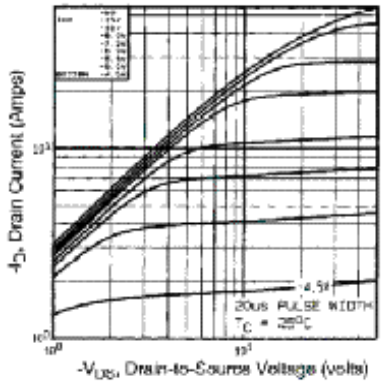
HEXFET TO-263AB

Dimensions are shown in millimeters (inches)

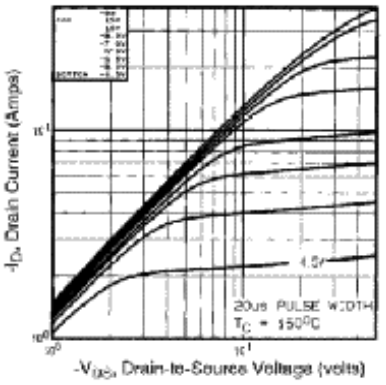


Tape & Reel Information

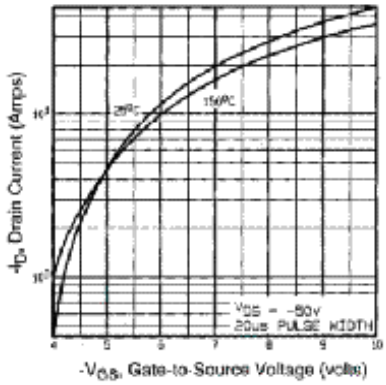
Figure 1. Design and construction- Continued.



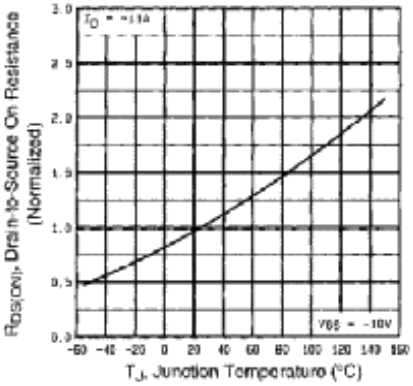
1. Typical Output Characteristics, T_C=25°C



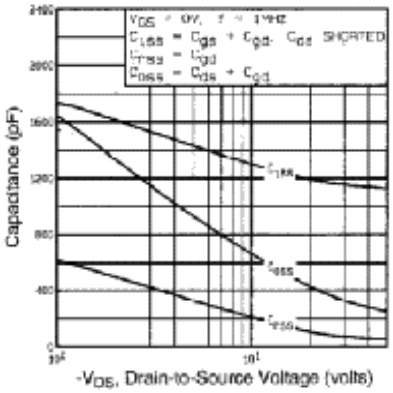
2. Typical Output Characteristics, T_C=150°C



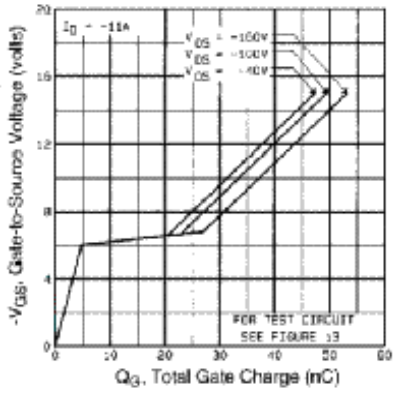
3. Typical Transfer Characteristics



4. Normalized On-Resistance Vs. Temperature

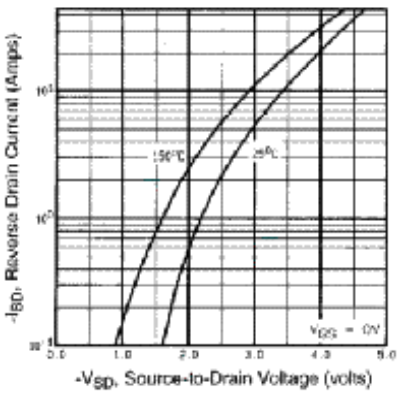


5. Typical Capacitance Vs. Drain-to-Source Voltage

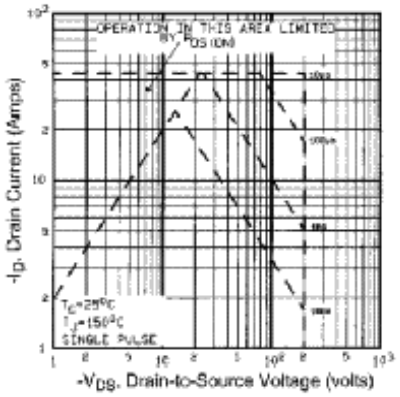


6. Typical Gate Charge Vs. Gate-to-Source Voltage

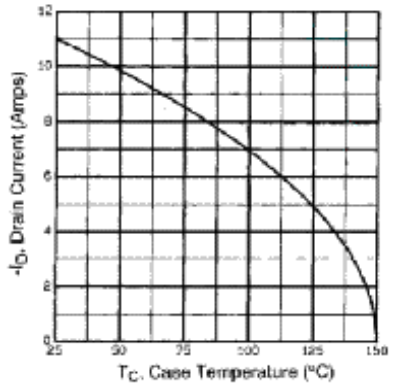
Figure 2. Typical characteristics diagrams.



7. Typical Source-Drain Diode Forward Voltage



8. Maximum Safe Operating Area



9. Maximum Drain Current Vs. Case Temperature

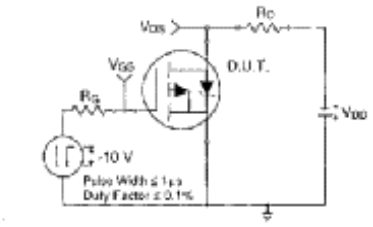
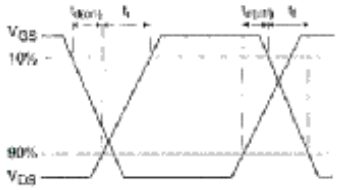
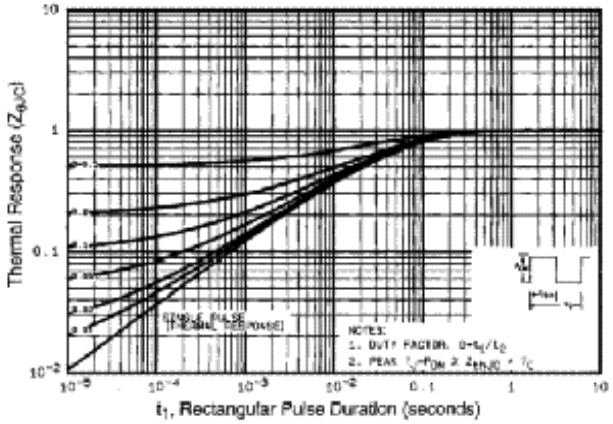


Fig 10a. Switching Time Test Circuit

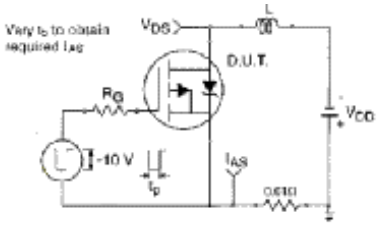


10b. Switching Time Waveforms

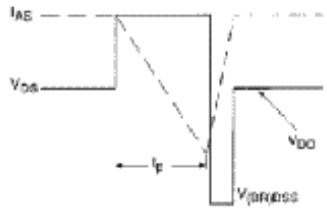


11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

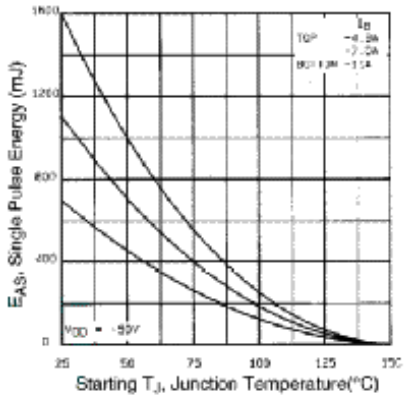
Figure 2. Typical characteristics diagrams - Continued.



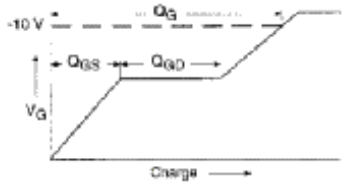
12a. Unclamped Inductive Test Circuit



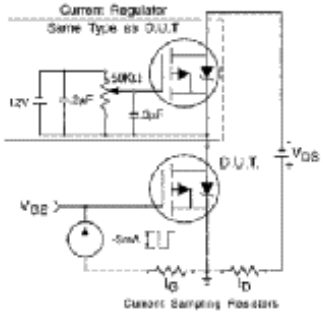
12b. Unclamped Inductive Waveforms



12c. Maximum Avalanche Energy Vs. Drain Current



13a. Basic Gate Charge Waveform



13b. Gate Charge Test Circuit

Figure 2. Typical characteristics diagrams - Continued.

4.0 Quality assurance provisions.

4.1 Responsibility for inspection. Unless otherwise specified in the contract or purchase order, the contractor is responsible for the performance of all inspection, examination, and test requirements specified herein. Except as otherwise specified in the contract or purchase order, the contractor may use his own or any other facilities suitable for the inspection requirements specified herein, unless disapproved by the Government. The Government reserves the right to perform any of the inspections, examinations, or tests set forth in this description where such inspections, examinations, and tests are deemed necessary to assure supplies and services conform to prescribed requirements.

4.2 Contractor certification statement. The contractor shall certify and maintain objective quality evidence that the product offered meets the requirements of this WSD, and that the product conforms to the producer's own drawings, specifications, standards, quality assurances practices, and is the same as the product provided as a bid sample. The acquiring activity reserves the right to require proof of such conformance prior to the first delivery and thereafter as may be otherwise provided for under the provisions of the contract.

4.3 Certificate of conformance. A certificate of conformance shall accompany all microcircuits supplied to this WSD.

5.1 Preservation, packaging, packing, labeling, and marking. Preservation, packaging, labeling, and marking shall be as specified in the contract or purchase order.

6.0 Notes. This section contains relevant information which is useful to buyers, users, and suppliers in the process of acquiring the item, but is not mandatory.

6.1 Radiation Tolerance Assured (RTA) . RTA performance is not covered under the manufacturers warranty. RTA testing has been performed and is an integral part of this drawing. The RTA performance is certified by White Sands Missile Range, Directorate for Applied Technology, Test and Simulation (WSMR, DATTS) to the performance characteristics as specified in TABLE III herein.

6.2 Electrical Performance over Temperature . Electrical performance over temperature ($-55°C \leq T_A \leq +150°C$) is covered under the manufacturers warranty. No further temperature testing is required for determining temperature related effects. There is no certification or warrantees by WSMR,DATTS to the performance characteristics specified in TABLE II herein.

TABLE III. RTA Electrical Performance Characteristics.

Test 1/	Symbol	Conditions 2/ T_J = +25°C unless otherwise specified	Limits		Units
			Min	Max	
Drain-to-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	-200		V
Static drain-to-source on resistance	$R_{(DS)ON}$	V_{GS} = -10 V, I_D = 6.6 A		0.6	Ω
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	-2.0	-4.4	V
Forward transconductance	g_{fs}	V_{DS} = -9 V, I_D = 6.6 A	3.9		S
Drain-to-source leakage current	I_{DSS}	V_{DS} = -200 V, V_{GS} = 0 V		-133	µA
Gate-to-source forward leakage current	I_{GSS}	V_{GS} = -20 V		-110	nA
Gate-to-source reverse leakage current		V_{GS} = 20 V		110	
Diode forward voltage	V_{SD}	I_S = -11 A, V_{GS} = 0 V		-5.2	V

1/ Devices supplied to this drawing will meet and only be tested at the level M of irradiation. When performing post irradiation electrical measurements for any radiation level, T_A = +25°C.
Radiation measurements at the level M are performed for:
Gamma total dose . . . . . 3000 Rads(Si)
Neutron fluence . . . . . $2.5x10^{12}$ n/cm^2/Mev
2/ All footnotes of Table II shall be applied here unless otherwise specified.

6.3 Ordering data. The contract or purchase order shall specify the following:

a. WSD document number and revision and WSD PIN.
b. Quality assurance provisions.
c. Packaging requirements.

6.4 Identification of the approved source(s) of supply hereon is not to be construed as a guarantee of present or continued availability as a source of supply for the item described on the drawing.

PART ID NUMBER	CAGE CODE	MANUFACTURER	ITEM IDENTIFICATION
W98M964001EUX	09WF0	International Rectifier	IRF9640S

09WF0

Commander, USAWSMR
ATTN: STEWS-DT-A
Building 90121
White Sands NM 88002-5158