



## **SIR Transceiver Module (115.2 kbit/s) 2.7 V to 5.5 V**



### **Description**

The TFDS4400 is a low-power infrared transceiver module compliant to the IrDA physical layer standard for infrared data communication, supporting IrDA speeds up to 115.2 kbit/s (SIR), HP-SIR, and carrier based remote control modes up to 100 kHz. Integrated within the transceiver module are a photo PIN diode, infrared emitter (IRED), and a low-power control IC to provide a total front-end solution in a single package. Vishay Semiconductors TFDS4400 transceiver represents a novel package option enabling a minimized package height over the PCB of only

1.8 mm and nevertheless offering a full 1m IrDA 1.2 transmission range. The transceiver is capable of directly interfacing with a wide variety of I/O chips which perform the modulation/demodulation function, including National Semiconductor's PC87338, PC87108 and PC87109, SMC's FDC37C669, FDC37N769 and CAM35C44, and Hitachi's SH3. At a minimum, a current-limiting resistor in series with the infrared emitter and a  $V_{CC}$  bypass capacitor are the only external components required to implement a complete solution.

### **Features**

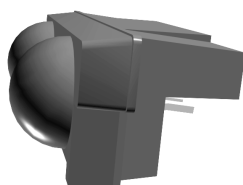
- Compliant to the latest IrDA physical layer standard (Up to 115.2 kbit/s), HP-SIR®, Sharp ASK® and TV Remote
- **For Sunk Mounting at the PCB Edge**
  - 1.8 mm Height over Board
- Operating 2.7 V to 5.5 V Applications
- Low-Power Consumption  
1.0 (1.3) mA Supply Current @ 3 V (5 V)
- Power Sleep Mode Through  $V_{CC1}$  (5 nA Sleep Current)
- Electrically identical to the TFDU4100 device
- High Efficiency Emitter
- Directly Interfaces with Various Super I/O and Controller Devices
- Built-In EMI Protection – No External Shielding Necessary
- Few External Components Required

### **Applications**

- Telecommunication Products (Cellular Phones, Pagers)
- Computers (Win CE, Palm PC), PDAs
- Digital Still and Video Cameras
- External Infrared Adapters (Dongles)
- Medical and Industrial Data Collection

### **Package**

TFDS4400  
Dracula



## Ordering Information

| Part Number  | Qty / Reel | Description |
|--------------|------------|-------------|
| TFDS4400-TR3 | 1000 pcs   |             |

## Functional Block Diagram

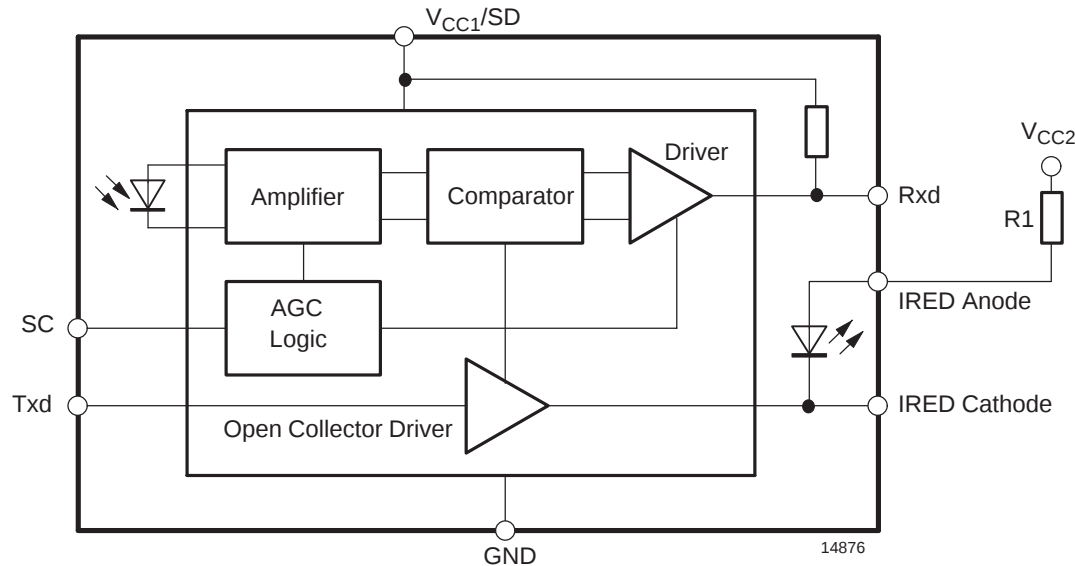


Figure 1. Functional Block Diagram

## Pin Description

| Pin Number | Function     | Description                                                                                                                                                                   | I/O | Active |
|------------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|--------|
| 1          | IRED Anode   | IRED Anode, should be externally connected to $V_{CC2}$ through a current control resistor                                                                                    |     |        |
| 2          | IRED Cathode | IRED Cathode, internally connected to driver transistor                                                                                                                       |     |        |
| 3          | Txd          | Transmit Data Input                                                                                                                                                           | I   | HIGH   |
| 4          | Rxd          | Received Data Output, open collector. No external pull-up or pull-down resistor is required (20 k $\Omega$ resistor internal to device). Pin is inactive during transmission. | O   | LOW    |
| 5          | NC           | Do not connect, reserved for future features                                                                                                                                  |     |        |
| 6          | $V_{CC1}$    | Supply Voltage                                                                                                                                                                |     |        |
| 7          | SC           | Sensitivity control, increases sensitivity when active                                                                                                                        | I   | HIGH   |
| 8          | GND          | Ground                                                                                                                                                                        |     |        |

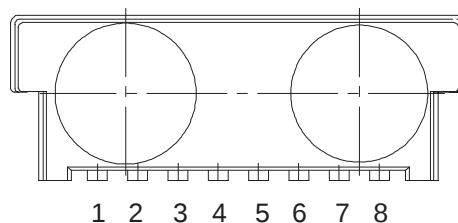


Figure 2. Pinning



## Absolute Maximum Ratings

Reference point Pin GND unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

| Parameters                                                                                                         | Test Conditions                               | Symbol          | Min.  | Typ. | Max.          | Unit  |
|--------------------------------------------------------------------------------------------------------------------|-----------------------------------------------|-----------------|-------|------|---------------|-------|
| Supply Voltage Range                                                                                               | $0\text{ V} \leq V_{CC2} \leq 6\text{ V}$     | $V_{CC1}$       | - 0.5 |      | 6             | V     |
|                                                                                                                    | $0\text{ V} \leq V_{CC1} \leq 6\text{ V}$     | $V_{CC2}$       | - 0.5 |      | 6             | V     |
| Input Currents                                                                                                     | For all Pins,<br>except IRED Anode Pin        |                 |       |      | 10            | mA    |
| Output Sink Current                                                                                                |                                               |                 |       |      | 25            | mA    |
| Power Dissipation                                                                                                  | See Derating Curve                            | $P_D$           |       |      | 200           | mW    |
| Junction Temperature                                                                                               |                                               | $T_J$           |       |      | 125           | °C    |
| Ambient Temperature<br>Range (Operating)                                                                           |                                               | $T_{amb}$       | -25   |      | +85           | °C    |
| Storage Temperature<br>Range                                                                                       |                                               | $T_{stg}$       | -25   |      | +85           | °C    |
| Soldering Temperature                                                                                              | See Recommended<br>Solder Profile             |                 |       | 215  | 240           | °C    |
| Average IRED Current                                                                                               |                                               | $I_{IRED} (DC)$ |       |      | 100           | mA    |
| Repetitive Pulsed IRED<br>Current                                                                                  | $t < 90\text{ }\mu\text{s}$ , $t_{on} < 20\%$ | $I_{IRED} (RP)$ |       |      | 500           | mA    |
| IRED Anode Voltage                                                                                                 |                                               | $V_{IRED A}$    | - 0.5 |      | 6             | V     |
| Transmitter Data Input<br>Voltage                                                                                  |                                               | $V_{Txd}$       | - 0.5 |      | $V_{CC1}+0.5$ | V     |
| Receiver Data Output<br>Voltage                                                                                    |                                               | $V_{Rxd}$       | - 0.5 |      | $V_{CC1}+0.5$ | V     |
| Virtual Source Size                                                                                                | Method:<br>(1-1/e) encircled energy           | d               | 2.5   | 2.8  |               | mm    |
| Maximum Intensity for<br>Class 1 Operation of<br>IEC825-1 or EN60825-1<br>(worst case IrDA SIR<br>pulse pattern *) | EN60825, 1997                                 |                 |       |      | 400           | mW/sr |

- \*) Note:  
Transmitted data: continuously transmitted "0". In normal data transfer operation "0" and "1" will be transmitted with the same probability. Therefore, for that case, about a factor of two of safety margin is included. However, for worst case thermal stress testing such data pattern are often used and for this case the 400 mW/sr value has to be taken.

## Electrical Characteristics

$T_{amb} = 25^{\circ}\text{C}$ ,  $V_{CC} = 2.7\text{ V}$  to  $5.5\text{ V}$  unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

| Parameters                                            | Test Conditions / Pins                                                                                             | Symbol               | Min.       | Typ.       | Max.       | Unit          |
|-------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------|----------------------|------------|------------|------------|---------------|
| <b>Transceiver</b>                                    |                                                                                                                    |                      |            |            |            |               |
| Supply Voltage                                        | Receive Mode<br>Transmit Mode, $R_2 = 47\ \Omega$<br>(see Recommended Application Circuit)                         | $V_{CC1}$            | 2.7<br>2.0 |            | 5.5<br>5.5 | V<br>V        |
| Supply Current Pin $V_{CC1}$<br>(Receive Mode)        | $V_{CC1} = 5.5\text{ V}$<br>$V_{CC1} = 2.7\text{ V}$                                                               | $I_{CC1}(\text{Rx})$ |            | 1.3<br>1.0 | 2.5<br>1.5 | mA<br>mA      |
| Supply Current Pin $V_{CC1}$<br>(avg) (Transmit Mode) | $I_{\text{RED}} = 210\text{ mA}$<br>(at IRED Anode Pin)<br>$V_{CC1} = 5.5\text{ V}$<br>$V_{CC1} = 2.7\text{ V}$    | $I_{CC1}(\text{Tx})$ |            | 5.0<br>3.5 | 5.5<br>4.5 | mA<br>mA      |
| Leakage Current of IR<br>Emitter, IRED Anode Pin      | $V_{CC1} = \text{OFF}$ , $T_{XD} = \text{LOW}$ ,<br>$V_{CC2} = 6\text{ V}$ , $T = 25\text{ to }85^{\circ}\text{C}$ | $I_L(\text{IRED A})$ |            | 0.005      | 0.5        | $\mu\text{A}$ |
| Transceiver Power On<br>Settling Time                 |                                                                                                                    | $T_{\text{PON}}$     |            | 50         |            | $\mu\text{s}$ |

## Optoelectronic Characteristics

$T_{amb} = 25^{\circ}\text{C}$ ,  $V_{CC} = 2.7\text{ V}$  to  $5.5\text{ V}$  unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

| Parameters                                | Test Conditions                                              | Symbol            | Min.          | Typ. | Max. | Unit                   |
|-------------------------------------------|--------------------------------------------------------------|-------------------|---------------|------|------|------------------------|
| <b>Receiver</b>                           |                                                              |                   |               |      |      |                        |
| Minimum Detection<br>Threshold Irradiance | $\text{BER} = 10^{-8}$ (IrDA Specification)                  |                   |               |      |      |                        |
|                                           | $\alpha = \pm 15^{\circ}$ , SIR Mode, SC = LOW               | $E_e$             |               | 20   | 35   | $\text{mW}/\text{m}^2$ |
|                                           | $\alpha = \pm 15^{\circ}$ , SIR Mode, SC = HIGH              | $E_e$             | 6             | 10   | 15   | $\text{mW}/\text{m}^2$ |
| Maximum Detection<br>Threshold Irradiance | $\alpha = \pm 90^{\circ}$ , SIR Mode, $V_{CC1} = 5\text{ V}$ | $E_e$             | 3.3           | 5    |      | $\text{kW}/\text{m}^2$ |
|                                           | $\alpha = \pm 90^{\circ}$ , SIR Mode, $V_{CC1} = 3\text{ V}$ | $E_e$             | 8             | 15   |      | $\text{kW}/\text{m}^2$ |
| Logic LOW Receiver<br>Input Irradiance    | SC = HIGH or LOW                                             | $E_e$             |               |      | 4    | $\text{mW}/\text{m}^2$ |
| Output Voltage –<br>Rxd                   | Active, $C = 15\text{ pF}$ , $R = 2.2\text{ k}\Omega$        | $V_{\text{OL}}$   |               | 0.5  | 0.8  | V                      |
|                                           | Non-active, $C = 15\text{ pF}$ , $R = 2.2\text{ k}\Omega$    | $V_{\text{OH}}$   | $V_{CC1}-0.5$ |      |      | V                      |
| Output Current –<br>Rxd                   | $V_{\text{OL}} < 0.8\text{ V}$                               | $I_{\text{OL}}$   |               | 4    |      | mA                     |
| Rise Time – Rxd                           | $C = 15\text{ pF}$ , $R = 2.2\text{ k}\Omega$                | $t_r(\text{Rxd})$ | 20            |      | 1400 | ns                     |
| Fall Time – Rxd                           | $C = 15\text{ pF}$ , $R = 2.2\text{ k}\Omega$                | $t_f(\text{Rxd})$ | 20            |      | 200  | ns                     |
| Pulse Width – Rxd<br>Output               | Input pulse width = $1.6\ \mu\text{s}$ ,<br>115.2 kbit/s     | $t_{\text{PW}}$   | 1.41          |      | 8    | $\mu\text{s}$          |
| Jitter, Leading Edge<br>of Output Signal  | Over a Period of 10 bit, 115.2 kbit/s                        | $t_j$             |               |      | 2    | $\mu\text{s}$          |
| Latency                                   |                                                              | $t_L$             |               | 100  | 500  | $\mu\text{s}$          |



## Optoelectronic Characteristics

$T_{amb} = 25^{\circ}\text{C}$ ,  $V_{CC} = 2.7\text{ V}$  to  $5.5\text{ V}$  unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

| Parameters                                              | Test Conditions                                                                                                                                                               | Symbol                     | Min. | Typ.     | Max.          | Unit          |
|---------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|------|----------|---------------|---------------|
| <b>Transmitter</b>                                      |                                                                                                                                                                               |                            |      |          |               |               |
| IRE D Operating Current                                 | IRE D Operating Current can be adjusted by Variation of R1. Current Limiting Resistor is in Series to IRE D:<br>$R1 = 14\ \Omega$ , $V_{CC2} = 5.0\text{ V}$                  | $I_{IRE D}$                |      | 0.2      | 0.28          | A             |
| Logic LOW Transmitter Input Voltage                     |                                                                                                                                                                               | $V_{IL} (Txd)$             | 0    |          | 0.8           | V             |
| Logic HIGH Transmitter Input Voltage                    |                                                                                                                                                                               | $V_{IH} (Txd)$             | 2.4  |          | $V_{CC1}+0.5$ | V             |
| Output Radiant Intensity                                | In Agreement with IEC825 Eye Safety Limit, if Current Limiting Resistor is in Series to IRE D:<br>$R1 = 14\ \Omega$ , $V_{CC2} = 5.0\text{ V}$ ,<br>$\alpha = \pm 15^{\circ}$ | $I_e$                      | 45   | 140      | 200           | mW/sr         |
|                                                         | Txd Logic LOW Level                                                                                                                                                           | $I_e$                      |      |          | 0.04          | mW/sr         |
| Angle of Half Intensity                                 |                                                                                                                                                                               | $a$                        |      | $\pm 24$ |               | $^{\circ}$    |
| Peak Wavelength of Emission                             |                                                                                                                                                                               | $\lambda_p$                | 880  |          | 900           | nm            |
| Half-Width of Emission Spectrum                         |                                                                                                                                                                               |                            |      | 60       |               | nm            |
| Optical Rise Time, Fall Time                            |                                                                                                                                                                               | $t_{ropt}$ ,<br>$t_{fopt}$ |      | 200      | 600           | ns            |
| Optical Overshoot                                       |                                                                                                                                                                               |                            |      |          | 25            | %             |
| Rising Edge Peak-to-Peak Jitter of Optical Output Pulse | Over a Period of 10 bits, Independent of Information content                                                                                                                  |                            |      |          | 0.2           | $\mu\text{s}$ |

## Recommended Circuit Diagram

The only required components for designing an IrDA 1.2 compatible design using Vishay SIR transceivers are a current limiting resistor to the IRED. However, depending on the entire system design and board layout, additional components may be required (see figure KEIN MERKER). It is recommended that the capacitors C1 and C2 are positioned as near as possible to the transceiver power supply pins. A tantalum capacitor should be used for C1, while a ceramic capacitor should be used for C2 to suppress RF noise. Also, when connecting the described circuit to the power supply, low impedance wiring should be used.

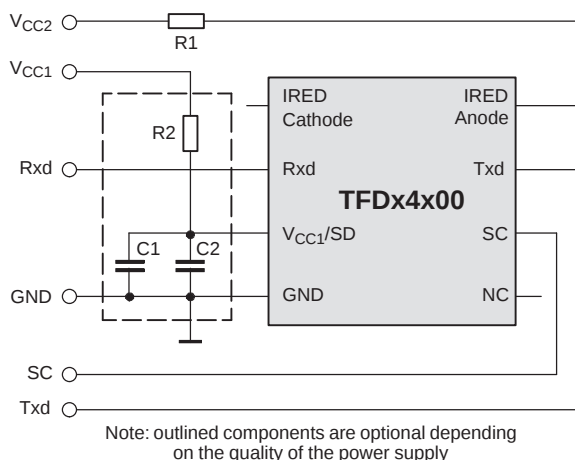


Figure 3. Recommended Application Circuit

R1 is used for controlling the current through the IRED emitter. For increasing the output power of the IRED, the value of the resistor should be reduced. Similarly, to reduce the output power of the IRED, the value of the resistor should be increased. For typical values of R1 (see figures 4 and 5), e.g. for IrDA compliant operation ( $V_{CC2} = 5\text{ V} \pm 5\%$ ), a current control resistor of  $14\ \Omega$  is recommended. The upper drive current limitation is dependent on the duty cycle and is given by the absolute maximum ratings on the data sheet and the eye safety limitations given by IEC825–1. R2, C1 and C2 are optional and dependent on the quality of the supply voltage  $V_{CC1}$  and injected noise. An unstable power supply with dropping voltage during transmission may reduce sensitivity (and transmission range) of the transceiver.

### Table 1. Recommended Application Circuit Components

| Component | Recommended Value                                                                     | Vishay Part Number   |
|-----------|---------------------------------------------------------------------------------------|----------------------|
| C1        | 4.7 $\mu$ F, Tantalum                                                                 | 293D 475X9 016B 2T   |
| C2        | 0.1 $\mu$ F, Ceramic                                                                  | VJ 1206 Y 104 J XXMT |
| R1        | 14 $\Omega$ , 0.25 W (recommended using two 7 $\Omega$ , 0.125 W resistors in series) | CRCW-1206-6R98-F-RT1 |
| R2        | 47 $\Omega$ , 0.125 W                                                                 | CRCW-1206-47R0-F-RT1 |

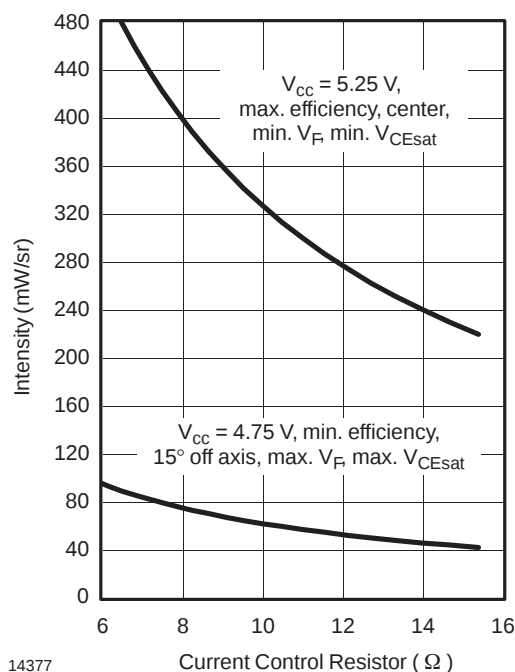


Figure 4.  $I_e$  vs.  $R1$

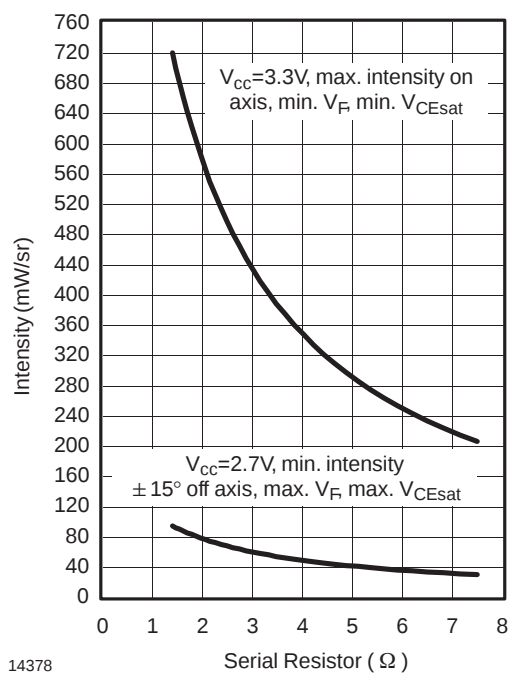


Figure 5.  $I_e$  vs.  $R1$

The sensitivity control (SC) pin allows the minimum detection irradiance threshold of the transceiver to be lowered when set to a logic HIGH. Lowering the irradiance threshold increases the sensitivity to infrared signals and increases transmission range up to 3 meters. However, setting the Pin SC to logic HIGH also makes the transceiver more susceptible to transmission errors due to an increased sensitivity to fluorescent light disturbances. It is recommended to set the Pin SC to logic LOW or left open if the increased range is not required or if the system will be operating in bright ambient light.

The guide pins on the side-view and top-view packages are internally connected to ground but should not be connected to the system ground to avoid ground loops. They should be used for mechanical purposes only and should be left floating.

## Shutdown

The internal switch for the IRED in Vishay SIR transceivers is designed to be operated like an open collector driver. Thus, the  $V_{CC2}$  source can be an unregulated power supply while only a well regulated power source with a supply current of 1.3 mA connected to  $V_{CC1}/SD$  is needed to provide power to the remainder of the transceiver circuitry in receive mode. In transmit mode, this current is slightly higher (approximately 4 mA average at 3 V supply current) and the voltage is not required to be kept as stable as in receive mode. A voltage drop of  $V_{CC1}$  is acceptable down to about 2.0 V when buffering the voltage directly from the Pin  $V_{CC1}$  to GND see figure 3.

This configuration minimizes the influence of high current surges from the IRED on the internal analog control circuitry of the transceiver and the application circuit. Also board space and cost savings can be achieved by eliminating the additional linear regulator normally needed for the IRED's high current requirements.

The transceiver can be very efficiently shutdown by keeping the IRED connected to the power supply  $V_{CC2}$  but switching off  $V_{CC1}/SD$ . The power source to  $V_{CC1}/SD$  can be provided directly from a microcontroller (see figure 6). In shutdown, current loss is realized only as leakage current through the current limiting resistor to the IRED (typically 5 nA). The settling time after switching  $V_{CC1}/SD$  on again is approximately 50  $\mu$ s. Vishay TOIM3232

interface circuit is designed for this shutdown feature. The  $V_{CC\_SD}$ , S0 or S1 outputs on the TOIM3232 can be used to power the transceiver with the necessary supply current.

If the microcontroller or the microprocessor is unable to drive the supply current required by the transceiver, a low-cost SOT23 pnp transistor can be used to switch voltage on and off from the regulated power supply (see figure 7). The additional component cost is minimal and saves the system designer additional power supply costs.

As external filter, only a capacitor is recommended.

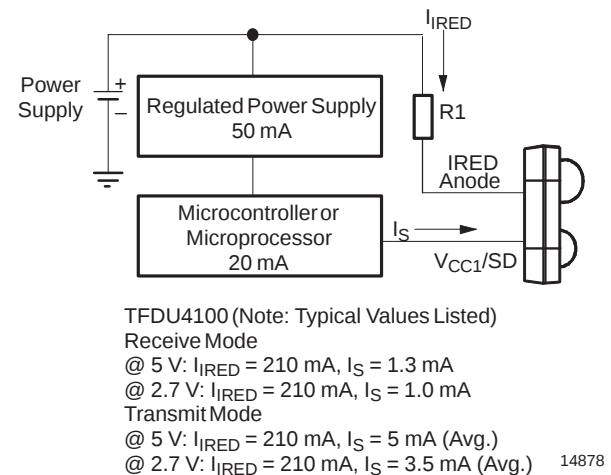


Figure 6.

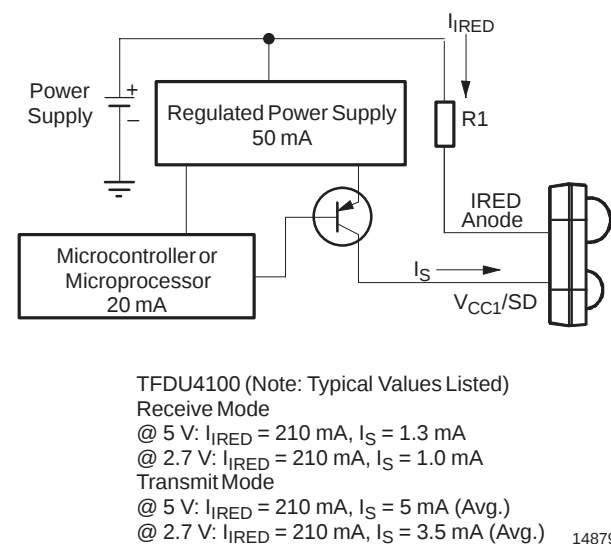


Figure 7.

Recommended SMD Pad Layout

The leads of the device should be soldered in the center position of the pads.

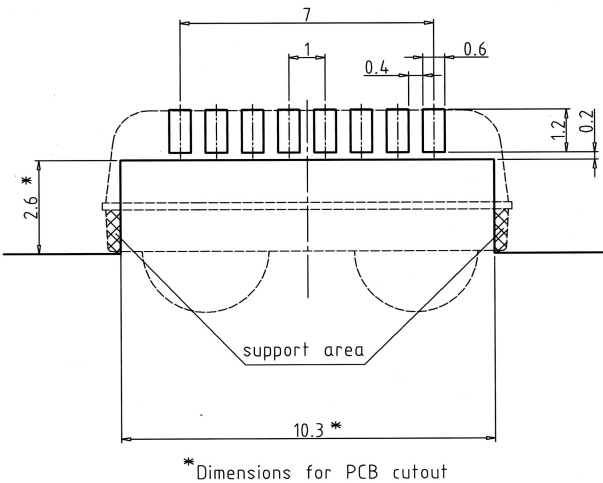


Figure 8. TFDS4400 (Dracula)

Note: Leads of the device should be at least 0.3 mm within the ends of the pads.  
Recommended Solder Profile.

Recommended Solder Profile

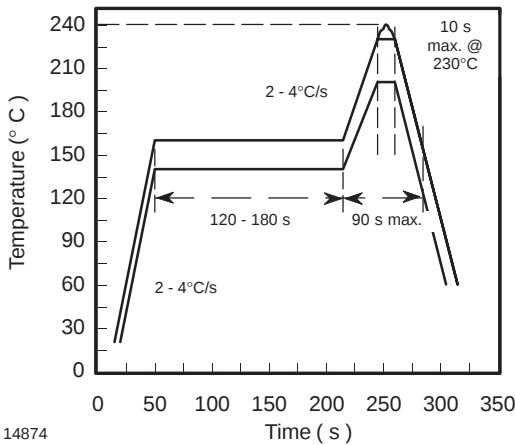


Figure 9. Recommended Solder Profile

Current Derating Diagram

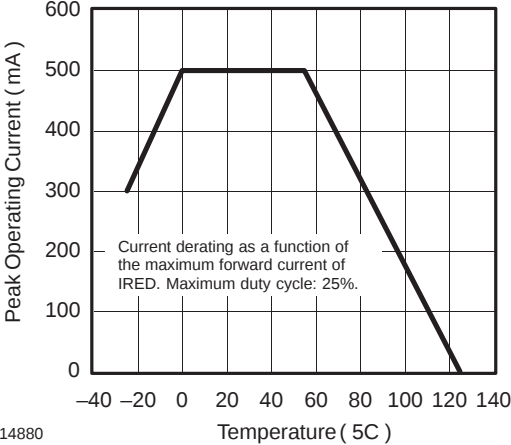
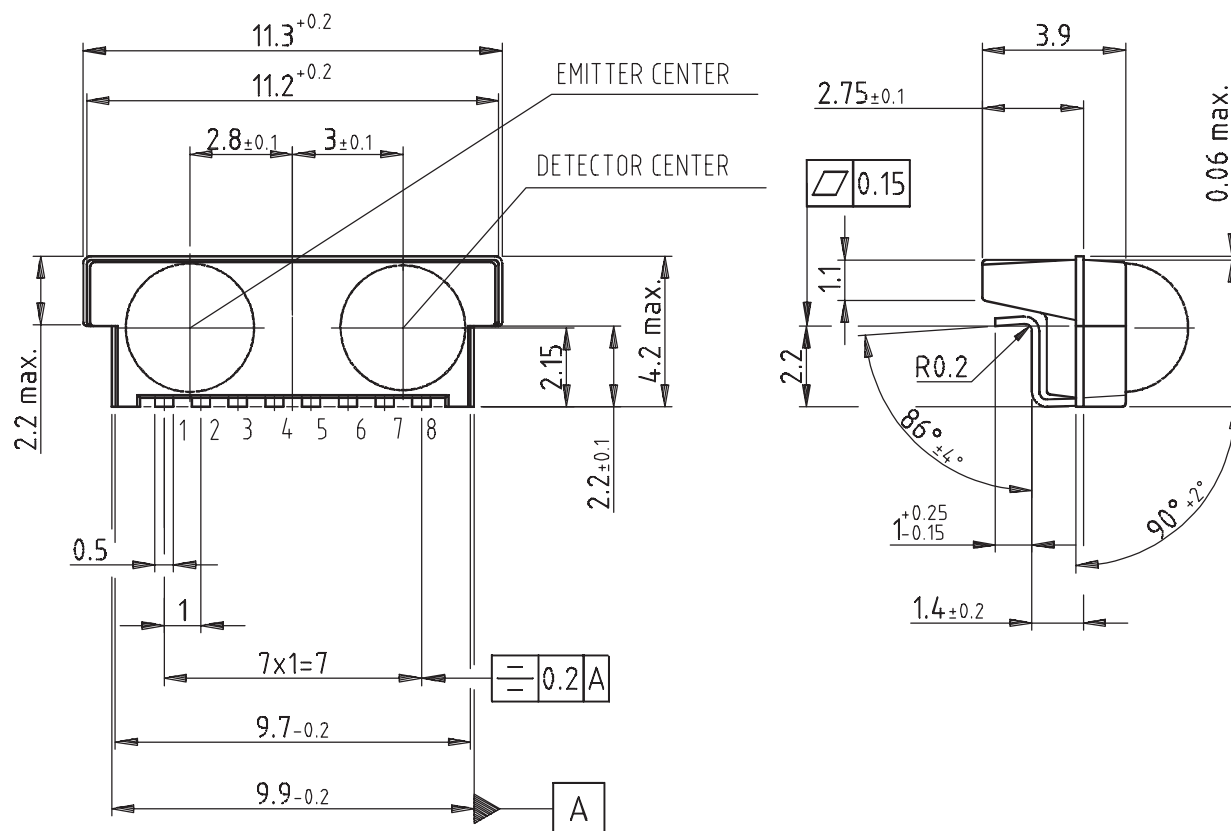


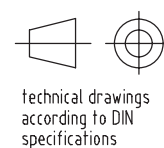
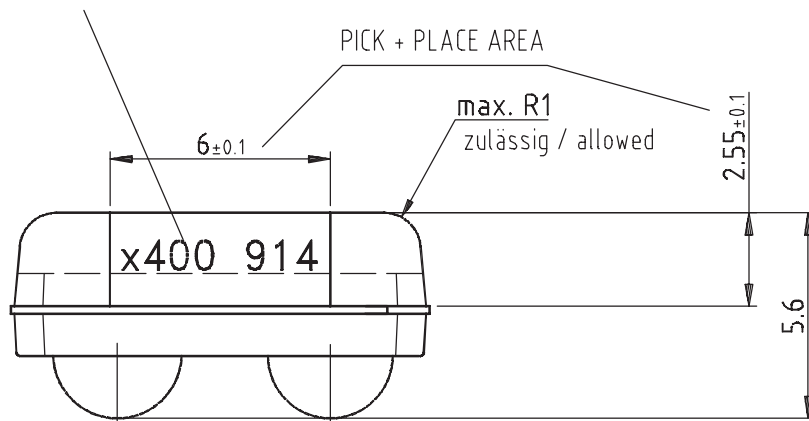
Figure 10. Current Derating Diagram

## TFDS4400 Package (Mechanical Dimensions)



\* MARKING SAMPLE ONLY

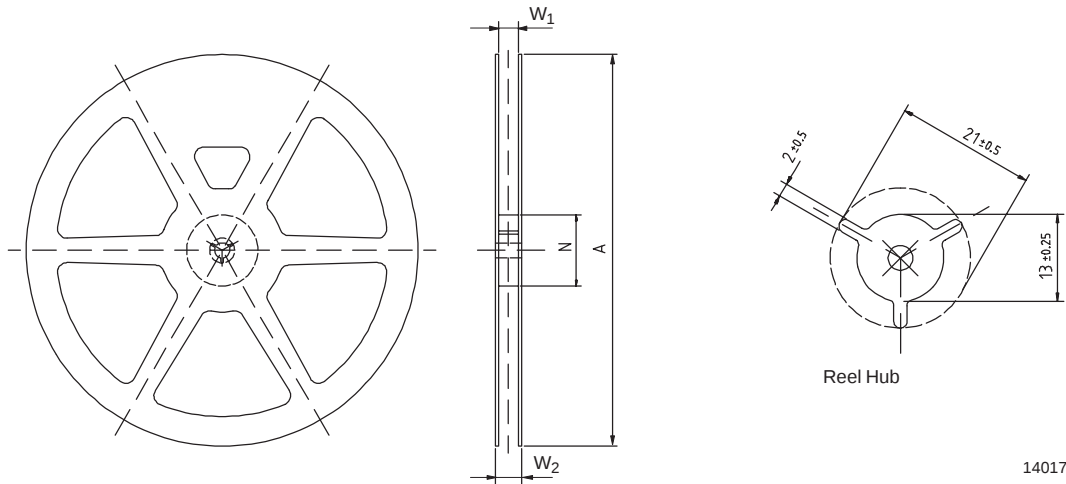
\* MARKING ORIENTATION  
180 DEGREES ALLOWED



Drawing-No.: 6.550-5203.01-3  
Issue: 2; 03.07.00

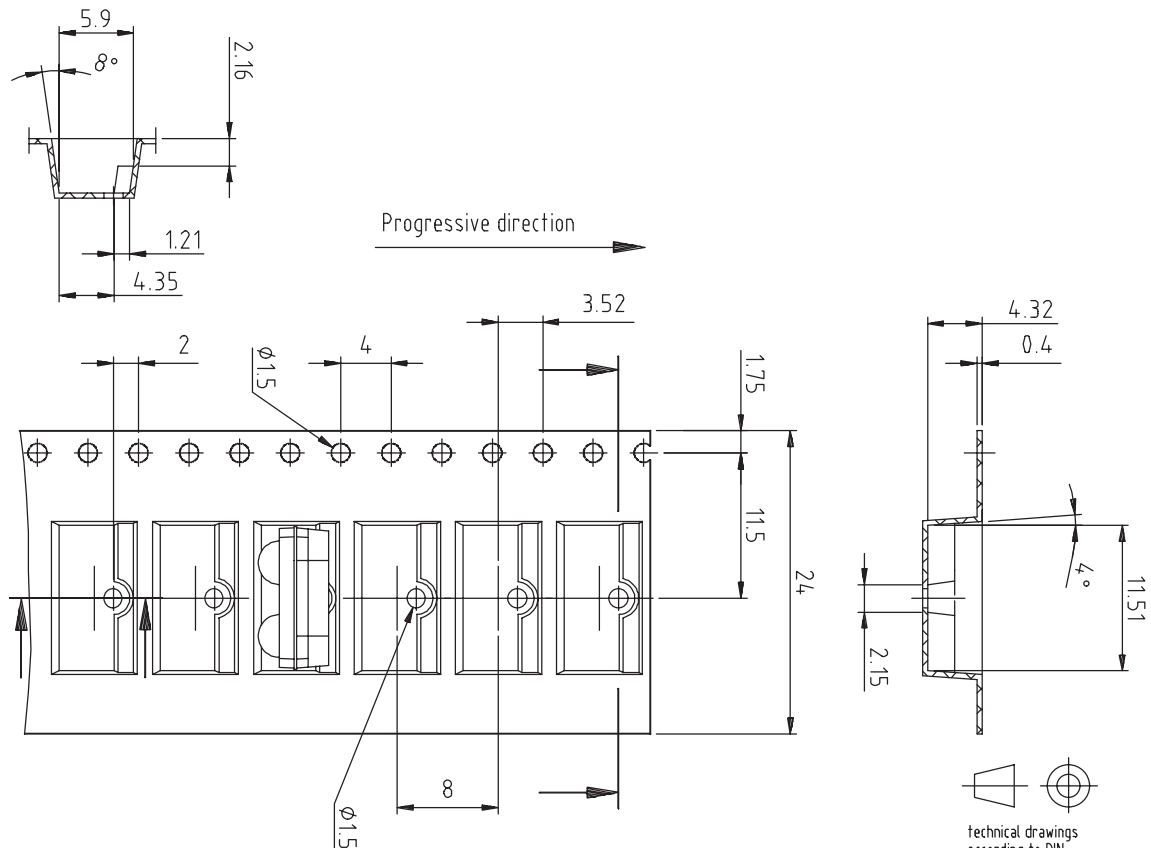
15971

Shape of Reel and Dimensions



| Version | Tape Width | A       | N         | W <sub>1</sub> | W <sub>2</sub> max |
|---------|------------|---------|-----------|----------------|--------------------|
| C       | 24         | 330 ± 1 | 100 + 1.5 | 24.4 + 2       | 30.4               |

Tape Dimensions



Drawing-No.: 9.700-5226.01-4  
Issue: 1; 31.01.00

Drawing refers to following types: TFDS .400

15182

## Leader and Trailer

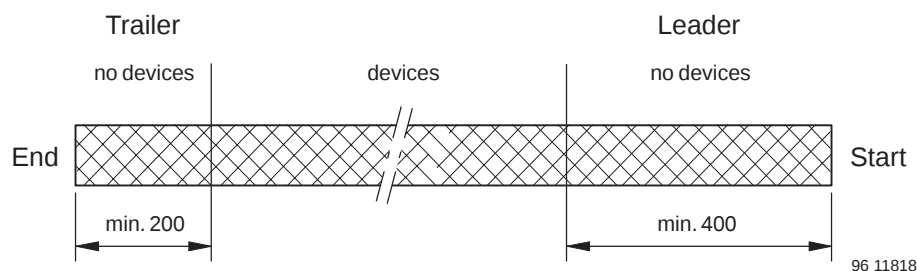


Figure 11. Leader and trailer

## Cover Tape Peel Strength

According to IEC 286  
0.1 N to 1.3 N  
300 ± 10% mm/min  
165° – 180° peel angle

## Label

### Standard bar code labels for finished goods

The standard bar code labels are product labels and used for identification of goods. The finished goods are packed in final packing area. The standard packing units are labeled with standard bar code labels before transported as finished goods to warehouses. The labels are on each packing unit and contain Vishay Semiconductor GmbH specific data.

### Vishay Semiconductor GmbH standard bar code product label (finished goods)

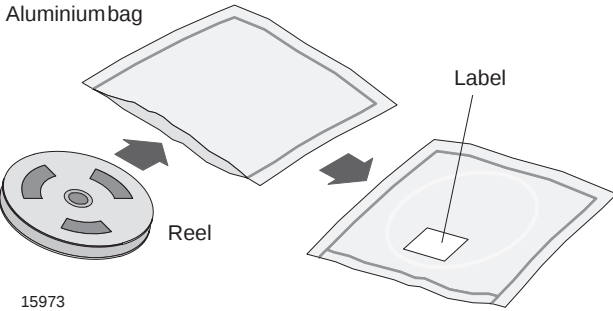
| Plain Writing        | Abbreviation | Length       |
|----------------------|--------------|--------------|
| Item-Description     | –            | 18           |
| Item-Number          | INO          | 8            |
| Selection-Code       | SEL          | 3            |
| LOT-/ Serial-Number  | BATCH        | 10           |
| Data-Code            | COD          | 3 (YWW)      |
| Plant-Code           | PTC          | 2            |
| Quantity             | QTY          | 8            |
| Accepted by:         | ACC          | –            |
| Packed by:           | PCK          | –            |
| Mixed Code Indicator | MIXED CODE   | –            |
| Origin               | xxxxxxx+     | Company logo |

| Long Bar Code Top | Type | Length |
|-------------------|------|--------|
| Item-Number       | N    | 8      |
| Plant-Code        | N    | 2      |
| Sequence-Number   | X    | 3      |
| Quantity          | N    | 8      |
| Total Length      | –    | 21     |

| Short Bar Code Bottom | Type | Length |
|-----------------------|------|--------|
| Selection-Code        | X    | 3      |
| Date-Code             | N    | 3      |
| Batch-Number          | X    | 10     |
| Filler                | –    | 1      |
| Total Length          | –    | 17     |

### Dry Packing

The reel is packed in an anti-humidity bag to protect the devices from absorbing moisture during transportation and storage.



### Final Packing

The sealed reel is packed into a cardboard box, which is 345 × 345 × 40 mm in size. A secondary cardboard box is used for shipping purposes, with the following size contents:

| Size<br>(Length × Width × Heights) | Quantity of boxes<br>(345 × 345 × 40 mm) |
|------------------------------------|------------------------------------------|
| 390 × 390 × 250 mm                 | 1                                        |
| 390 × 390 × 250 mm                 | 6                                        |

### Recommended Method of Storage

Dry box storage is recommended as soon as the aluminium bag has been opened to prevent moisture absorption. The following conditions should be observed, if dry boxes are not available:

- Storage temperature 10°C to 30°C
- Storage humidity ≤ 60% RH max.

After more than 72 hours under these conditions moisture content will be too high for reflow soldering.

In case of moisture absorption, the devices will recover to the former condition by drying under the following condition:

- 192 hours at 40°C +5°C/ -0°C and <5% RH (dry air/ nitrogen) or
- 96 hours at 60°C +5°C and <5% RH for all device containers or
- 24 hours at 125°C +5°C not suitable for reel or tubes.

An EIA JEDEC Standard JESD22-A112 Level 4 label is included on all aluminium bags

**CAUTION**  
This bag contains  
MOISTURE -SENSITIVE DEVICES

LEVEL

4

1. Shelf life in sealed bag 12 months at <40°C and < 90% relative humidity (RH)
2. After this bag is opened devices that will be subjected to infrared reflow, vapor-phase reflow, or equivalent processing (peak package body temp. 220°C) must be:
 

2a. Mounted within **72 hours** at factory condition of ≤ 30°C/60%RH or
2b. Stored at ≤20% RH.
3. Devices require baking before mounting if:  
 Humidity Indicator Card is >20% when read at 23°C ± 5°C or  
 2a or 2b is not met.
4. If baking is required, devices may be baked for:
 

**192 hours** at 40°C + 5°C/-0°C and <5%RH (dry air/nitrogen) or
**96 hours** at 60±5°C and <5%RH For all device containers or

**24 hours** at 125±5°C
Not suitable for reels or tubes

Bag Seal Date: \_\_\_\_\_  
 (If blank, see bar code label)

Note: LEVEL defined by EIA JEDEC Standard JESD22-A112

Example of JESD22-A112 Level 4 label

### ESD Precaution

Proper storage and handling procedures should be followed to prevent ESD damage to the devices especially when they are removed from the Antistatic Shielding Bag. Electro-Static Sensitive Devices warning labels are on the packaging.

### Vishay Semiconductors Standard Bar-Code Labels

The Vishay Semiconductors standard bar-code labels are printed at final packing areas. The labels are on each packing unit and contain Vishay Semiconductors specific data.





## **Revision History:**

A1.2, 06/05/1999: First released edition

A1.4, 18/08/1999: p1:Description and applications corr., p2: pinning added

A1.5, 31/05/2000 Packing and storage information added



### Ozone Depleting Substances Policy Statement

It is the policy of **Vishay Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

**Vishay Semiconductor GmbH** has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

**Vishay Semiconductor GmbH** can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

**We reserve the right to make changes to improve technical design and may do so without further notice.**

Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use Vishay Semiconductors products for any unintended or unauthorized application, the buyer shall indemnify Vishay Semiconductors against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

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