

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

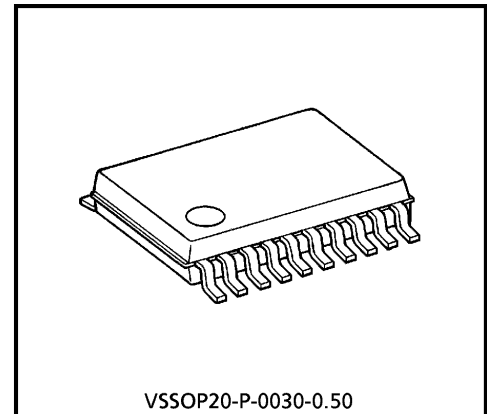
**TC7MZ574FK****LOW VOLTAGE OCTAL D-TYPE FLIP-FLOP  
WITH 5 V TOLERANT INPUTS AND OUTPUTS**

The TC7MZ574 is a high performance CMOS OCTAL D-TYPE FLIP FLOP. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3 V)  $V_{CC}$  applications, but it could be used to interface to 5 V supply environment for both inputs and outputs.

This 8 bit D-type flip-flop is controlled by a clock input (CK) and an output enable input ( $\overline{OE}$ ). When the  $\overline{OE}$  input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge.



VSSOP20-P-0030-0.50

Weight : 0.03 g (typ.)

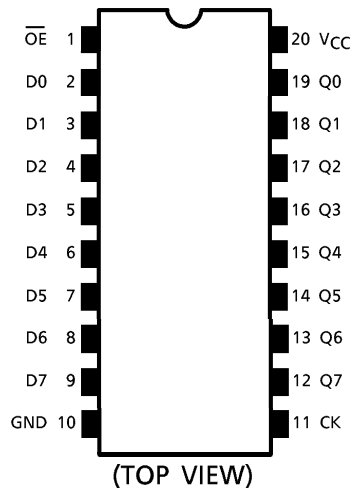
**Features**

- Low voltage operation :  $V_{CC} = 2.0\sim 3.6\text{ V}$
- High speed operation :  $t_{pd} = 8.5\text{ ns (max)}$   
( $V_{CC} = 3.0\sim 3.6\text{ V}$ )
- Output current :  $|I_{OH}|/I_{OL} = 24\text{ mA (min)}$   
( $V_{CC} = 3.0\text{ V}$ )
- Latch-up performance :  $\pm 500\text{ mA}$
- Available in VSSOP (US20)
- Power down protection is provided on all inputs and outputs.
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 574 type.

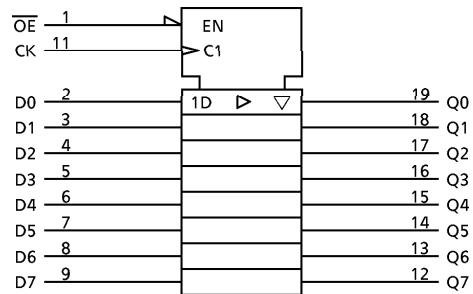
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**Pin Assignment**



**IEC Logic Symbol**

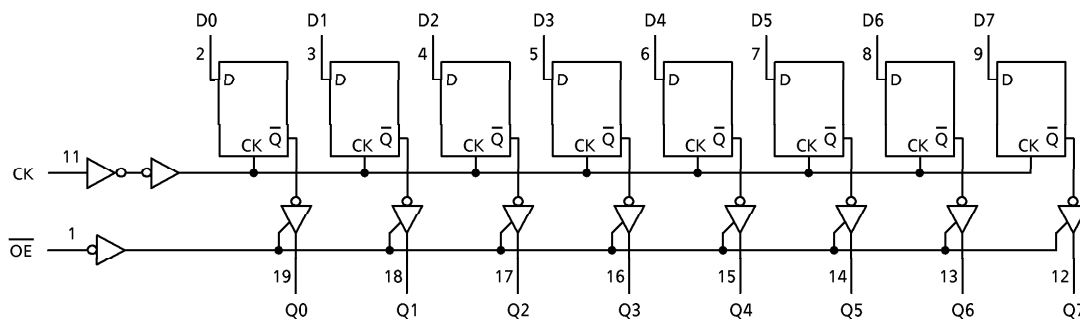


**Truth Table**

INPUTS			OUTPUTS
$\overline{OE}$	CK	D	
H	X	X	Z
L		X	Qn
L		L	L
L		H	H

- X : Don't Care
- Z : High Impedance
- Qn : No change

**System Diagram**



## Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~7.0	V
DC Output Voltage	$V_{OUT}$	-0.5~7.0 (Note 1)	V
		-0.5~ $V_{CC}$ + 0.5 (Note 2)	
Input Diode Current	$I_{IK}$	-50	mA
Output Diode Current	$I_{OK}$	±50 (Note 3)	mA
DC Output Current	$I_{OUT}$	±50	mA
Power Dissipation	$P_D$	180	mW
DC $V_{CC}$ /Ground Current	$I_{CC}/I_{GND}$	±100	mA
Storage Temperature	$T_{stg}$	-65~150	°C

(Note 1): Output in Off-State

(Note 2): High or Low State.  $I_{OUT}$  absolute maximum rating must be observed.

(Note 3):  $V_{OUT} < GND$ ,  $V_{OUT} > V_{CC}$

## Recommended Operating Conditions

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	$V_{CC}$	2.0~3.6	V
		1.5~3.6 (Note 4)	
Input Voltage	$V_{IN}$	0~5.5	V
Output Voltage	$V_{OUT}$	0~5.5 (Note 5)	V
		0~ $V_{CC}$ (Note 6)	
Output Current	$I_{OH}/I_{OL}$	±24 (Note 7)	mA
		±12 (Note 8)	
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise And Fall Time	$dt/dv$	0~10 (Note 9)	ns/V

(Note 4): Data Retention Only

(Note 5): Output in Off-State

(Note 6): High or Low State

(Note 7):  $V_{CC} = 3.0\sim 3.6$  V

(Note 8):  $V_{CC} = 2.7\sim 3.0$  V

(Note 9):  $V_{IN} = 0.8\sim 2.0$  V,  $V_{CC} = 3.0$  V

**Electrical Characteristics**

DC characteristics (Ta = -40~85°C)

PARAMETER		SYMBOL	TEST CONDITION		V <sub>CC</sub> (V)	Min	Max	UNIT
Input Voltage	"H" Level	V <sub>IH</sub>			2.7~3.6	2.0	—	V
	"L" Level	V <sub>IL</sub>			2.7~3.6	—	0.8	
Output Voltage	"H" Level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -100 μA	2.7~3.6	V <sub>CC</sub> - 0.2	—	V
				I <sub>OH</sub> = -12 mA	2.7	2.2	—	
				I <sub>OH</sub> = -18 mA	3.0	2.4	—	
				I <sub>OH</sub> = -24 mA	3.0	2.2	—	
	"L" Level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	2.7~3.6	—	0.2	
				I <sub>OL</sub> = 12 mA	2.7	—	0.4	
				I <sub>OL</sub> = 16 mA	3.0	—	0.4	
				I <sub>OL</sub> = 24 mA	3.0	—	0.55	
Input Leakage Current		I <sub>IN</sub>	V <sub>IN</sub> = 0~5.5 V		2.7~3.6	—	± 5.0	μA
3-State Output Off-State Current		I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = 0~5.5 V		2.7~3.6	—	± 5.0	μA
Power Off Leakage Current		I <sub>OFF</sub>	V <sub>IN</sub> / V <sub>OUT</sub> = 5.5 V		0	—	10.0	μA
Quiescent Supply Current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		2.7~3.6	—	10.0	μA
			V <sub>IN</sub> / V <sub>OUT</sub> = 3.6~5.5 V		2.7~3.6	—	± 10.0	
Increase In I <sub>CC</sub> Per Input		ΔI <sub>CC</sub>	V <sub>IH</sub> = V <sub>CC</sub> - 0.6 V		2.7~3.6	—	500	μA

AC characteristics (Ta = -40~85°C)

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	Min	Max	UNIT
Maximum Clock Frequency	f <sub>MAX</sub>	(Fig.1, 2)	2.7	—	—	MHz
			3.3 ± 0.3	150	—	
Propagation Delay Time (CK-Q)	t <sub>pLH</sub> t <sub>pHL</sub>	(Fig.1, 2)	2.7	—	9.5	ns
			3.3 ± 0.3	1.5	8.5	
Output Enable Time	t <sub>pZL</sub> t <sub>pZH</sub>	(Fig.1, 3)	2.7	—	9.5	ns
			3.3 ± 0.3	1.5	8.5	
Output Disable Time	t <sub>pLZ</sub> t <sub>pHZ</sub>	(Fig.1, 3)	2.7	—	7.0	ns
			3.3 ± 0.3	1.5	6.5	
Minimum Pulse Width (CK)	t <sub>w</sub> (H) t <sub>w</sub> (L)	(Fig.1, 2)	2.7	3.3	—	ns
			3.3 ± 0.3	3.3	—	
Minimum Set-Up Time	t <sub>s</sub>	(Fig.1, 2)	2.7	2.5	—	ns
			3.3 ± 0.3	2.5	—	
Minimum Hold Time	t <sub>h</sub>	(Fig.1, 2)	2.7	1.5	—	ns
			3.3 ± 0.3	1.5	—	
Output To Output Skew	t <sub>osLH</sub> t <sub>osHL</sub>	(Note 10)	2.7	—	—	ns
			3.3 ± 0.3	—	1.0	

(Note 10): Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

Dynamic Switching Characteristics (Ta = 25°C, Input t<sub>r</sub> = t<sub>f</sub> = 2.5 ns, C<sub>L</sub> = 50 pF, R<sub>L</sub> = 500 Ω)

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	Typ.	UNIT
Quiet Output Maximum Dynamic V <sub>OL</sub>	V <sub>OLP</sub>	V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V	3.3	0.8	V
Quiet Output Minimum Dynamic V <sub>OL</sub>	V <sub>OLV</sub>	V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V	3.3	0.8	V

Capacitive Characteristics (Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	Typ.	UNIT
Input Capacitance	C <sub>IN</sub>	—	3.3	7	pF
Output Capacitance	C <sub>OUT</sub>		3.3	8	pF
Power Dissipation Capacitance	C <sub>PD</sub>	f <sub>IN</sub> = 10 MHz (Note 11)	3.3	25	pF

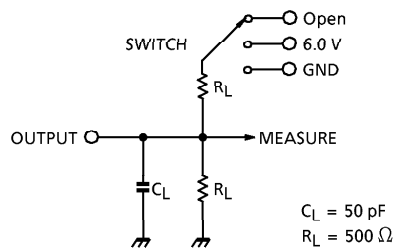
(Note 11): C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

Test Circuit

Fig.1



PARAMETER	SWITCH
$t_{pLH}$ , $t_{pHL}$	Open
$t_{pLZ}$ , $t_{pZL}$	6.0 V
$t_{pHZ}$ , $t_{pZH}$	GND
$t_w$ , $t_s$ , $t_h$ , $f_{MAX}$	Open

AC Waveform

Fig.2  $t_{pLH}$ ,  $t_{pHL}$ ,  $t_w$ ,  $t_s$ ,  $t_h$

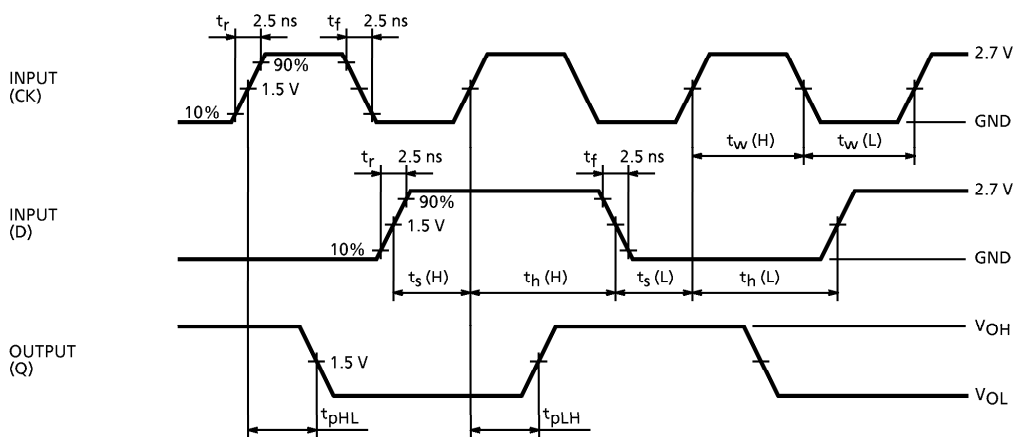
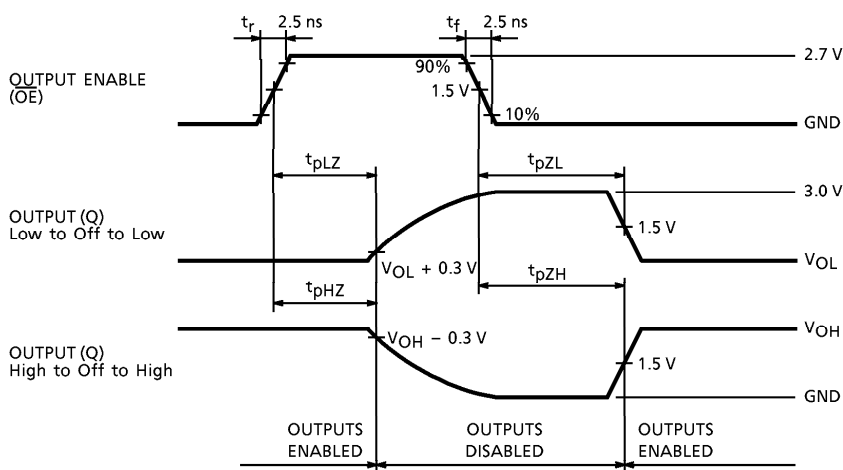
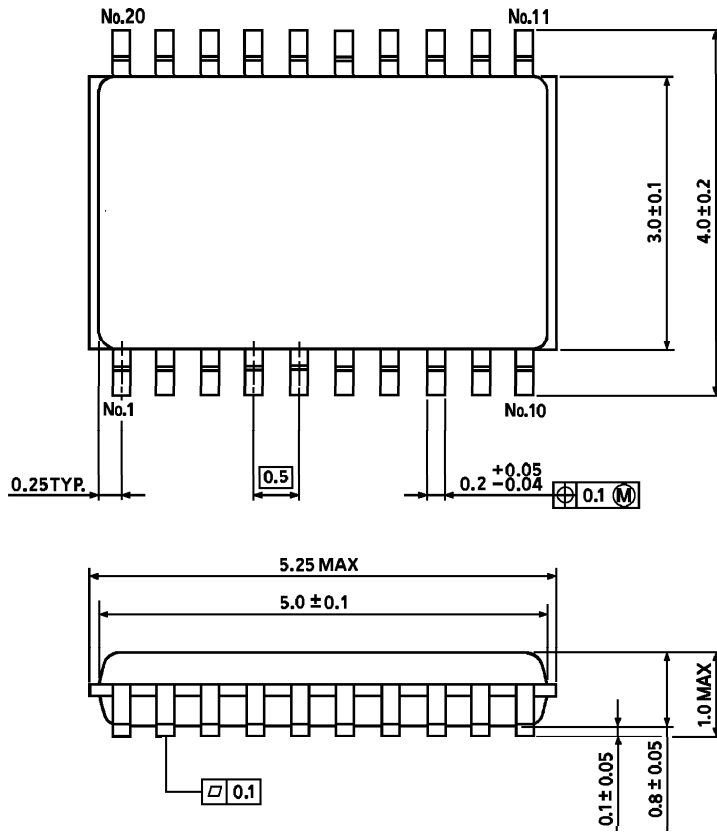


Fig.3  $t_{pLZ}$ ,  $t_{pHZ}$ ,  $t_{pZL}$ ,  $t_{pZH}$



**PACKAGE DIMENSIONS**  
VSSOP20-P-0030-0.50

Unit : mm



Weight : 0.03 g (typ.)