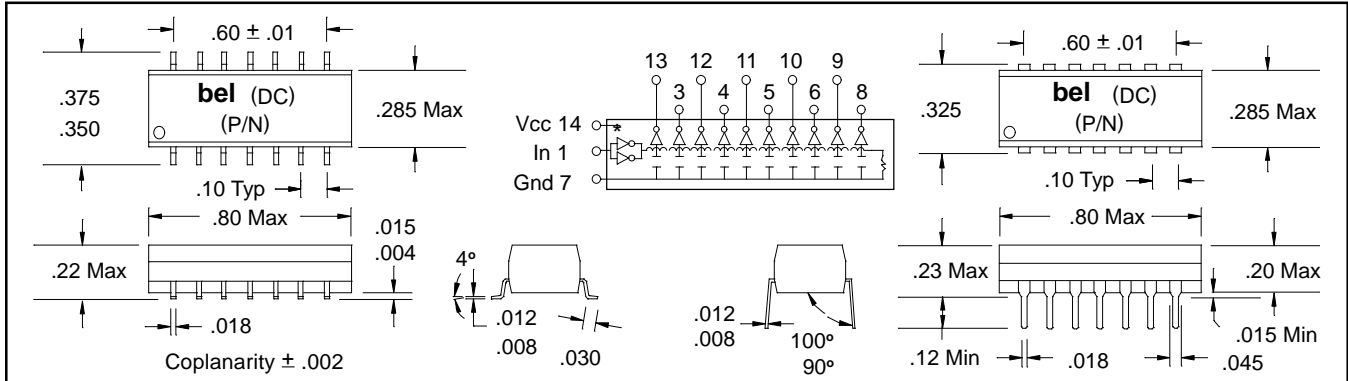


10 TAP LEADING EDGE CONTROL LOW VOLTAGE DELAY MODULES

Cat 31-R1



Part Numbers

| SMD | Thru-Hole | Total Delay | Delay per Tap | Rise Time |
|--------------|--------------|-------------|---------------|-----------|
| S477-0025-10 | A477-0025-10 | * 22.5 ns | 2.5 ns | 3 ns |
| S477-0030-10 | A477-0030-10 | * 27 ns | 3 ns | 3 ns |
| S477-0040-10 | A477-0040-10 | * 36 ns | 4 ns | 3 ns |
| S477-0050-10 | A477-0050-10 | 50 ns | 5 ns | 3 ns |
| S477-0060-10 | A477-0060-10 | 60 ns | 6 ns | 3 ns |
| S477-0070-10 | A477-0070-10 | 70 ns | 7 ns | 3 ns |
| S477-0080-10 | A477-0080-10 | 80 ns | 8 ns | 3 ns |
| S477-0090-10 | A477-0090-10 | 90 ns | 9 ns | 3 ns |
| S477-0100-10 | A477-0100-10 | 100 ns | 10 ns | 3 ns |
| S477-0125-10 | A477-0125-10 | 125 ns | 12.5 ns | 3 ns |
| S477-0150-10 | A477-0150-10 | 150 ns | 15 ns | 3 ns |
| S477-0200-10 | A477-0200-10 | 200 ns | 20 ns | 3 ns |
| S477-0250-10 | A477-0250-10 | 250 ns | 25 ns | 3 ns |

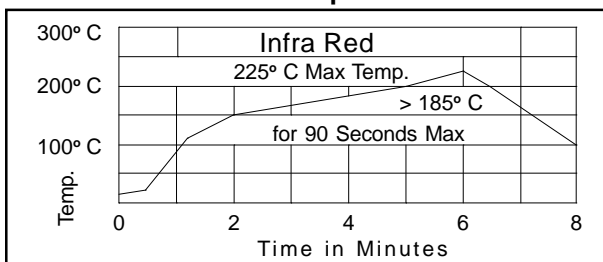
Tolerances

Input to Taps ± 2 ns or 5% , Whichever is Greater
 Tap to Tap ± 2 ns or 7%, Whichever is Greater
 Delays measured @ 50% levels on Leading Edge only
 with no loads on Taps
 Rise and Fall Times measured from 10% to 90% levels
 * Ref. Delay from P13, Delay P1-P13 = 5.5 ns typical

Drive Capabilities

| | | | |
|----|----------------|---|---------------------|
| Nh | Logic 1 Fanout | - | 10 LSTTL Loads Max. |
| Nl | Logic 0 Fanout | - | 10 LSTTL Loads Max. |

Recommended Temperature Profile



Test Conditions @ 25°C

| | | |
|------|----------------|-------------------|
| Ein | Pulse Voltage | 3.0 Volts |
| Trin | Rise Time | 3.0 ns (10%-90%) |
| PW | Pulse Width | 1.2 x Total Delay |
| PP | Pulse Period | 4 x Pulse Width |
| Iccl | Supply Current | 30 ma Typical |
| Vcc | Supply Voltage | 3.3 Volts |

Electrical Characteristics

| | Min. | Max. | Units | |
|------|---------------------------------------|-------------------------|-------|----|
| Vcc | Supply Voltage | 3.0 | 3.6 | V |
| Vih | Logic 1 Input Voltage | 2.4 | | V |
| Vil | Logic 0 Input Voltage | | 0.8 | V |
| Iik | Input Clamp Current | | -20 | ma |
| Ioh | Logic 1 Output Current | | 20 | ma |
| Iol | Logic 0 Output Current | | -20 | ma |
| Voh | Logic 1 Output Voltage | 2.9 | | V |
| Vol | Logic 0 Output voltage | | 0.1 | V |
| Vik | Input Clamp Voltage | | -0.5 | V |
| Iih | Logic 1 Input Current | | 2 | ua |
| Iil | Logic 0 Input Current | | -2 | ua |
| Icch | Logic 1 Supply Current | | 10 | ma |
| Iccl | Logic 0 Supply Current | | 40 | ma |
| Ta | Operating Free Air Temperature | 0° | 70° | C |
| PW | Min. Input Pulse Width of Total Delay | 40 | | % |
| d | Maximum Duty Cycle | | 50 | % |
| Tc | Temp. Coeff. of Total Delay (TD) | 100 + (25000/TD) PPM/°C | | |

Notes

Transfer molded for better reliability
 Compatible with TTL & CMOS circuits
 Terminals: Electro-Tin plate phosphor bronze
 Performance warranty is limited to specified parameters listed
 SMD - Tape & Reel available:
 32mm Wide x 16mm Pitch, 500 pieces per 13" reel

Other Delays and Tolerances Available Consult Sales

Specifications subject to change without notice.

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