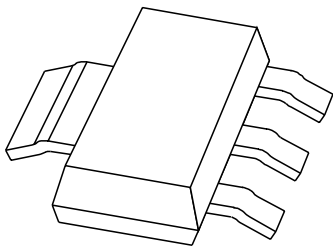


DATA SHEET



PZTA64 PNP Darlington transistor

Product specification
Supersedes data of September 1994
File under Discrete Semiconductors, SC04

1997 Jun 20

PNP Darlington transistor

PZTA64

FEATURES

- High current (max. 500 mA)
- Low voltage (max. 30 V).

APPLICATIONS

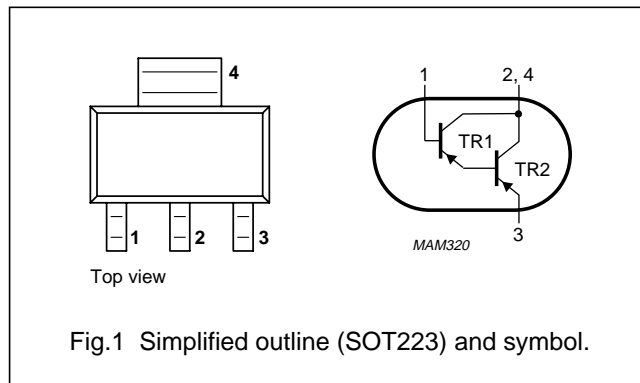
- Preamplifiers requiring high input impedance.

DESCRIPTION

PNP Darlington transistor in a SOT223 plastic package.
NPN complement: PZTA14.

PINNING

PIN	DESCRIPTION
1	base
2, 4	collector
3	emitter



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–30	V
V_{CES}	collector-emitter voltage	$V_{BE} = 0$	–	–30	V
I_C	collector current (DC)		–	–500	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}$	–	1.25	W
h_{FE}	DC current gain	$I_C = -10\text{ mA}; V_{CE} = -5\text{ V}$	10000	–	
f_T	transition frequency	$I_C = -10\text{ mA}; V_{CE} = -5\text{ V}; f = 100\text{ MHz}$	125	–	MHz

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	–	–30	V
V _{CES}	collector-emitter voltage	V _{BE} = 0	–	–30	V
V _{EBO}	emitter-base voltage	open collector	–	–10	V
I _C	collector current (DC)		–	–500	mA
I _{CM}	peak collector current		–	–800	mA
I _B	base current (DC)		–	–200	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	–	1.25	W
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C

Note

- Device mounted on a printed-circuit board, single-sided copper, tinplated, mounting pad for collector 1 cm².
For other mounting conditions, see *“Thermal considerations for SOT223 in the General part of handbook SC04”*.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient	note 1	100	K/W
R _{th j-s}	thermal resistance from junction to soldering point		19	K/W

Note

- Device mounted on a printed-circuit board, single-sided copper, tinplated, mounting pad for collector 1 cm².
For other mounting conditions, see *“Thermal considerations for SOT223 in the General part of handbook SC04”*.

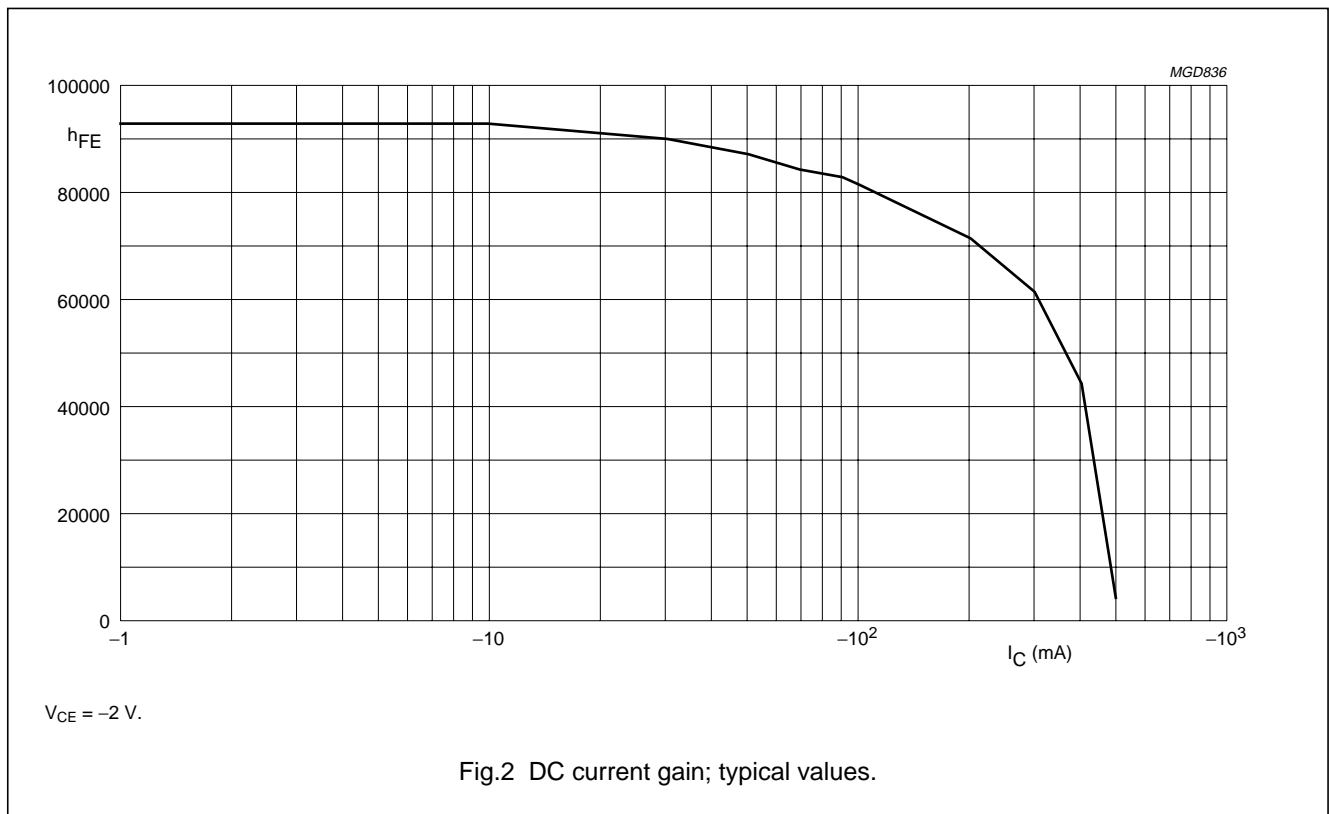
PNP Darlington transistor

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CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0; V_{CB} = -30\text{ V}$	–	–100	nA
I_{CES}	collector cut-off current	$V_{BE} = 0; V_{CE} = -30\text{ V}$	–	–100	nA
I_{EBO}	emitter cut-off current	$I_C = 0; V_{EB} = -10\text{ V}$	–	–100	nA
h_{FE}	DC current gain	$V_{CE} = -5\text{ V}$; see Fig.2 $I_C = -10\text{ mA}$ $I_C = -100\text{ mA}$	10000 20000	– –	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -100\text{ mA}; I_B = -0.1\text{ mA}$	–	–1.5	V
V_{BEon}	base-emitter voltage	$I_C = -100\text{ mA}; V_{CE} = -5\text{ V}$	–	–2	V
f_T	transition frequency	$I_C = -10\text{ mA}; V_{CE} = -5\text{ V}; f = 100\text{ MHz}$	125	–	MHz



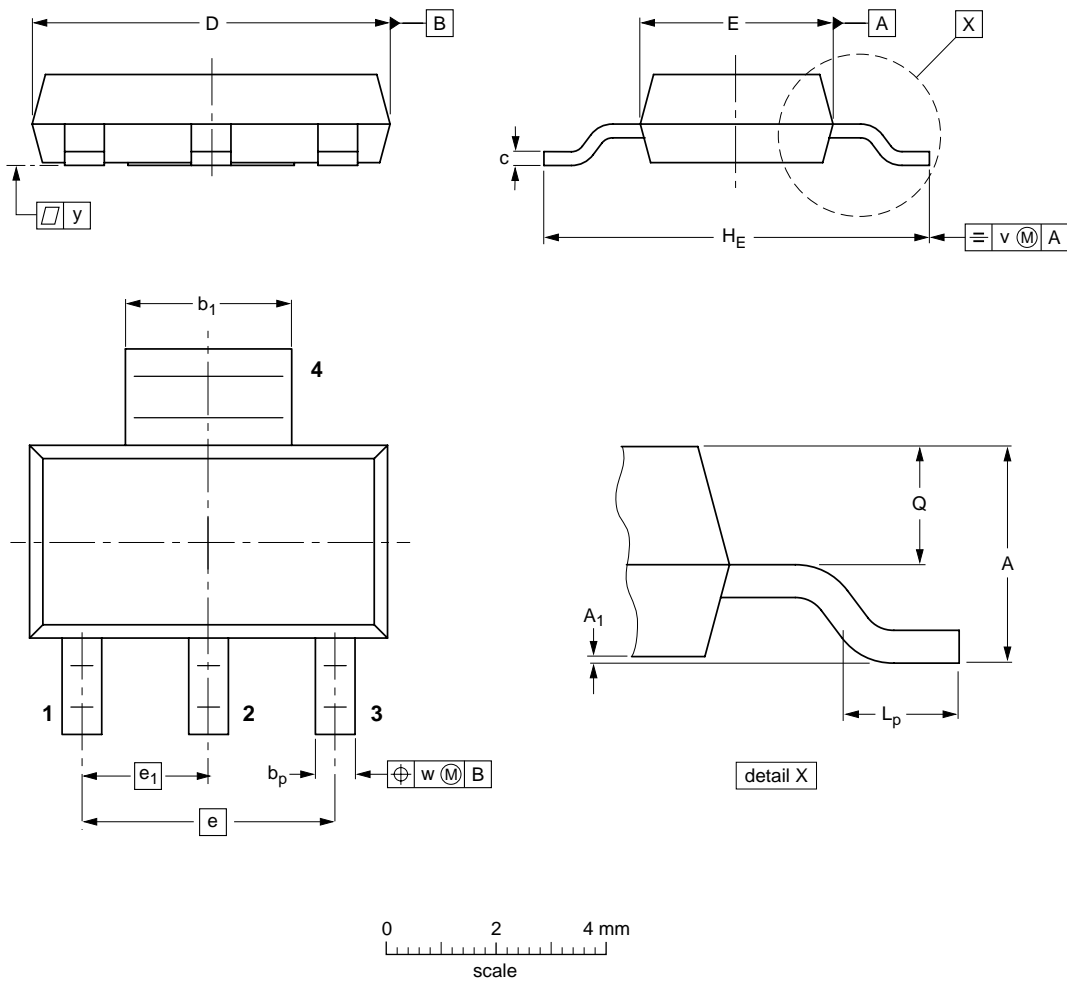
PNP Darlington transistor

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PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223						96-11-11 97-02-28

PNP Darlington transistor

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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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PNP Darlington transistor

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