

PMWD18UN

Dual N-channel μ TrenchMOS™ ultra low level FET

Rev. 02 — 23 February 2004

Product data

1. Product profile

1.1 Description

Dual common drain N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Surface mounted package
- Very low threshold
- Low profile
- Fast switching.

1.3 Applications

- Portable appliances
- Battery management
- PCMCIA cards
- Load switching.

1.4 Quick reference data

- $V_{DS} \leq 30$ V
- $P_{tot} \leq 2.3$ W
- $I_D \leq 7.8$ A
- $R_{DSon} \leq 21.5$ m Ω .

2. Pinning information

Table 1: Pinning - SOT530-1 (TSSOP8), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,8	drain (d)	<p>Top view MBK885</p>	<p>mb1600</p>
2,3	source1 (s1)		
4	gate1 (g1)		
5	gate2 (g2)		
6,7	source2 (s2)		

SOT530-1 (TSSOP8)



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3. Ordering information

Table 2: Ordering information

Type number	Package		Version
	Name	Description	
PMWD18UN	TSSOP8	Plastic thin shrink small outline package; 8 leads	SOT530-1

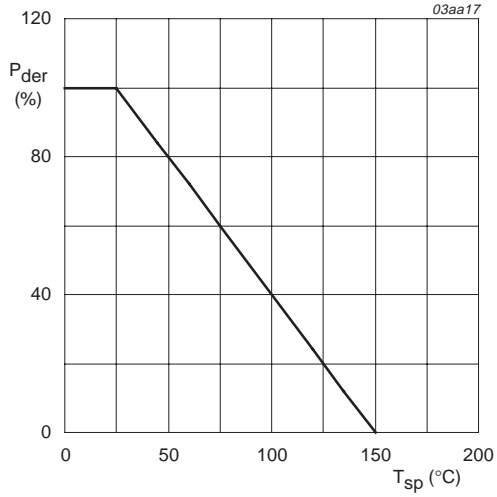
4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

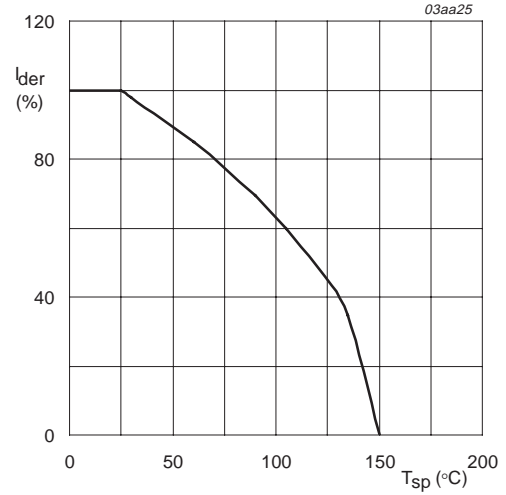
Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V	
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V	
V_{GS}	gate-source voltage		-	± 12	V	
I_D	drain current (DC)	$T_{sp} = 25\text{ °C}$; $V_{GS} = 4.5\text{ V}$; Figure 2 and 3	[1]	-	7.8	A
		$T_{sp} = 100\text{ °C}$; $V_{GS} = 4.5\text{ V}$; Figure 2	[1]	-	5	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	[1]	-	32	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; Figure 1	[1]	-	2.3	W
T_{stg}	storage temperature		-55	+150	°C	
T_j	junction temperature		-55	+150	°C	
Source-drain diode						
I_S	source (diode forward) current (DC)	$T_{sp} = 25\text{ °C}$	[1]	-	1.9	A
I_{SM}	peak source (diode forward) current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	[1]	-	7.6	A

[1] Single device conducting



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

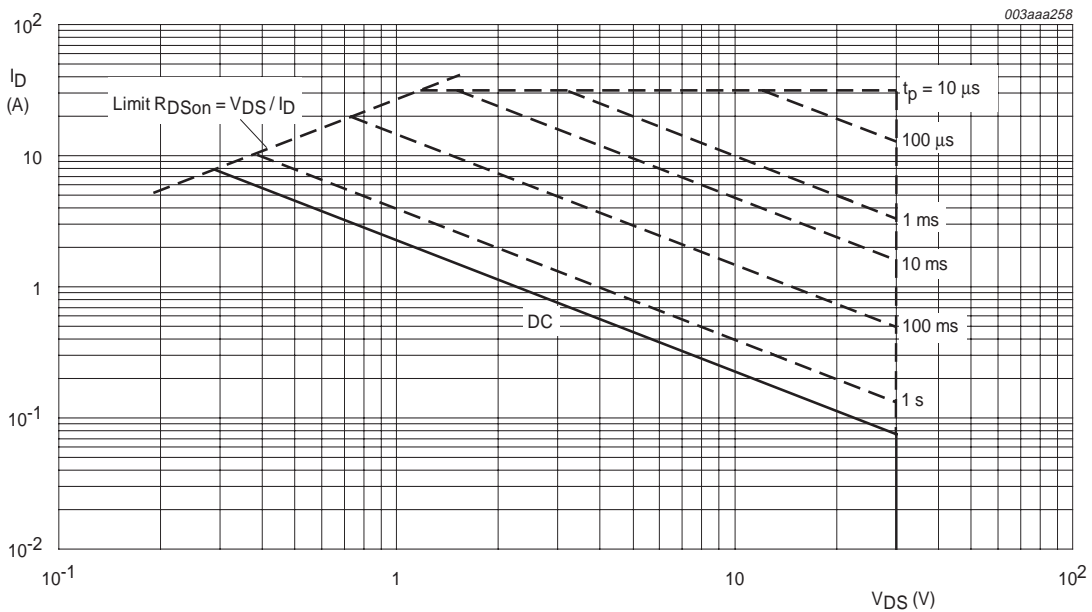
Fig 1. Normalized total power dissipation as a function of solder point temperature.



V_{GS} ≥ 4.5 V

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



T_{sp} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	55	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint	-	100	-	K/W

5.1 Transient thermal impedance

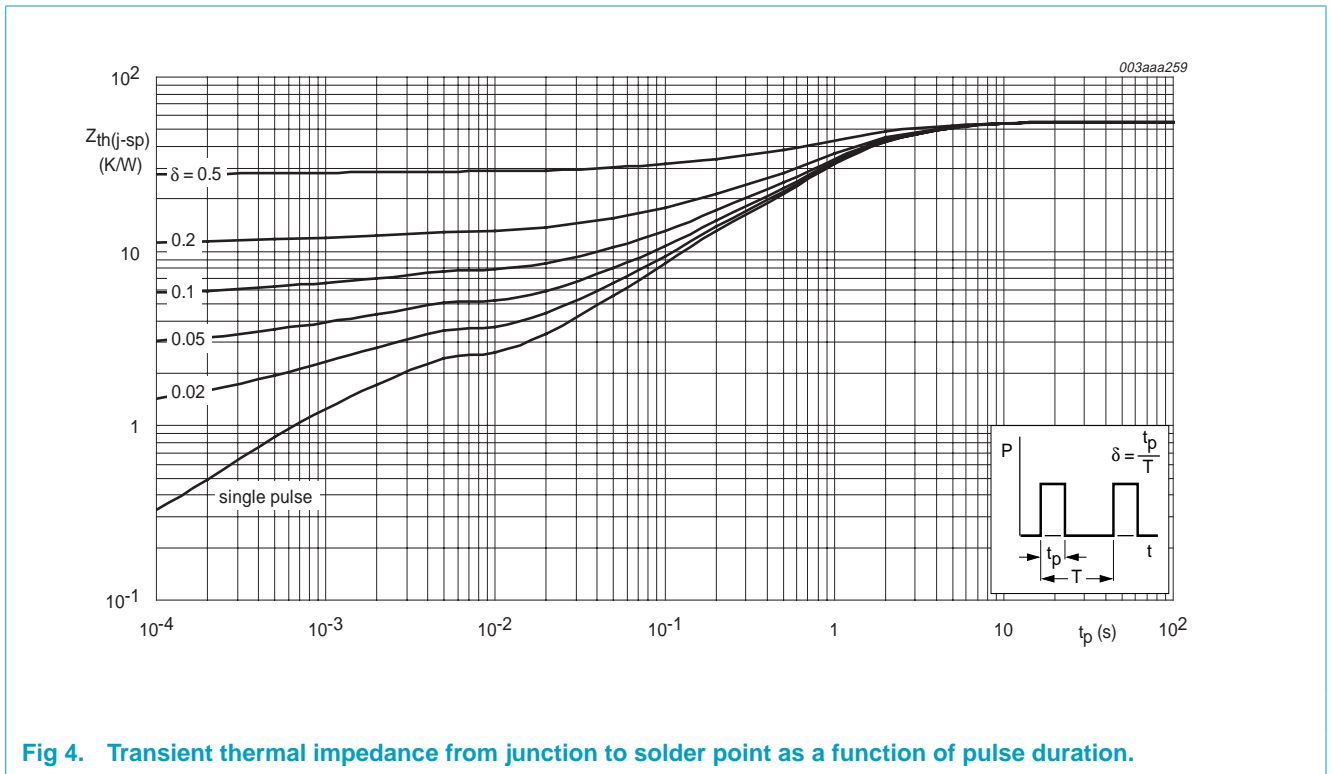


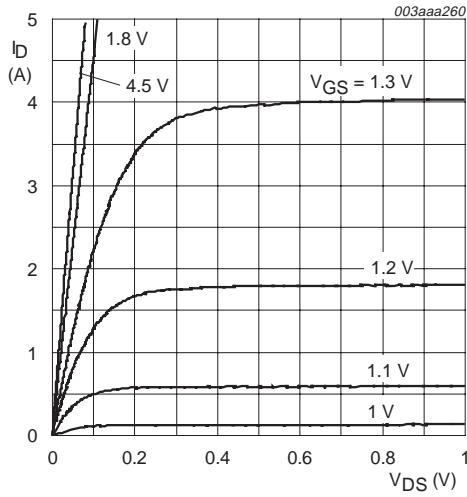
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.

6. Characteristics

Table 5: Characteristics

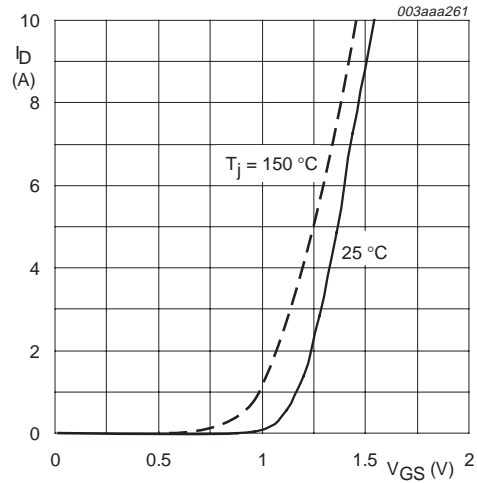
$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$ $T_j = 25\text{ }^\circ\text{C}$	30	-	-	V
		$T_j = -55\text{ }^\circ\text{C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; Figure 9	0.45	0.7	-	V
I_{DSS}	drain-source leakage current	$V_{DS} = 30\text{ V}$; $V_{GS} = 0\text{ V}$ $T_j = 25\text{ }^\circ\text{C}$	-	-	1	μA
		$T_j = 150\text{ }^\circ\text{C}$	-	-	100	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 10\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$; $I_D = 5\text{ A}$; Figure 7 and 8 $T_j = 25\text{ }^\circ\text{C}$	-	18	21.5	m Ω
		$T_j = 150\text{ }^\circ\text{C}$	-	31	37	m Ω
		$V_{GS} = 1.8\text{ V}$; $I_D = 4.5\text{ A}$; Figure 7 and 8	-	24	35	m Ω
		$V_{GS} = 2.5\text{ V}$; $I_D = 5\text{ A}$; Figure 7 and 8	-	20	23.5	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = 4\text{ A}$; $V_{DD} = 16\text{ V}$; $V_{GS} = 4.5\text{ V}$; Figure 13	-	24.7	-	nC
Q_{gs}	gate-source charge		-	2.2	-	nC
Q_{gd}	gate-drain (Miller) charge		-	6.4	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 16\text{ V}$; $f = 1\text{ MHz}$; Figure 11	-	1526	-	pF
C_{oss}	output capacitance		-	210	-	pF
C_{rss}	reverse transfer capacitance		-	160	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 10\text{ V}$; $I_D = 1\text{ A}$; $V_{GS} = 4.5\text{ V}$; $R_G = 6\text{ }\Omega$	-	15	-	ns
t_r	rise time		-	21	-	ns
$t_{d(off)}$	turn-off delay time		-	57	-	ns
t_f	fall time		-	26	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 5\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 12	-	0.87	1.2	V
t_{rr}	reverse recovery time	$I_S = 5\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_R = 30\text{ V}$; $V_{GS} = 0\text{ V}$	-	55	-	ns
Q_r	recovered charge		-	21	-	nC



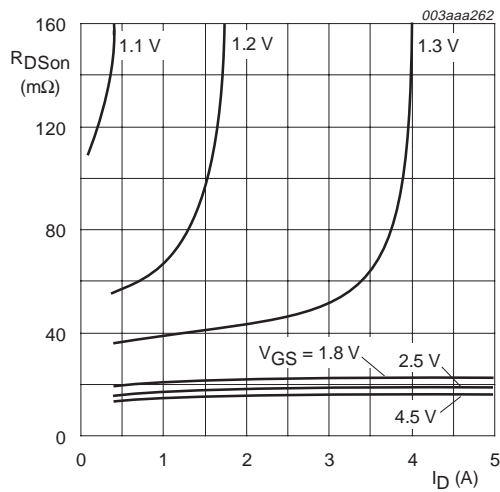
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



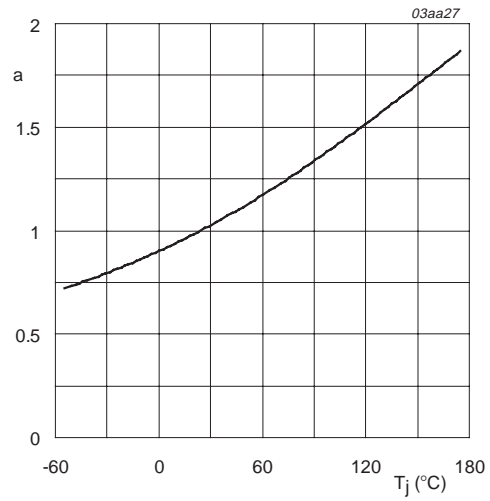
$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{DS} \geq I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



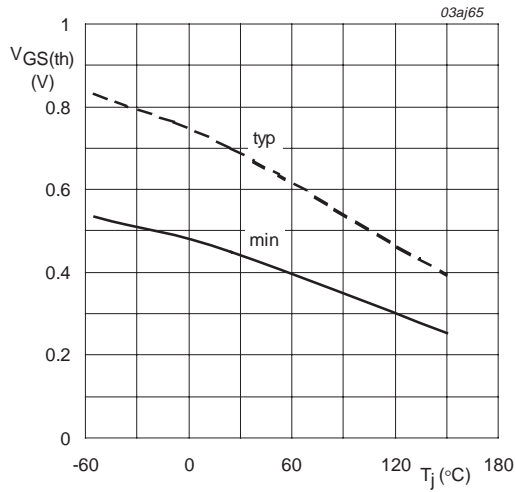
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



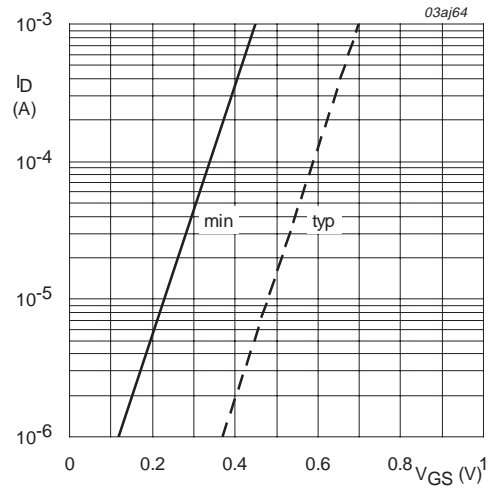
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain source on-state resistance factor as a function of junction temperature.



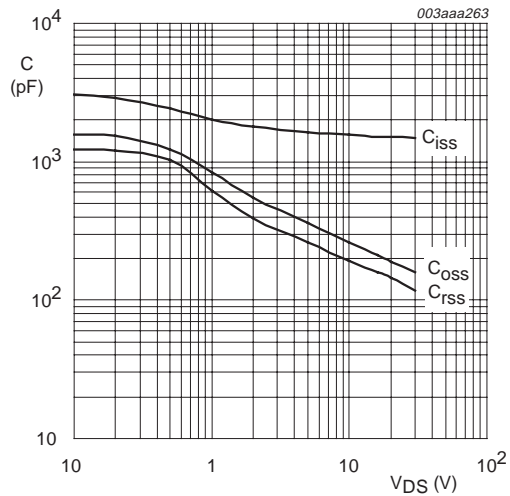
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



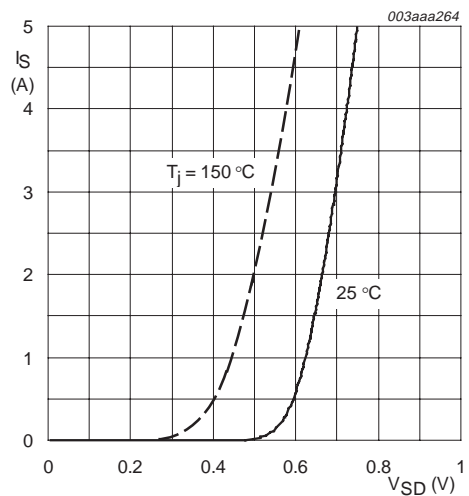
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



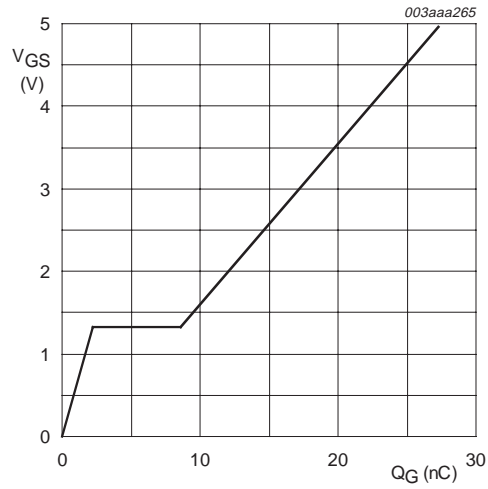
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25 \text{ }^{\circ}C \text{ and } 150 \text{ }^{\circ}C; V_{GS} = 0 \text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 4 \text{ A}; V_{DD} = 16 \text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 4.4 mm

SOT530-1

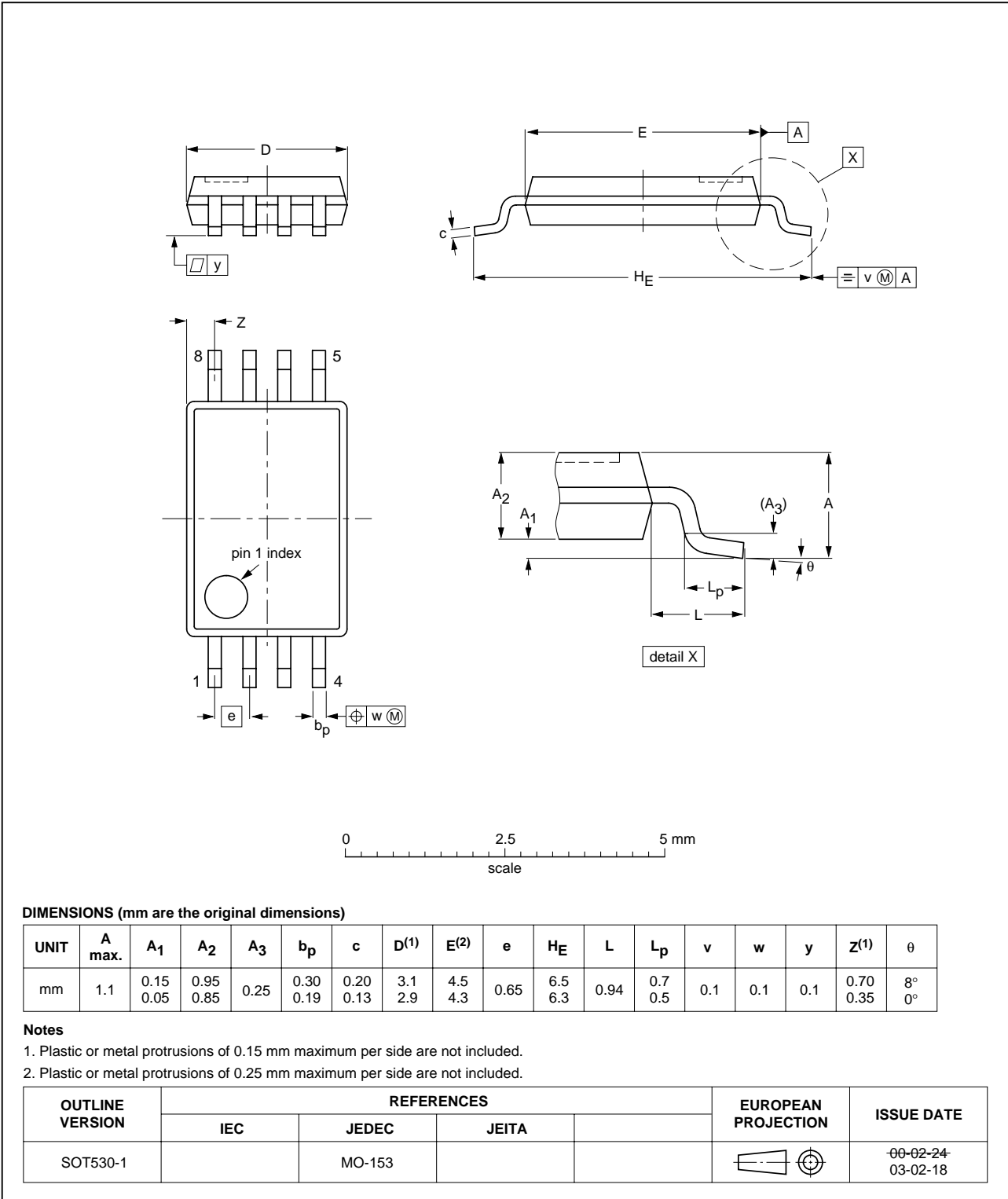


Fig 14. SOT530-1 (TSSOP8).

8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
02	20040223	-	Product data (9397 750 12706) Modifications: <ul style="list-style-type: none">• Correction to I_D data in Section 1.4 “Quick reference data”• Correction to P_{tot}, I_D, I_{DM}, I_S and I_{SM} data in Table 3 “Limiting values”• Correction to $R_{th(j-sp)}$ data in Table 4 “Thermal characteristics”• Figure 3 and Figure 4 updated.• Section 3 “Ordering information” added
01	20030204	-	Product data (9397 750 10832)

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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