PD63000

PoE Microcontroller Unit

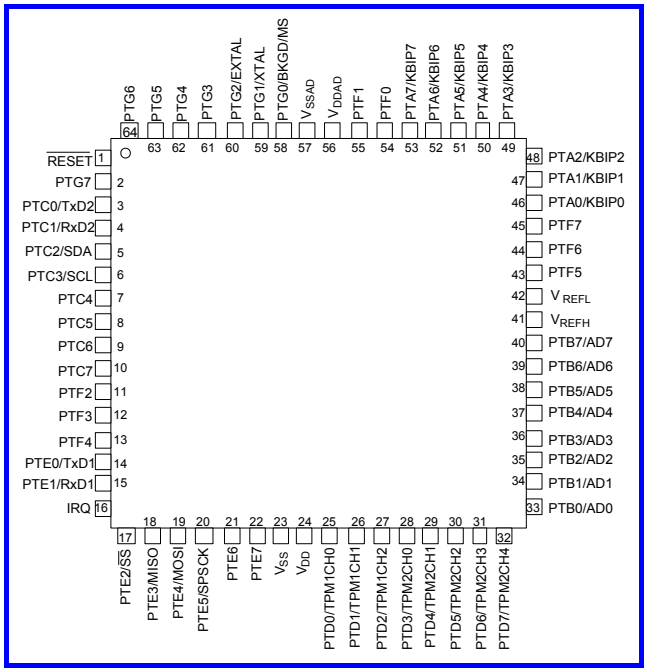
Description

PowerDsine's™ Microcontroller Unit, PD63000, is a member of Motorola's HCS08 Family of 8-bit microcontroller units (MCUs). This MCU uses the enhanced HCS08 core and is pre-programmed with a special proprietary application. It is used in conjunction with PowerDsine's PD64012 PoE Manager in Ethernet switches and Midspans to allow next generation network devices to share power and data over the same cable, according to IEEE 802.3af. When used in conjunction with the PD63000, the PD64012 operates in Enhanced mode.

The MCU features a 1 Mb/s SPI to each of the PoE Managers and a communication interface with the host CPU via UART or I^2C protocol. The I/O lines, the SPI bus and the control signals are loaded by 50-ohm serial resistors. The MCU runs at about 10 MHz, providing a 1 MHz clock frequency to the SPI bus. An external resonator is used for clock generation.

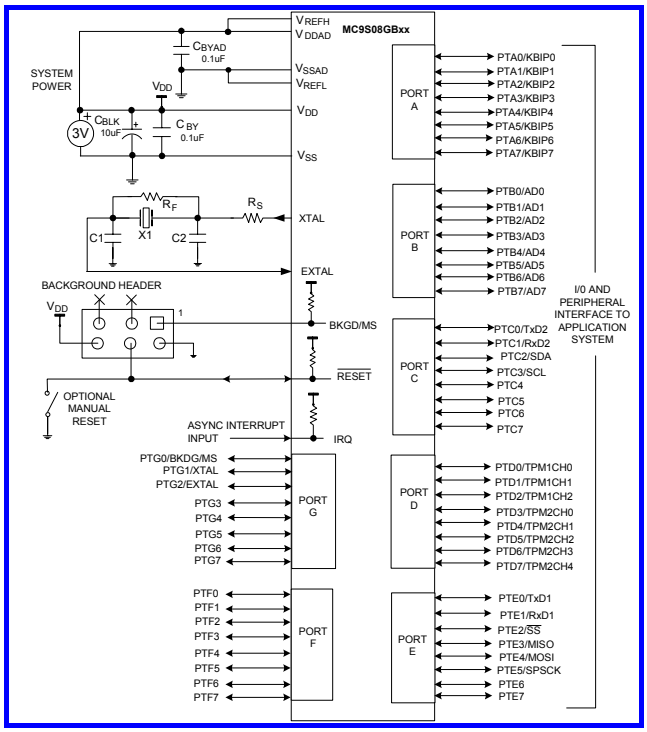
The device is a Motorola's MC9S08GB60CFU microprocessor control unit – this is an 8-bit device composed of standard on-chip peripherals including: an 8-bit CPU, a 60-kbyte flash EEPROM, a 4-kbyte RAM, an asynchronous serial communications interface, a serial peripheral interface, a 3-channel timer and a 5-channel timer. In addition this chip includes: an 10-bit analog-to-digital converter.

Pin Configuration



System Connectivity

In order to properly relate to the MCU in this document, a diagram of basic system connectivity is presented, hereafter. The various port groups are depicted along with their respective port lines. This block diagram can be compared with the application schematics from PowerDsine's Application Notes and Data Sheets, so as to understand the circuits used.



Program Burn-in

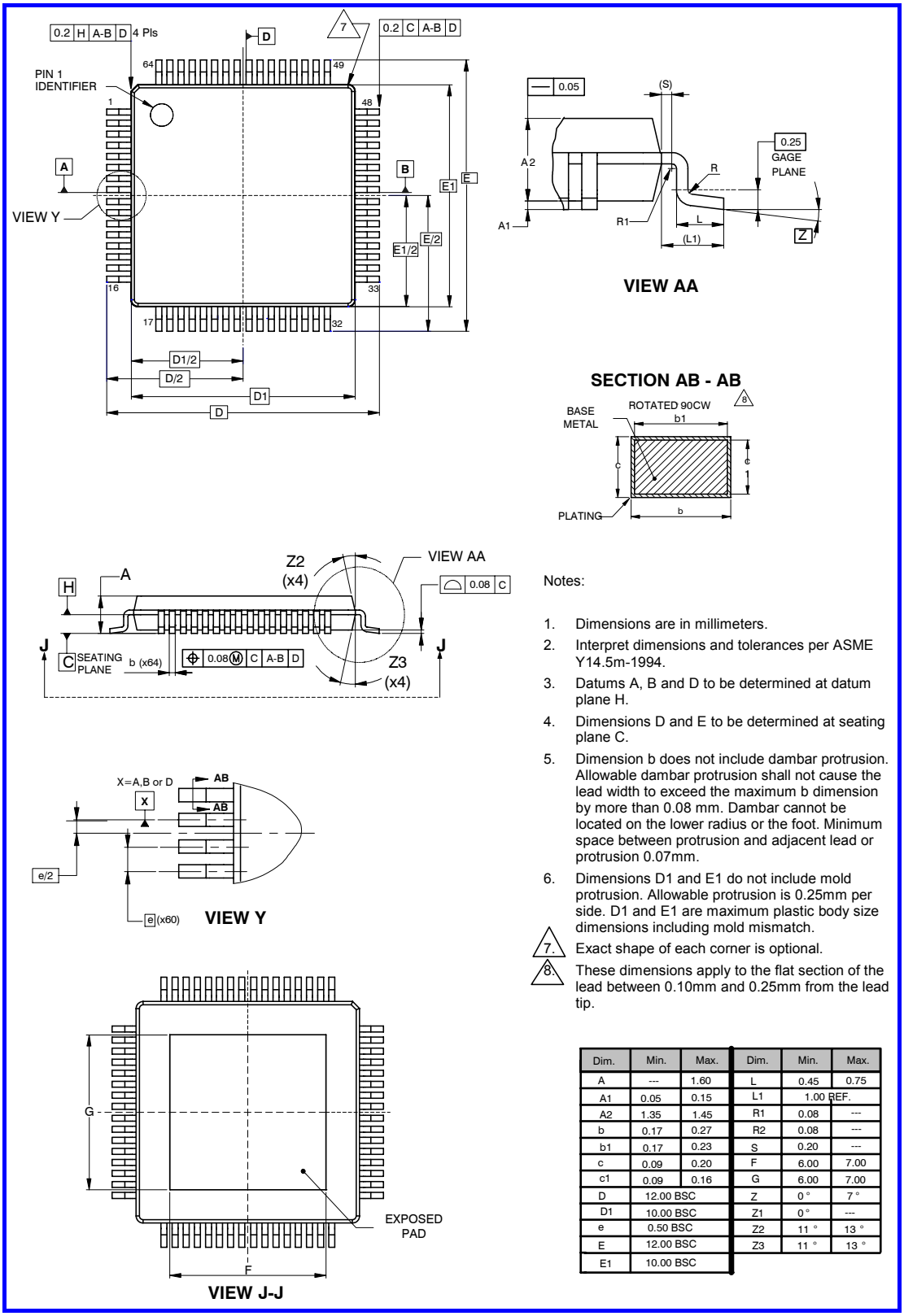
Initial burn-in is accomplished via the background header (BDM), by PowerDsine. Thereafter the MCU is downloaded with a special Powerdsine program referred to as the PD64012 Enhanced Mode Software. This software can be downloaded via the UART port (pins 14 & 15, PTE0/TxD1 & PTE1/RxD1) or via the I^2C port (pins 5 & 6, SDA & SCL.).

Applicable Documents

- IEEE 802.3af-2003 standard, DTE Power via MDI
- PowerDsine PD64012 Data Sheet, Cat. No. 06-0003-058
- Serial Communication Protocol, Cat. No. 06-0032-056
- PowerDsine Application Note 129 for Designing a 48-port Enhanced PoE System
- MC9S08GB/GT Data sheet (V1.5) 8-/16-Bit Products Division, Motorola, Inc.
  Obtain from: http://e-www.motorola.com/files/microcontrollers/doc/data_sheet/MC9S08GB60.pdf

Package Information

The PD63000 is housed in a 64-pin LQFP plastic package, 10 x 10 x 1.4 mm, meeting JEDEC's MS-026 package outline and dimensions.



Notes:

1. Dimensions are in millimeters.
2. Interpret dimensions and tolerances per ASME Y14.5m-1994.
3. Datums A, B and D to be determined at datum plane H.
4. Dimensions D and E to be determined at seating plane C.
5. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and adjacent lead or protrusion 0.07mm.
6. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
7. Exact shape of each corner is optional.
8. These dimensions apply to the flat section of the lead between 0.10mm and 0.25mm from the lead tip.

Dim.	Min.	Max.	Dim.	Min.	Max.
A	---	1.60	L	0.45	0.75
A1	0.05	0.15	L1	1.00 REF.	
A2	1.35	1.45	R1	0.08	---
b	0.17	0.27	R2	0.08	---
b1	0.17	0.23	S	0.20	---
c	0.09	0.20	F	6.00	7.00
c1	0.09	0.16	G	6.00	7.00
D	12.00 BSC		Z	0 °	7 °
D1	10.00 BSC		Z1	0 °	---
e	0.50 BSC		Z2	11 °	13 °
E	12.00 BSC		Z3	11 °	13 °
E1	10.00 BSC				

Pin Functionality

PIN	PIN NAME	PIN TYPE	PIN DESCRIPTION
1.	Reset	Digital input	xRESET_IN **(1)**
2.	PTG7		
3.	PTC0/TxD2	Digital I/O	
4.	PTC1/RxD2	Digital I/O	
5.	PTC2/SDA	Digital I/O	SDA
6.	PTC3/SCL	Digital I/O	SCL
7.	PTC4	Digital I/O	
8.	PTC5	Digital I/O	
9.	PTC6	Digital I/O	
10	PTC7	Digital I/O	
11	PTF2		
12	PTF3		
13	PTF4		
14	PTE0/TxD1	Digital I/O	TX_3_3_V
15	PTE1/RxD1	Digital I/O	RX_3_3_V
16	IRQ	Digital input	xInt_in
17	PTE2/SS	Digital I/O	
18	PTE3/MISO	Digital I/O	MISO
19	PTE4/MOSI	Digital I/O	MOSI
20	PTE5/SPSCK	Digital I/O	SCK
21	PTE6	Digital I/O	xDISABLE_PORTS
22	PTE7	Digital I/O	
23	VSS	Digital	D (ground)
24	VDD	Digital	3_3VCPU
25	PTD0/TPM1		Shorted to pin 28
26	PTD1/TPM1		
27	PTD2/TPM1		
28	PTD3/TPM2		Shorted to pin 25
29	PTD4/TPM2	Digital I/O	xSPI_CS0
30	PTD5/TPM2	Digital I/O	xSPI_CS1
31	PTD6/TPM2	Digital I/O	xSPI_CS2
32	PTD7/TPM2	Digital I/O	xSPI_CS3
33	PTB0/AD0	A/D input	

PIN	PIN NAME	PIN TYPE	PIN DESCRIPTION
34	PTB1/AD1	A/D input	HW VER
35	PTB2/AD2	A/D input	
36	PTB3/AD3	A/D input	I2C_Init_E
37	PTB4/AD4	A/D input	GND_Analog_CPU
38	PTB5/AD5	A/D input	
39	PTB6/AD6	A/D input	
40	PTB7/AD7	A/D input	
41	VREFH	A/D ref.	VREFH
42	VREFL	A/D ref.	GND_Analog_CPU
43	PTF5		
44	PTF6		
45	PTF7		
46	PTA0/KBIP0	Digital I/O	xASIC_RESET **(1)**
47	PTA1/KBIP1	Digital I/O	xDISABLE_PORTS_TO_ASIC **(1)**
48	PTA2/KBIP2	A/D input	Power Good PG3 **(2)**
49	PTA3/KBIP3	A/D input	Power Good PG2 **(2)**
50	PTA4/KBIP4	A/D input	Power Good PG1 **(2)**
51	PTA5/KBIP5	A/D input	
52	PTA6/KBIP6		
53	PTA7/KBIP7		
54	PTF0		
55	PTF1		
56	VDDAD	Analog	VDDAD
57	VSSAD	Analog	GND_Analog_CPU
58	PTG0/BKGD/	Digital I/O	
59	PTG1/XTAL	Resonator/o	XTAL
60	PTG2/EXTAL	Resonator/o	EXTAL
61	PTG3	Digital I/O	
62	PTG4	Digital I/O	
63	PTG5	Digital output	xInt_Out (future use)
64	PTG6	Digital I/O	SELF RESET

(1). Upon receiving an active low reset level via pin 1 (xRESET_IN) from the switch host, the PD63000 MCU immediately disables all PoE Manager (PD64012) output ports. The MCU does this using the xDISABLE_PORTS_TO_ASIC signal (pin 47). During this process, the PoE Managers are still actively operational, although their ports are disabled. Once the active low is released, the MCU performs a software reboot. After the reboot, the MCU sends a reset to all PoE Managers, via pin 46 (xASIC_RESET).

(2) Refer to Tech Note TN-113 for information on power management.

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Revision History

Revision Level / Date	Para. Affected	Description
1.2 / 9 Feb. 04	Front & back pages	Added policy statement and replaced Cat. no.
1.3 / 12 Feb. 04	Pin Functionality (page 3)	Added pin descriptions and explanation related to reset.
1.4 / 10 Mar. 04	Pin Functionality (page 3)	Added definitions for power management pins (Power Good)