10 AMP, 75 VOLT MOSFET SMART POWER 3-PHASE MOTOR DRIVE HYBRID

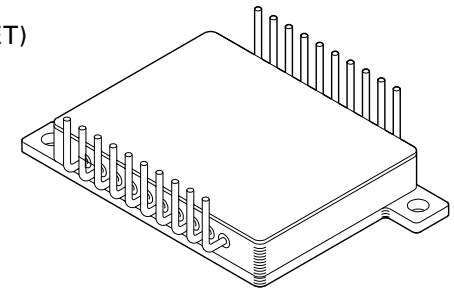
4303

M.S.KENNEDY CORP.
4707 Dey Road Liverpool, N.Y. 13088
(315) 701-6751

MIL-PRF-38534 CERTIFIED

FEATURES:

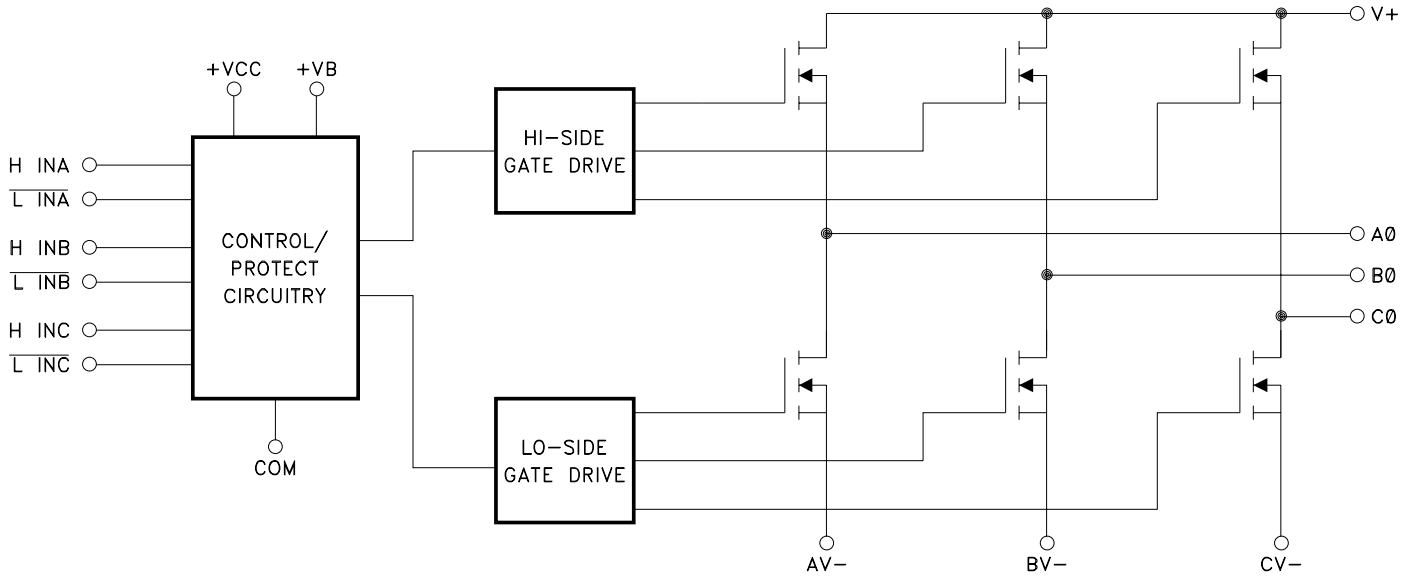
- 75V, 10 Amp Capability
- Ultra Low Thermal Resistance - Junction to Case - 1.5°C/W (Each MOSFET)
- Self-Contained, Smart Lowside/Highside Drive Circuitry
- Bootstrap High-Side Supplies
- Under-Voltage Lockout
- Capable of Switching Frequencies to 25KHz
- Isolated Case Allows Direct Heat Sinking
- Bolt-down Design Allows Superior Heat Dissipation



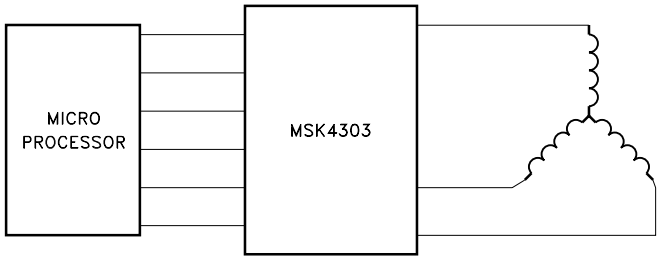
DESCRIPTION:

The MSK 4303 is a 10 Amp, 3 Phase Bridge Smart Power Motor Drive Hybrid with a 75 volt rating on the output switches. The output switches are MOSFETs. This new smart power motor drive hybrid is 5.0 volt input logic compatible. Under-voltage lockout shuts down the bridge when the supply voltage gets to a point of incomplete turn-on of the output switches. The internal high-side bootstrap power supply derived from the +VB supply completely eliminates the need for 3 floating independent power supplies.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS



3 PHASE SIX STEP DC BRUSHLESS MOTOR DRIVE OR 3 PHASE SINUSOIDAL INDUCTION MOTOR DRIVE

PIN-OUT INFORMATION

1	H INA	20	V+
2	L INA	19	N/C
3	+VCC	18	AV-
4	H INB	17	AØ
5	L INB	16	N/C
6	COM	15	BV-
7	COM	14	BØ
8	+VB	13	N/C
9	H INC	12	CV-
10	L INC	11	CØ

ABSOLUTE MAXIMUM RATINGS ⑥

V+ High Voltage Supply 75V
VCC Logic Supply 18V
IOUT Continuous Output Current 10A
IPK Peak Output Current 14A
θJC Thermal Resistance @ 125°C
(Output Switches)(Junction to Case) 1.5°C/W

TsT Storage Temperature Range . . . -65° to +150°C
TLD Lead Temperature Range
TC (10 Seconds) . . . . . 300°C
Case Operating Temperature
MSK 4303 . . . . . -40°C to +85°C
MSK 4303H/E . . . . . -55°C to +125°C
TJ Junction Temperature . . . . . +150°C

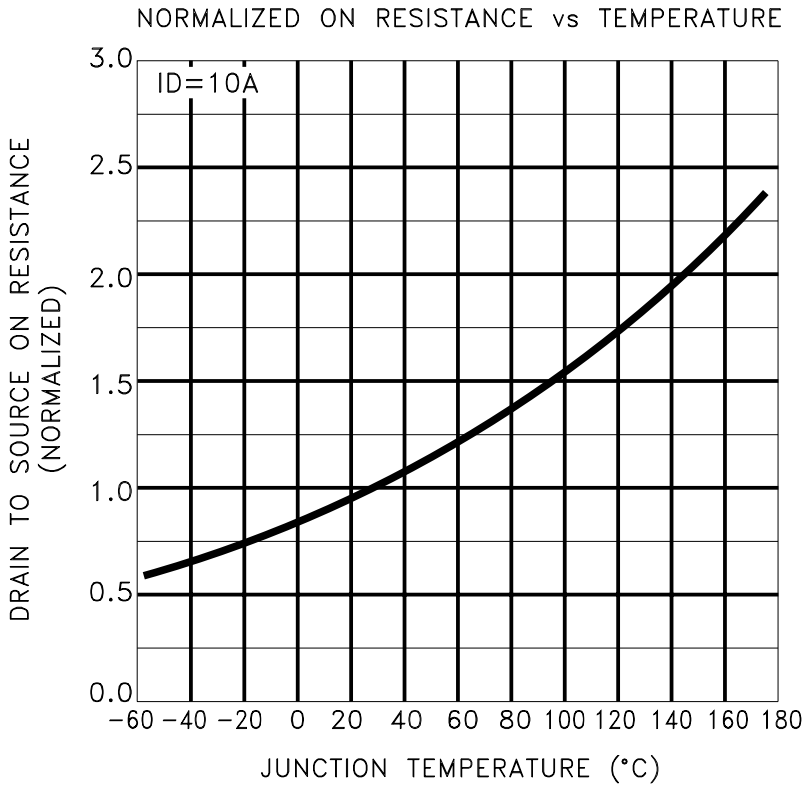
ELECTRICAL SPECIFICATIONS

Parameters	Test Conditions	GROUP A SUBGROUP ⑤	MSK 4303H/E ③ Min.	Typ.	Max.	MSK 4303 ② Min.	Typ.	Max.	UNITS
OUTPUT CHARACTERISTICS									
Drain-Source ON Resistance ① (each MOSFET) (for thermal calculations only)	Ic = 10A	1	-	-	0.013	-	-	0.013	Ω
		2	-	-	0.026	-	-	-	Ω
		3	-	-	0.013	-	-	-	Ω
Drain-Source Voltage (VDS(on)) (each MOSFET)	Ic = 10A	1	-	0.56	1.2	-	0.56	1.4	volts
		2	-	0.78	1.5	-	-	-	volts
		3	-	0.42	1.0	-	-	-	volts
Leakage Current (Each MOSFET)	V+ = 75V	1	-	1	25	-	1	25	μA
	V+ = 75V	2	-	10	250	-	-	-	mA
	V+ = 75V	3	-	1	25	-	-	-	mA
Reverse Recovery Time ①	ID = 10A, di/dt = 100A/μS	-	-	120	-	-	120	-	nS
BIAS SUPPLY CHARACTERISTICS									
+Vcc Bias Current	+Vcc = 15V	1,2,3	-	12	20	-	12	20	mA
+VB Bias Current	+VB = 15V	1,2,3	-	6	9	-	6	9	mA
INPUT SIGNAL CHARACTERISTICS									
Positive Trigger Threshold Voltage ①	+Vcc = 15V	-	2.7	-	-	2.7	-	-	volts
Negative Trigger Threshold Voltage ①	+Vcc = 15V	-	-	-	0.8	-	-	0.8	volts
Under-voltage Lockout	+Vcc Positive Going Threshold	1,2,3	8.0	8.9	9.8	8.0	8.9	9.8	volts
	+Vcc Negative Going Threshold	1,2,3	7.4	8.2	9.0	7.4	8.2	9.0	volts
Dead Time ①	Low Side Turn-off to High Side Turn-On	-	280	400	520	280	400	520	nSEC
	High Side Turn-off to Low Side Turn-On	-	4	5	6	4	5	6	μSEC

NOTES:

① Guaranteed by design but not tested. Typical parameters are representative of actual device performance but are for reference only.
② Industrial grade and "E" suffix devices shall be tested to subgroups 1 and 4 unless otherwise specified.
③ Military grade devices ("H" suffix) shall be 100% tested to subgroups 1, 2 and 3.
④ Subgroups 5 and 6 testing available upon request.
⑤ Subgroup 1, 4 TA = TC = +25°C
2, 5 TA = TC = +125°C
3, 6 TA = TC = -55°C
⑥ Continuous operation at or above absolute maximum ratings may adversely effect the device performance and/or life cycle.

TYPICAL PERFORMANCE CURVES



APPLICATION NOTES

MSK 4303 PIN DESCRIPTIONS

+VCC - Is the low voltage supply for all the internal logic and drivers. A 0.1 μF ceramic capacitor in parallel with a 10μF tantalum capacitor is the recommended bypassing from the +VCC pin to the COM pin.

H INA, H INB, H INC - Are high active logic inputs for signalling the corresponding phase high-side switch to turn on. The logic inputs are compatible with standard CMOS or LSTTL outputs. These logic inputs are internally zener clamped at 5.2 volts.

$\overline{\text{L INA}}$, $\overline{\text{L INB}}$, $\overline{\text{L INC}}$ - Are low active logic inputs for signalling the corresponding phase low-side switch to turn on. The logic inputs are compatible with standard CMOS or LSTTL outputs. These logic inputs are internally zener clamped at 5.2 volts.

AØ, BØ, CØ - Are the pins connecting the 3 phase bridge switch outputs.

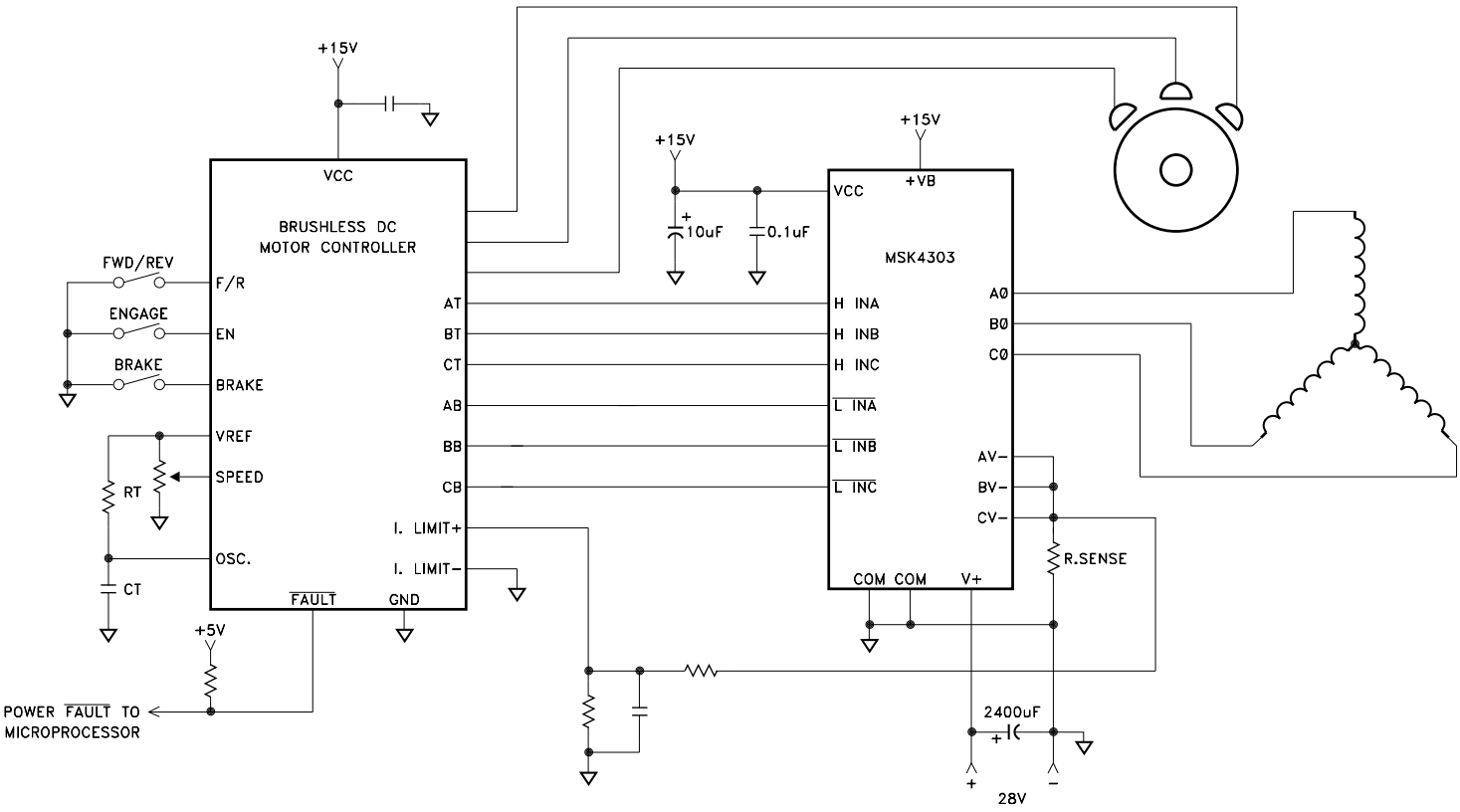
AV-, BV-, CV- - Are the connections from the bottoms of the three half bridges. These pins get connected to the COM pin. If current sensing is desired they may be connected to the COM pin through a low value sense resistor.

+VB - Is the connection used to provide power to the floating high-side bootstrap supplies in the gate drive circuitry.

V+ - Is the high voltage positive rail connection to the tops of the three half bridges. Proper power supply bypassing must be connected from this pin to the COM pin for good filtering. This bypassing must be done as close to the hybrid as possible.

COM - Is the connection that all hybrid power supply connections are returned to and bypassed to.

TYPICAL SYSTEM OPERATION



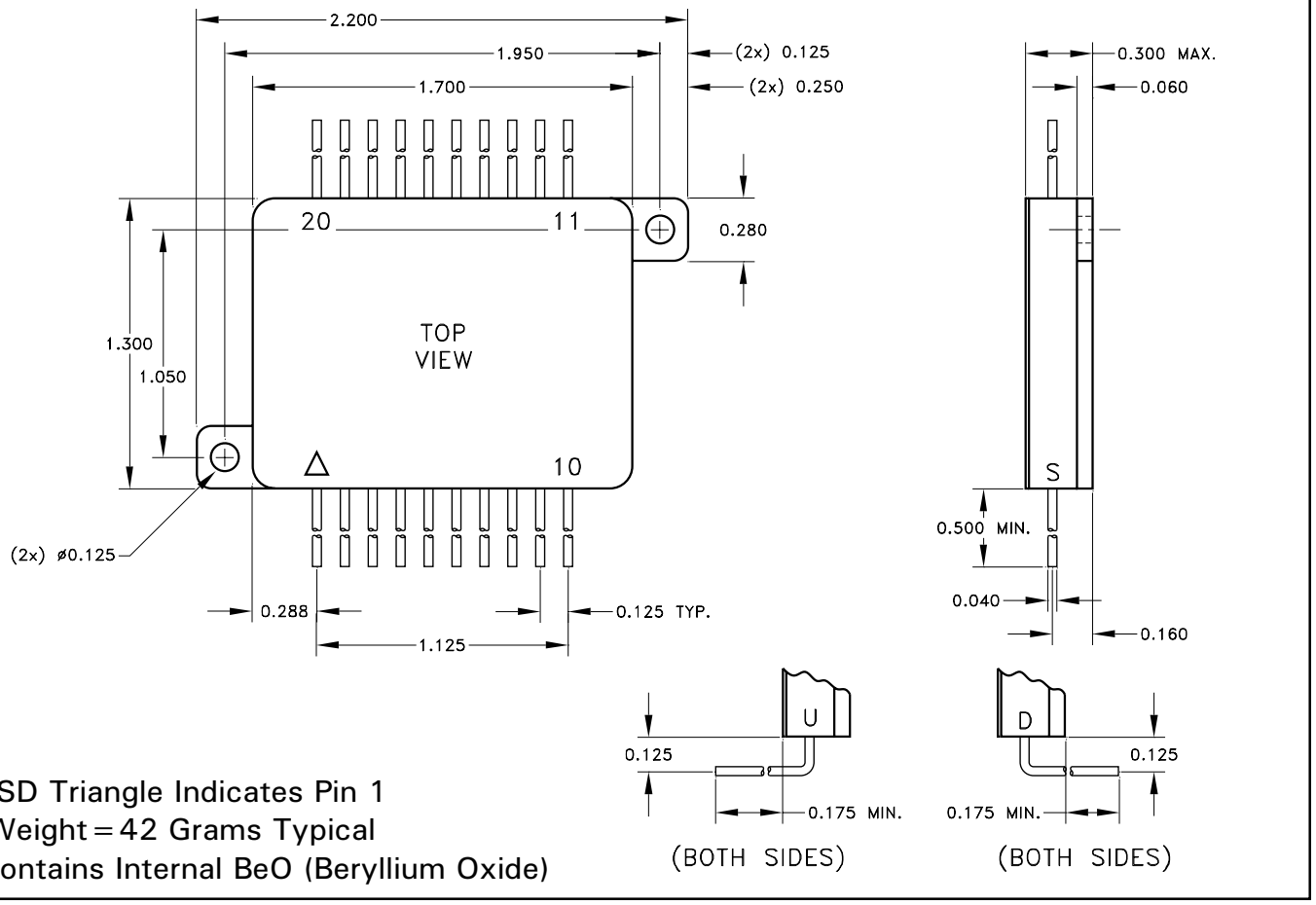
The MSK 4303 is designed to be used with a +28 volt high voltage bus, +15 volt low power bus and +5 volt logic signals. Proper derating should be applied when designing the MSK 4303 into a system. High frequency layout techniques with ground planes on a printed circuit board is the only method that should be used for circuit construction. This will prevent pulse jitter caused by excessive noise pickup on the current sense signal or the error amp signal.

Ground planes for the lower power circuitry and the high power circuitry should be kept separate. The connection between the bottom of the current sense resistor, COM pin and the high power ground, AV-, BV- and CV- pins are connected at this point. This is a critical path and high currents should not be flowing between the current sense and COM. Inductance in this path should be kept to a minimum. An RC filter (shown in 2 places) will filter out the current spikes and keep the detected noise for those circuits down to a minimum.

In the system shown a PWM pulse by pulse current limit scheme controlled by the motor controller is implemented.

When controlling the motor speed by the PWM method, it is required that the low side switches be PWM pulsed due to the bootstrap supplies used to power the high side switch drives. The higher the PWM speed the higher the current load on the drive supply. PWM of the low side will prevent sagging of the high side supplies. A separate pin (+VB) is provided for connecting an external floating power supply to power the bootstrap supplies.

MECHANICAL SPECIFICATIONS



ESD Triangle Indicates Pin 1
Weight = 42 Grams Typical
Contains Internal BeO (Beryllium Oxide)

All dimensions are ±0.01 inches unless otherwise specified.

ORDERING INFORMATION

MSK4303 H U

LEAD CONFIGURATIONS
S = STRAIGHT; U = BENT UP; D = BENT DOWN

SCREENING
BLANK = INDUSTRIAL; H = MIL-PRF-38534 CLASS H;
E = EXTENDED RELIABILITY

GENERAL PART NUMBER

M.S. Kennedy Corp.
4707 Dey Road, Liverpool, New York 13088
Phone (315) 701-6751
FAX (315) 701-6752
www.mskennedy.com