

MM74HCT00 Quad 2 Input NAND Gate

General Description

The MM74HCT00 is a NAND gates fabricated using advanced silicon-gate CMOS technology which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. This device is input and output characteristic and pin-out compatible with standard 74LS logic families. All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

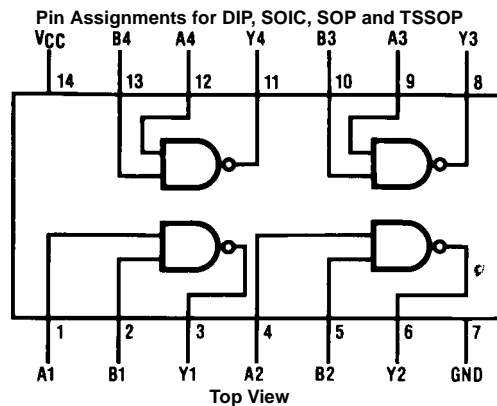
- TTL, LS pin-out and threshold compatible
- Fast switching: t_{PLH} , t_{PHL} =14 ns (typ)
- Low power: 10 μ W at DC
- High fan out, 10 LS-TTL loads

Ordering Code:

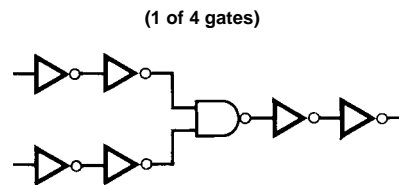
| Order Number | Package Number | Package Description |
|------------------|----------------|--|
| MM74HCT00M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| MM74HCT00MX_NL | M14A | Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| MM74HCT00SJ | M14D | Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| MM74HCT00MTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| MM74HCT00MTCX_NL | MTC14 | Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| MM74HCT00N | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| MM74HCT00N_NL | N14A | Pb-Free 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Connection Diagram



Logic Diagram



Absolute Maximum Ratings (Note 1)

(Note 2)

| | |
|--|-----------------------|
| Supply Voltage (V_{CC}) | -0.5 to +7.0V |
| DC Input Voltage (V_{IN}) | -1.5 to $V_{CC}+1.5V$ |
| DC Output Voltage (V_{OUT}) | -0.5 to $V_{CC}+0.5V$ |
| Clamp Diode Current (I_{IK}, I_{OK}) | ± 20 mA |
| DC Output Current, per pin (I_{OUT}) | ± 25 mA |
| DC V_{CC} or GND Current, per pin (I_{CC}) | ± 50 mA |
| Storage Temperature Range (T_{STG}) | -65°C to +150°C |
| Power Dissipation (P_D) | |
| (Note 3) | 600 mW |
| S.O. Package only | 500 mW |
| Lead Temperature (T_L) | |
| (Soldering 10 seconds) | 260°C |

Recommended Operating Conditions

| | Min | Max | Units |
|---|-----|----------|-------|
| Supply Voltage (V_{CC}) | 4.5 | 5.5 | V |
| DC Input or Output Voltage (V_{IN}, V_{OUT}) | 0 | V_{CC} | V |
| Operating Temperature Range (T_A) | -40 | +85 | °C |
| Input Rise or Fall Times (t_r, t_f) | | 500 | ns |

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ (unless otherwise specified)

| Symbol | Parameter | Conditions | $T_A = 25^\circ\text{C}$ | | $T_A = -40$ to 85°C | $T_A = -55$ to 125°C | Units | |
|----------|-----------------------------------|--|--------------------------|-------------------|-----------------------------------|------------------------------------|---------------|---|
| | | | Typ | Guaranteed Limits | | | | |
| V_{IH} | Minimum HIGH Level Input Voltage | | | 2.0 | 2.0 | 2.0 | V | |
| V_{IL} | Maximum LOW Level Input Voltage | | | 0.8 | 0.8 | 0.8 | V | |
| V_{OH} | Minimum HIGH Level Output Voltage | $V_{IN} = V_{IH}$ or V_{IL} | | V_{CC} | $V_{CC}-0.1$ | $V_{CC}-0.1$ | $V_{CC}-0.1$ | V |
| | | $ I_{OUT} = 20 \mu\text{A}$ | | 4.2 | 3.98 | 3.84 | 3.7 | V |
| | | $ I_{OUT} = 4.0 \text{ mA}, V_{CC} = 4.5V$ $ I_{OUT} = 4.8 \text{ mA}, V_{CC} = 5.5V$ | | 5.2 | 4.98 | 4.84 | 4.7 | V |
| V_{OL} | Maximum LOW Level Voltage | $V_{IN} = V_{IH}$ | | 0 | 0.1 | 0.1 | 0.1 | V |
| | | $ I_{OUT} = 20 \mu\text{A}$ | | 0.2 | 0.26 | 0.33 | 0.4 | V |
| | | $ I_{OUT} = 4.0 \text{ mA}, V_{CC} = 4.5V$ $ I_{OUT} = 4.8 \text{ mA}, V_{CC} = 5.5V$ | | 0.2 | 0.26 | 0.33 | 0.4 | V |
| I_{IN} | Maximum Input Current | $V_{IN} = V_{CC}$ or GND, V_{IH} or V_{IL} | | ± 0.05 | ± 0.5 | ± 1.0 | μA | |
| I_{CC} | Maximum Quiescent Supply Current | $V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0 \mu\text{A}$ | | 1.0 | 10 | 40 | μA | |
| | | $V_{IN} = 2.4V$ or $0.5V$ (Note 4) | 0.18 | 0.3 | 0.4 | 0.5 | mA | |

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics
 $V_{CC} = 5.0V$, $t_r = t_f = 6 \text{ ns}$, $C_L = 15 \text{ pF}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Units |
|-----------------------|---------------------------|------------|-----|------------------|-------|
| t_{PLH} , t_{PHL} | Maximum Propagation Delay | | 14 | 18 | ns |

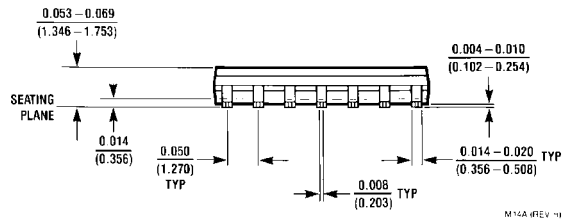
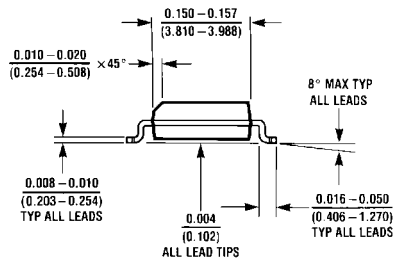
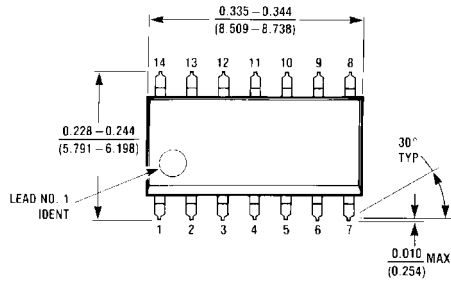
AC Electrical Characteristics
 $V_{CC} = 5.0V \pm 10\%$, $t_r = t_f = 6 \text{ ns}$, $C_L = 50 \text{ pF}$ (unless otherwise noted)

| Symbol | Parameter | Conditions | $T_A = 25^\circ\text{C}$ | | $T_A = -40 \text{ to } 85^\circ\text{C}$ | $T_A = -55 \text{ to } 125^\circ\text{C}$ | Units |
|-----------------------|---------------------------------|------------|--------------------------|-------------------|--|---|-------|
| | | | Typ | Guaranteed Limits | | | |
| t_{PLH} , t_{PHL} | Maximum Propagation Delay | | 18 | 23 | 29 | 35 | ns |
| t_{THL} , t_{TLH} | Maximum Output Rise & Fall Time | | 8 | 15 | 19 | 22 | ns |
| C_{PD} | Power Dissipation Capacitance | (Note 5) | 30 | | | | pF |
| C_{IN} | Input Capacitance | | 5 | 10 | 10 | 10 | pF |

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

MM74HCT00

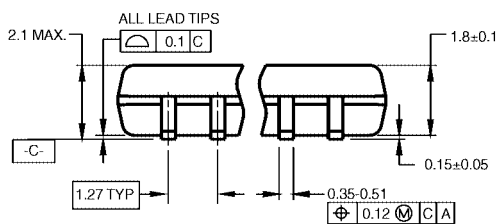
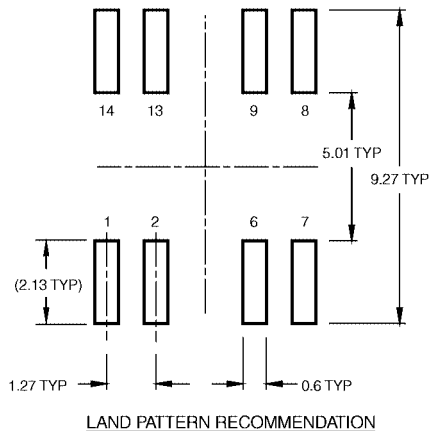
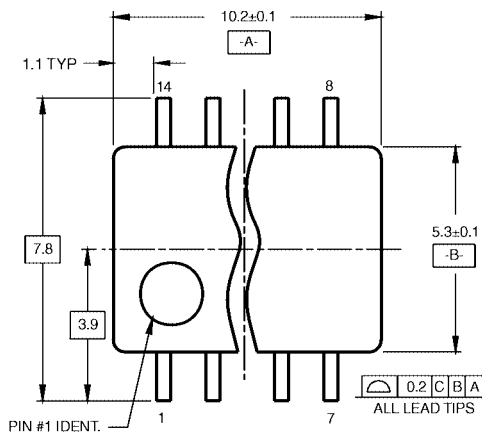
Physical Dimensions inches (millimeters) unless otherwise noted



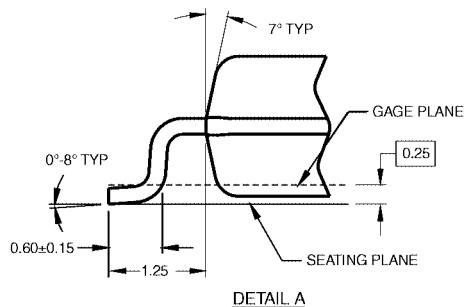
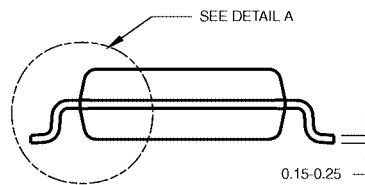
M14A (REV. 11)

**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

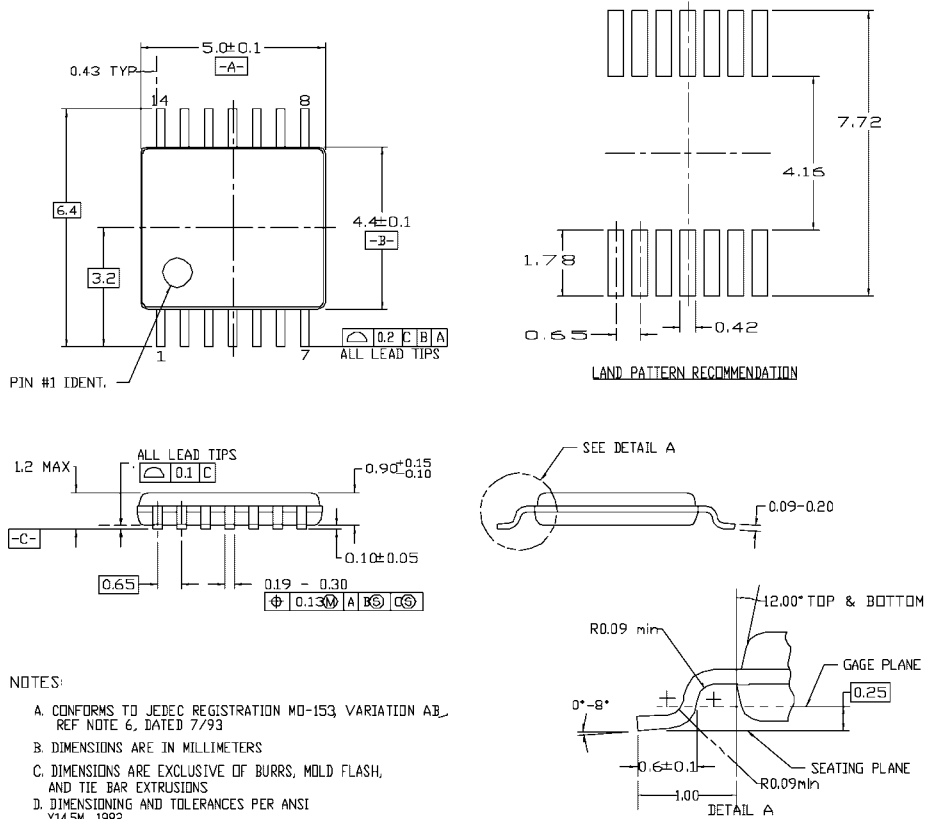


- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

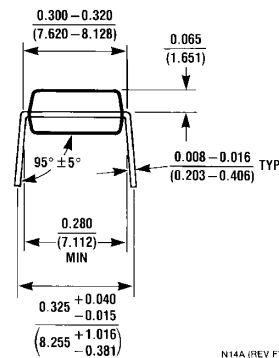
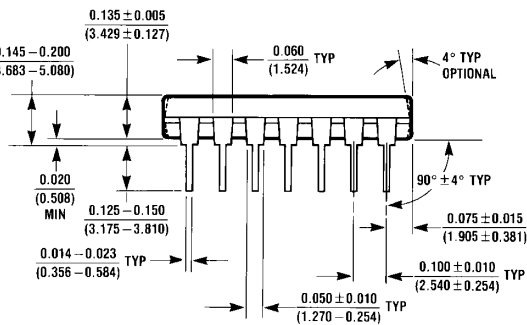
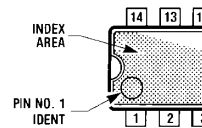
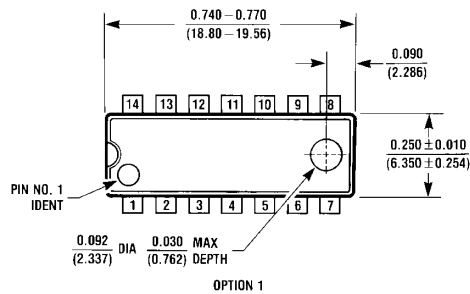


- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153 VARIATION AB, REF NOTE 6, DATED 7/93
 - B. DIMENSIONS ARE IN MILLIMETERS
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
 - D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

N14A (REV F)

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