NPN
MJ3281A*
PNP
MJ1302A*

*Motorola Preferred Device

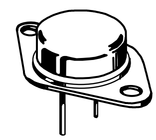
Designer's™ Data Sheet

Complementary NPN-PNP Silicon Power Bipolar Transistor

The MJ3281A and MJ1302A are PowerBase power transistors for high power audio, disk head positioners and other linear applications.

- Designed for 100 W Audio Frequency
- Gain Complementary:
  - — Gain Linearity from 100 mA to 7 A
  - — High Gain — 60 to 175
  - — h_{FE} = 45 (Min) @ I_C = 8 A
- Low Harmonic Distortion
- High Safe Operation Area — 1 A/100 V @ 1 sec
- High f_T — 30 MHz Typical

15 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 200 VOLTS 250 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	200	Vdc
Collector–Base Voltage	V_{CBO}	200	Vdc
Emitter–Base Voltage	V_{EBO}	7	Vdc
Collector–Emitter Voltage — 1.5 V	V_{CEX}	200	Vdc
Collector Current — Continuous — Peak (1)	I_C	15 25	Adc
Base Current — Continuous	I_B	1.5	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	250 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle <10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Designer's is a trademark of Motorola, Inc.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	200	—	—	Vdc
Emitter–Base Voltage (I_E = 100 µAdc, I_C = 0)	V_{EBO}	7	—	—	Vdc
Collector Cutoff Current (V_{CB} = 200 Vdc, I_E = 0)	I_{CBO}	—	—	50	µAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	—	—	5	µAdc
Emitter Cutoff Current (V_{EB} = 7 Vdc, I_C = 0)	I_{EBO}	—	—	25	µAdc
SECOND BREAKDOWN					
Second Breakdown Collector with Base Forward Biased	$I_{S/b}$				Adc
(V_{CE} = 50 Vdc, t = 1 s (non–repetitive)		4	—	—	
(V_{CE} = 100 Vdc, t = 1 s (non–repetitive)		1	—	—	
ON CHARACTERISTICS					
DC Current Gain	h_{FE}				
(I_C = 100 mAdc, V_{CE} = 5 Vdc)		60	125	175	
(I_C = 1 Adc, V_{CE} = 5 Vdc)		60	—	175	
(I_C = 3 Adc, V_{CE} = 5 Vdc)		60	—	175	
(I_C = 5 Adc, V_{CE} = 5 Vdc)		60	—	175	
(I_C = 7 Adc, V_{CE} = 5 Vdc)		60	115	175	
(I_C = 8 Adc, V_{CE} = 5 Vdc)		45	—	—	
(I_C = 15 Adc, V_{CE} = 5 Vdc)		12	35	—	
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1 Adc)	$V_{CE(sat)}$	—	—	3	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 1 Adc, V_{CE} = 5 Vdc, f_{test} = 1 MHz)	f_T	—	30	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	—	—	600	pF

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

PNP MJ1302A

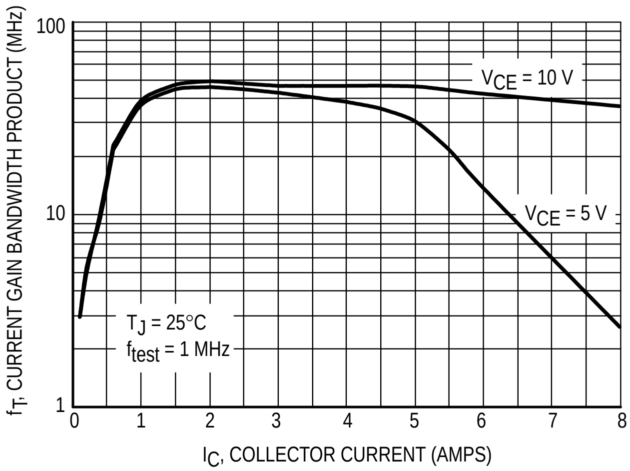


Figure 1. Current–Gain — Bandwidth Product

NPN MJ3281A

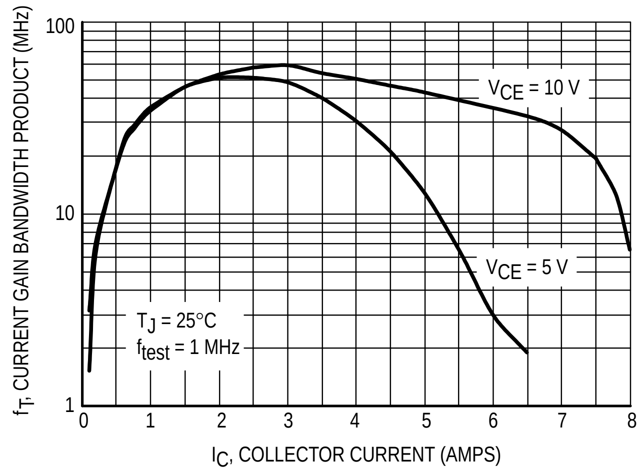


Figure 2. Current–Gain — Bandwidth Product

PNP MJ1302A

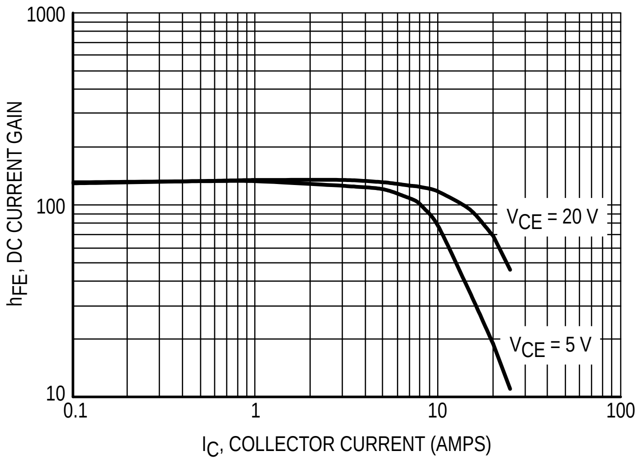


Figure 3. DC Current Gain

NPN MJ3281A

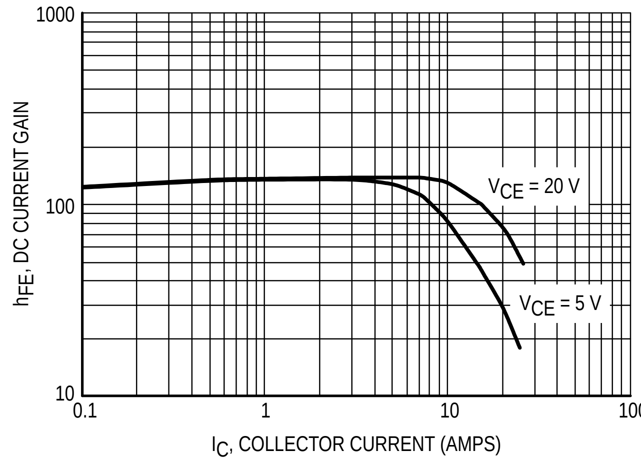


Figure 4. DC Current Gain

PNP MJ1302A

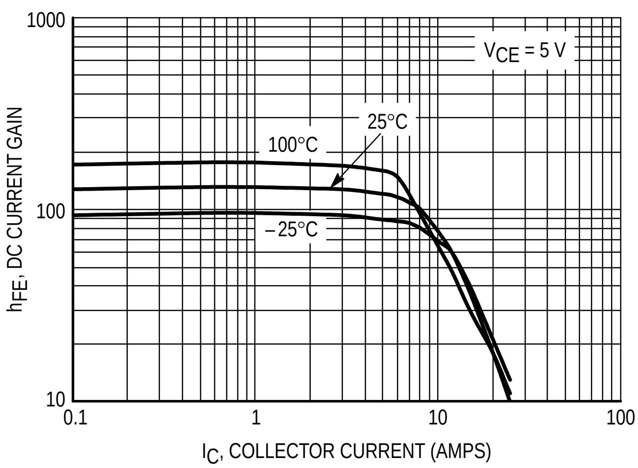


Figure 5. DC Current Gain, V_{CE} = 5 V

NPN MJ3281A

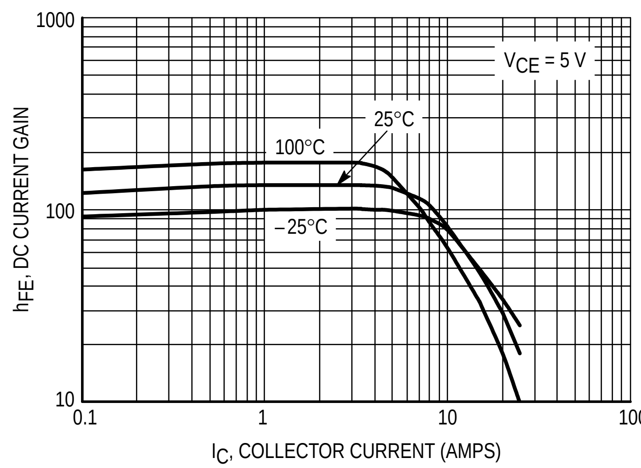


Figure 6. DC Current Gain, V_{CE} = 5 V

TYPICAL CHARACTERISTICS

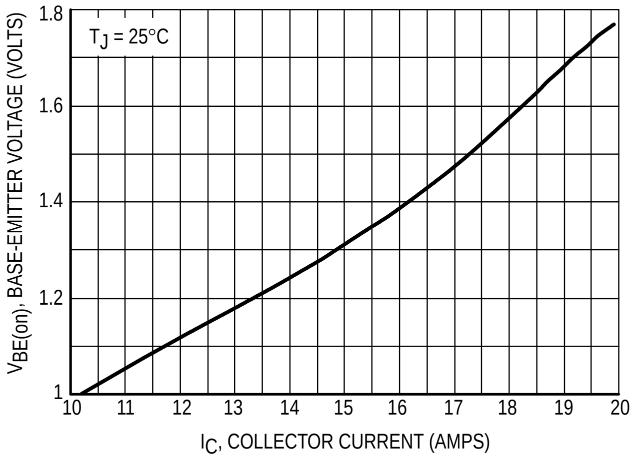


Figure 7. Typical Base–Emitter Voltage

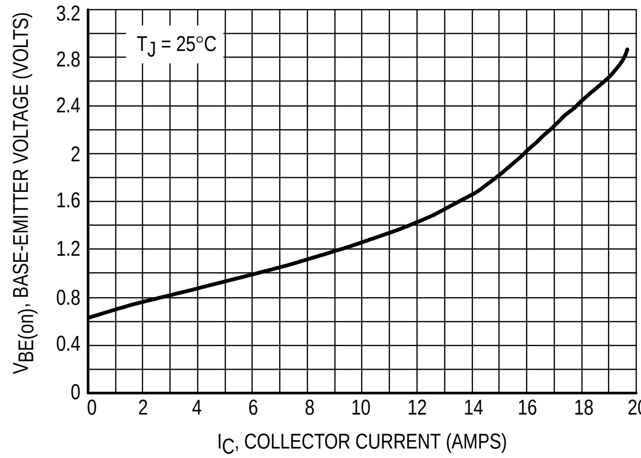


Figure 8. Typical Base–Emitter Voltage

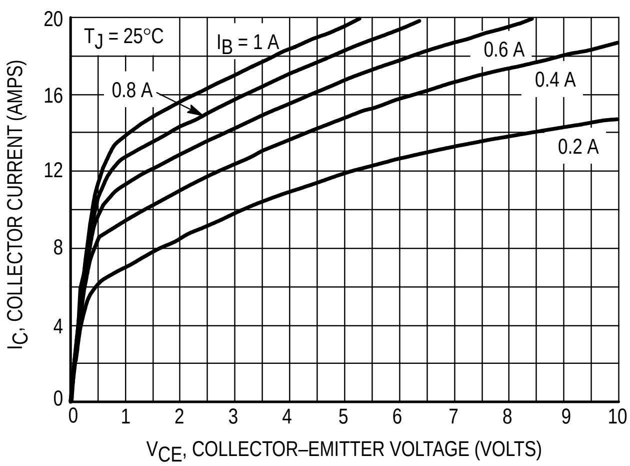


Figure 9. Typical Output Characteristics

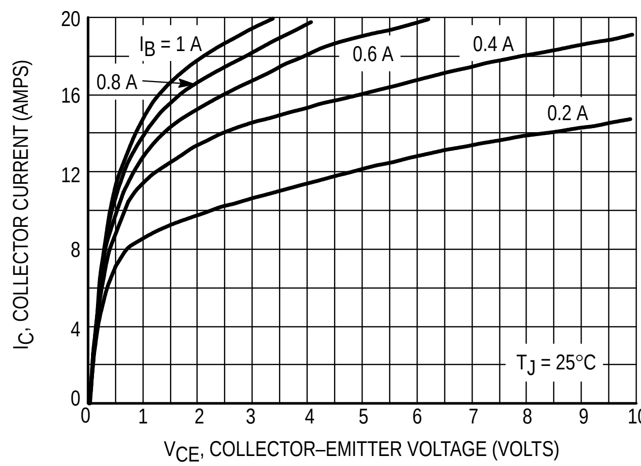


Figure 10. Typical Output Characteristics

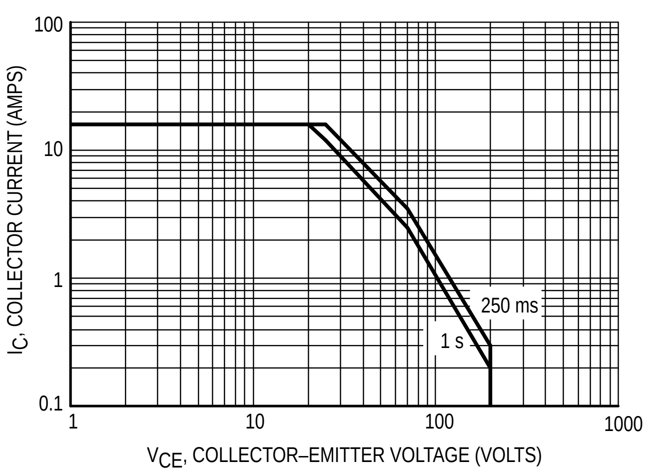
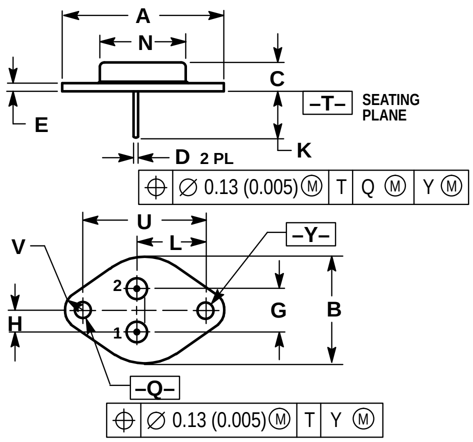


Figure 11. Forward Bias Safe Operating Area (FBSOA)

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

CASE 1–07
TO–204AA (TO–3)
ISSUE Z

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