M66244FP

June 1998 Ver.8.0.0

High Speed Monolithic Pulse Width Modulator

NOTE:This is not final specification. Some parametric limits are subject to change

DESCRIPTION

The M66244FP is a high-speed digitally programmable pulse width modulator (PWM) which uses high-performance silicon gate CMOS process technology.Output pulse width is proportional to a 6-bit DATA input value. Two additional CONTROL inputs determine if the pulse is placed at the beginning , middle ,or end of the clock period. Pulse width and placement can be changed every clock cycle up to 72MHz.

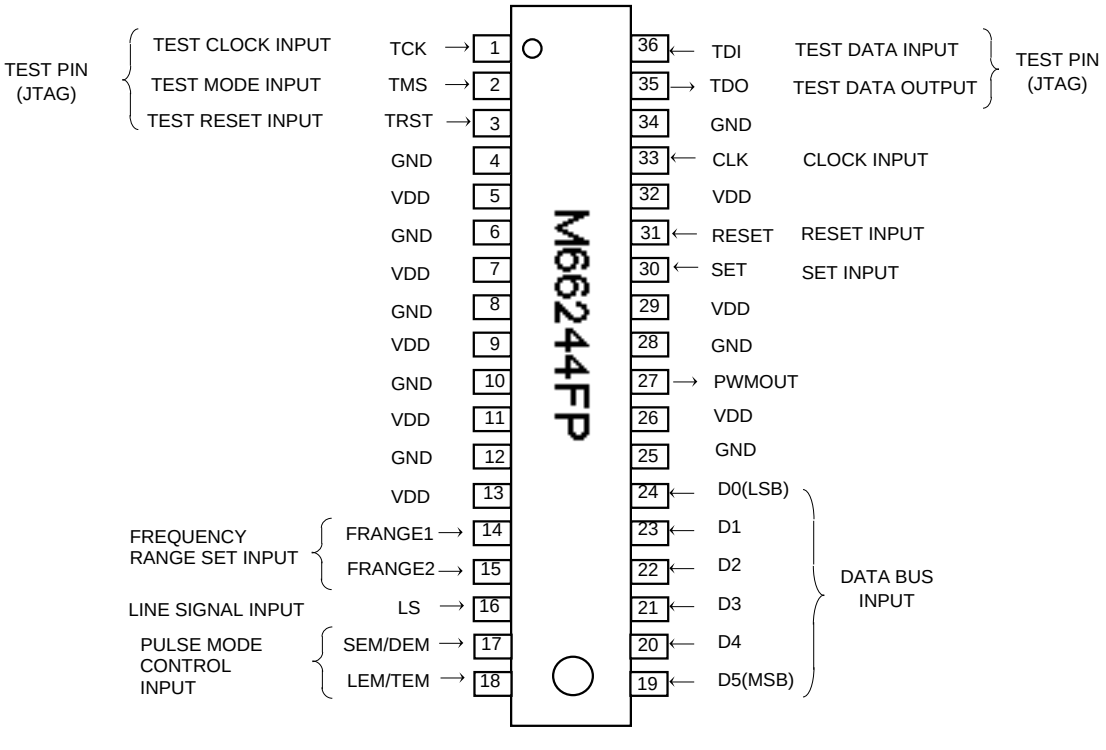
FEATURES

- Frequency 45MHz to 72MHz
- 6 bit Resolution
- Center, Leading, Trailing Edge Modulation
- Single 3.3V Operation
- JTAG (IEEE Standard 1149.1Test Port)

APPLICATIONS

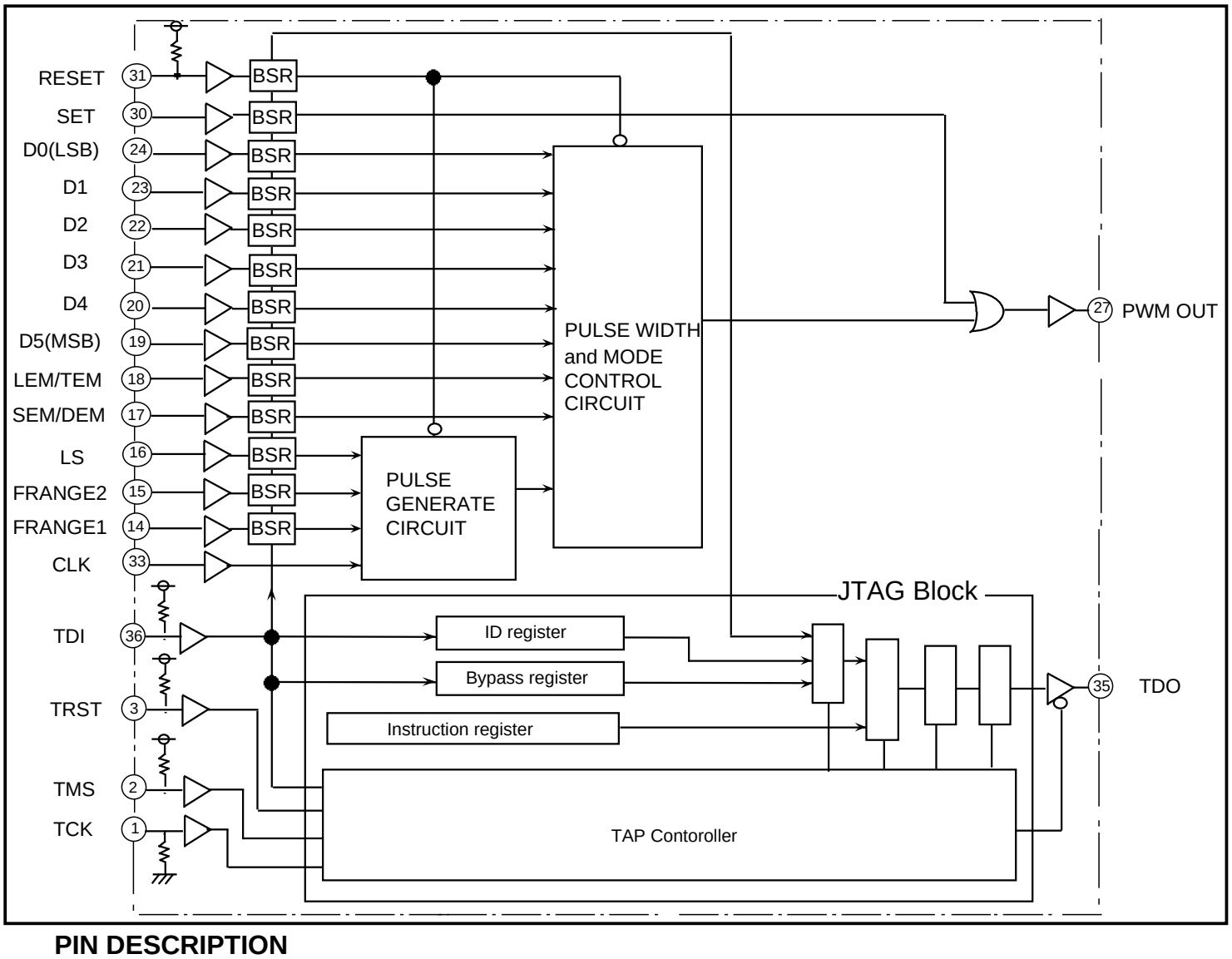
- Laser Printers
  Gray Scale Capability
  Resolution Enhancement
- Copiers
- Optical Disk Drives
- Precision Pulse Placement

PIN CONFIGURATION (TOP VIEW)



Outline 36P2R

BLOCK DIAGRAM



PIN DESCRIPTION

PIN NAME	NAME	IN/OUT buffer type	DESCRIPTION
D0-D5	Digital Data Bit	normal Input	6 bit Digital Data from MPU
CLK	Clock input	normal Input	Dot Clock input
PWM OUT	PWM output	normal output	PWM output
SEM/DEM LEM/TEM	Control output pulse mode	normal Input	Control pin of output pulse mode (refer to page 3)
SET	Set input	normal Input	When SET is "H", PWM output is "H" (direct set) When SET is "L", PWM output depend on D<5:0>
RESET	Reset input	schmitt Input (Pull-up 50kΩ)	When RESET is "L", M66244FP is reset to initial state.
LS	Line Signal input	normal Input	refer to page 10
FRANGE1 FRANGE2	Operation Frequency range set up	normal Input	FRANGE1 and FRANGE2 are set up correspond to operation frequency range (refer to page 8)
TRST	Test Reset input	schmitt Input (Pull-up 50kΩ)	Test Reset input of JTAG test circuit
TMS	Test Mode Select input	normal Input (Pull-up 50kΩ)	Test Mode Select input of JTAG test circuit
TCK	Test Clock input	schmitt Input(Pull-down 50kΩ)	Test Clock input of JTAG test circuit
TDI	Test Data In input	normal Input (Pull-up 50kΩ)	Test Data input of JTAG test circuit
TDO	Test Data Out output	3-sate output	Test Data output of JTAG test circuit

FUNCTION

M66244 can control "H" width and positioning of PWM output by DATA pins (D<5:0>) and CONTROL pins (SEM/DEM,LEM/TEM) in each CLK period.

These inputs can be updated on the rising edge of the CLK.

Positioning the width-controlled pulse are begging , middle ,or end of the clock period.

This is accomplished through CONTROL pins (SEM/DEM,LEM/TEM)

Pulse positioning within the clock period is defined by the following CONTROL truth table.

SEM/DEM	LEM/TEM	Alignment
1	1	Right hand justify
1	0	Left hand justify
0	X	Center justify

SEM/DEM : single edge modulation / dual edge modulation
LEM/TEM : leading edge modulation / trailing edge modulation

The diagram of page4 illustrates the output of the M66244FP with various DATA(D<5:0>) , CONTROL(SEM/DEM, LEM/TEM) inputs and PWM output.
This does not take into account any delays,which will explain later.
The rising edge is delayed from the leading edge of the clock, and the falling edge is delayed from the center of the clock period.

Top line shows the clock; the second shows DATA inputs ; third shows CONTROL inputs being updated on the rising edge of clock. The forth line shows the resulting PWM pulse with an explanation of the second and third lines.

In the first cycle (Ncycle) , DATA is 3F . So the CONTROL value is shown as "X". This means the value is not important because a 100% pulse will be output for any CONTROL value.

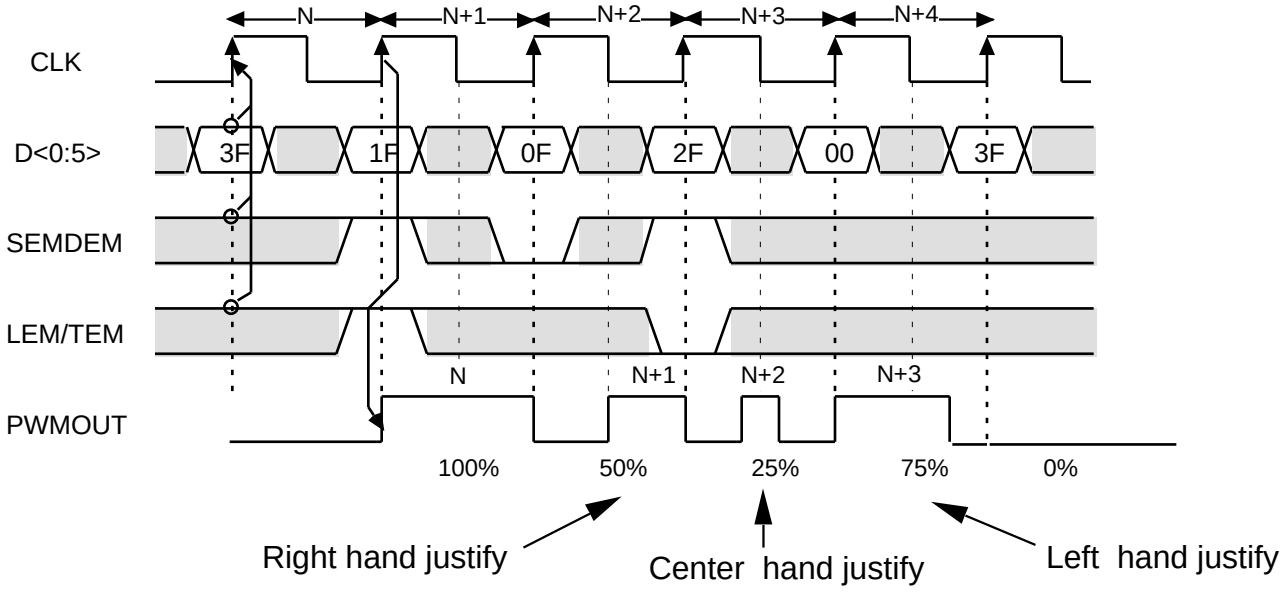
In the second cycle (N+1cycle) , DATA is 1F , SEM/DEM is "H" and LEM/TEM is "H". This means PWMoutput width is 50% and positioning is right hand justify.

In the third cycle (N+2cycle) , DATA is 0F , SEM/DEM is "L" and LEM/TEM is "X". This means PWMoutput width is 25% and positioning is center justify.

In the fourth cycle (N+3cycle) , DATA is 2F , SEM/DEM is "H" and LEM/TEM is "L". This means PWMoutput width is 75% and positioning is left hand justify.

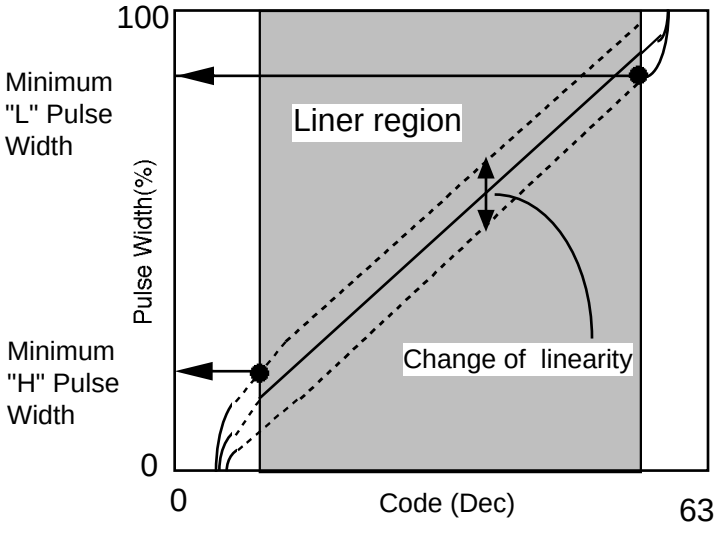
In the fifth cycle (N+4cycle) , DATA is 00 . So the CONTROL value is shown "X" . This means the value is not important because a 0% pulse will be output for any CONTROL value.

PWM OUTPUT EXAMPLE

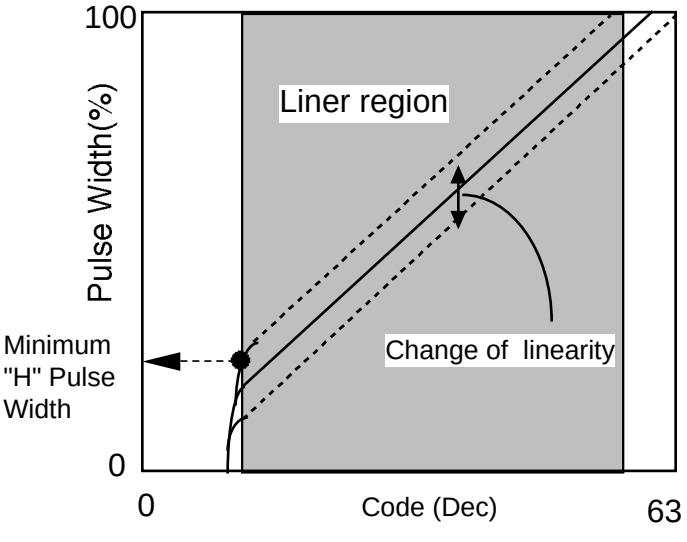


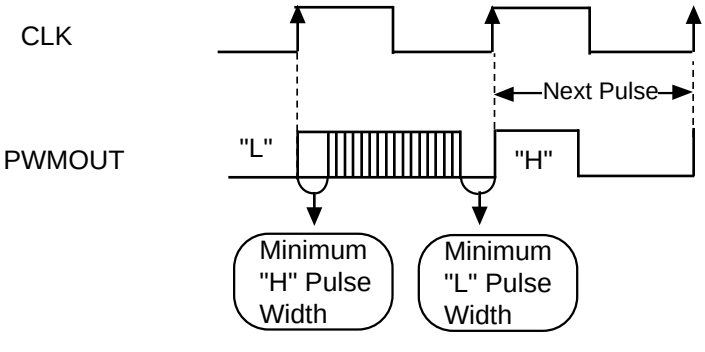
PWM Pulse linearity (image figure)

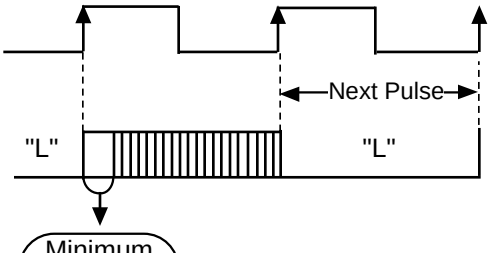
(1) In case of next pulse is "H"



(2) In case of next pulse is "L"



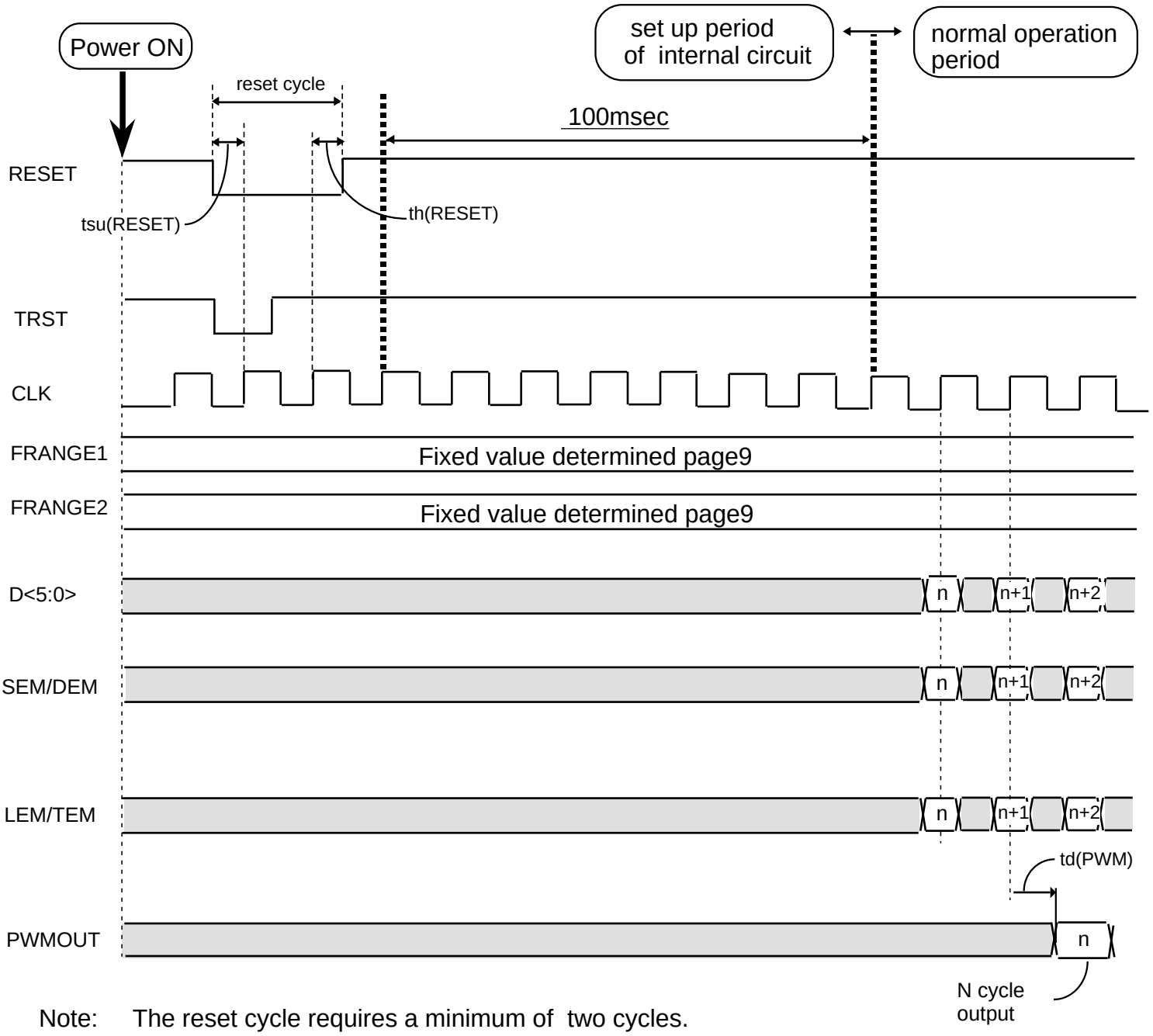




OPERATING TIMING BETWEEN POWER ON TO NORMAL OPERATION

After Power on, it needs following oerations before start normal operation.

(1) Set the value of FRANGE1 and FRANGE2 depends on operation ferequency. (Refer to page 9)
(2) Input CLK same as normal operarion frequency.
(3) Reset operarion using RESET (31pin) and TRST (3pin) .
(reset to initial state of internal logic and BSR)
(4) CLK continue to input during 100msec.

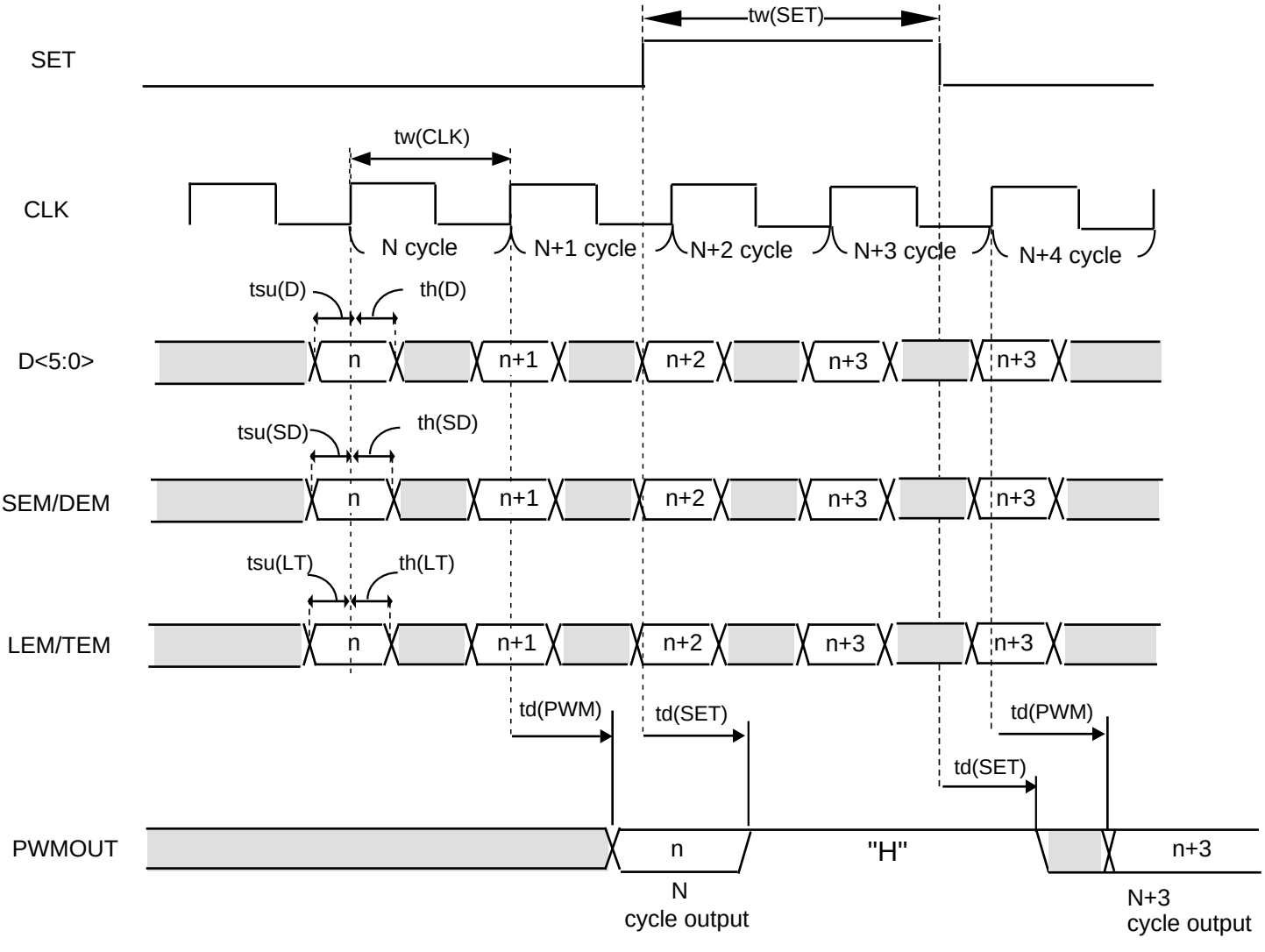


Note: The reset cycle requires a minimum of two cycles.

OPERATING TIMING EXAMPLE

DATA(D<0:5>) and CONTROL(SEM/DEM,LEM/TEM) are written to the latching circuit at the first rise edge of CLK. PWMOUT is outputted at the next edge of CLK. A propagation delay exists between the CLK and PWMOUT pulse. The minimum propagation delay can be observed when alternating between codes 00(H) and 3F(H).

In the following diagram, when SET is "H" , PWM output is "H" , when SET is "L" , PWMOUT is determined correspond to D<5:0>. The function of SET is direct set, so when the rise edge of CLK and SET are entered at the same time PWMOUT will be "H" .



TIMING CONDITIONS (Ta=0~ 70˚C,Vcc=3.3V±5%, GND=0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
tw(CLK)	Clock cycle	14		22	ns
duty(CLK)	Clock duty			±7	%
tsu(RESET)	RESET setup time to CLK	6			ns
th(RESET)	RESET hold time to CLK	6			ns
tw(SET)	SET pulse width	14			ns
tsu(D)	Input data setup time to CLK	6			ns
th(D)	Input data hold time to CLK	6			ns
tsu(SD)	SEM/DEM setup time to CLK	6			ns
th(SD)	SEM/DEM hold time to CLK	6			ns
tsu(LT)	LEM/TEM setup time to CLK	6			ns
th(LT)	LEM/TEM hold time to CLK	6			ns
tr / tf	Input pulse rise / fall time			2	ns
tw(TCK)	TCK cycle	50			ns
tsu(TDI)	TDI setup time to CLK	10			ns
th(TDI)	TDI hold time to CLK	10			ns
tsu(TMS)	TMS setup time to CLK	10			ns
th(TMS)	TMS hold time to CLK	10			ns
tw(TRST)	TRST pulse width	20			ns

SWITCHING CHARACTERISTICS (Ta=0~ 70˚C,Vcc=3.3V±5%, GND=0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
td (PWM)	PWM output access time			40	ns
td (SET)	"H" output access time			20	ns
td (TDO)	TDO access time			40	ns

OUTPUT PULSE LINEARITY (Ta=0~ 70˚C,Vcc=3.3V±5%, GND=0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
DLV	Differential linearity by voltage change			4	%
DLT	Differential linearity by temperature change			4	%
DLW	Differential linearity by wafer lot change			4	%
Pw+(min)	Minimum "H" pulse width (@CL=10pF)	4			ns
Pw−(max)	Minimum "L" pulse width (@CL=10pF)	4			ns

ABSOLUTE MAXIMUM RATINGS (Ta=0~70˚C unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	A value based GND pin	-0.3~+4.6	V
VI	Input voltage		-0.3~Vcc+0.3	V
Vo	Output voltage		-0.3~Vcc+0.3	V
Pd	Maximum power dissipation	Ta = 70 ˚C	414	mW
Tstg	Storage temperature		-55~150	˚C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
Vcc	Supply voltage	3.15	3.3	3.45	V
GND	Supply voltage		0		V
Topr	Operating ambient temperature	0~70			˚C

ELECTRICAL CHARACTERISTICS (Ta=0~70˚C, Vcc=3.3V±5%,GND=0V unless otherwise noted)

Symbol	Parameter	Conditions		Limits			Unit
				Min.	Typ.	Max.	
VIH	"H" Input voltage for normal type input	D0~D5, LEM/TEM ,LS SEM//DEM, CLK, SET, FRANGE1, FRANGE2		Vcc x 0.8			V
VIL	"L" Input voltage for normal type input					0.8	V
VT-	Negative going threshold voltage for schmitt type input	TCK, TRST, RESET Vcc=3.3V		0.5		1.65	V
VT+	positive going threshold voltage for schmitt type input			1.4		2.4	V
VH	Hysteresis for schmitt type input				0.75		V
VOH	"H" Output voltage	IOH=-2mA		2.0			V
VOL	"L" Output voltage	IOL=2mA				0.55	V
IIH	"H" Input current	VI=Vcc				10	µA
IIL	"L" Input current	VI=GND				-10	µA
IOZH	Off state "H" output current	Vo=Vcc	TDO			10	µA
IOZL	Off state "L" output current	Vo=GND	TDO			-10	µA
Icc	Operating mean current dissipation	f=72MHz , CL=10pF				120	mA
CI	Input capacitance	f=1MHz				10	pF
CO	Off state output capacitance	f=1MHz				15	pF

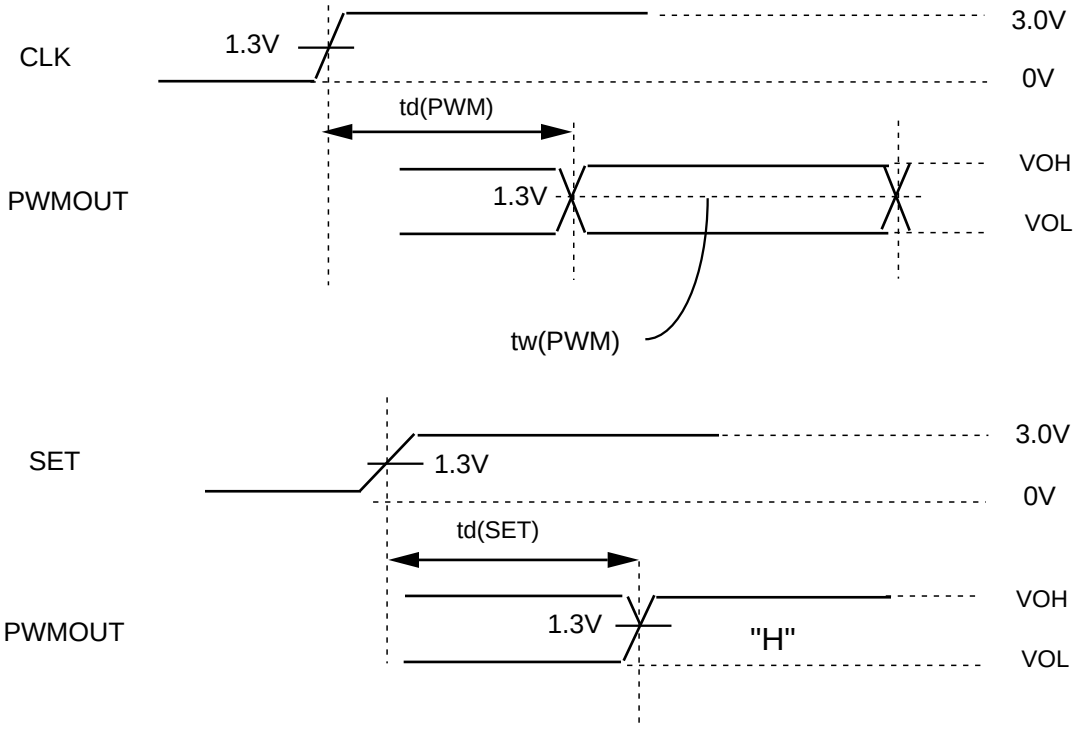
Note 1 : under consideration

SETTING OF OPERATING FREQUENCY RANGE

M66244FP can operate between 45MHz to 72MHz of clock frequency, it needs to set the value of the FRANGE1 and FRANGE2 correspond to operating frequency.

Frequency range	FRANGE1	FRANGE2
45MHz~50MHz	L	H
50MHz~60MHz	H	L
60MHz~72MHz	H	H

TIMING of PROPAGATION DELAY and THRESHOLD VOLTAGE of PULSE WIDTH



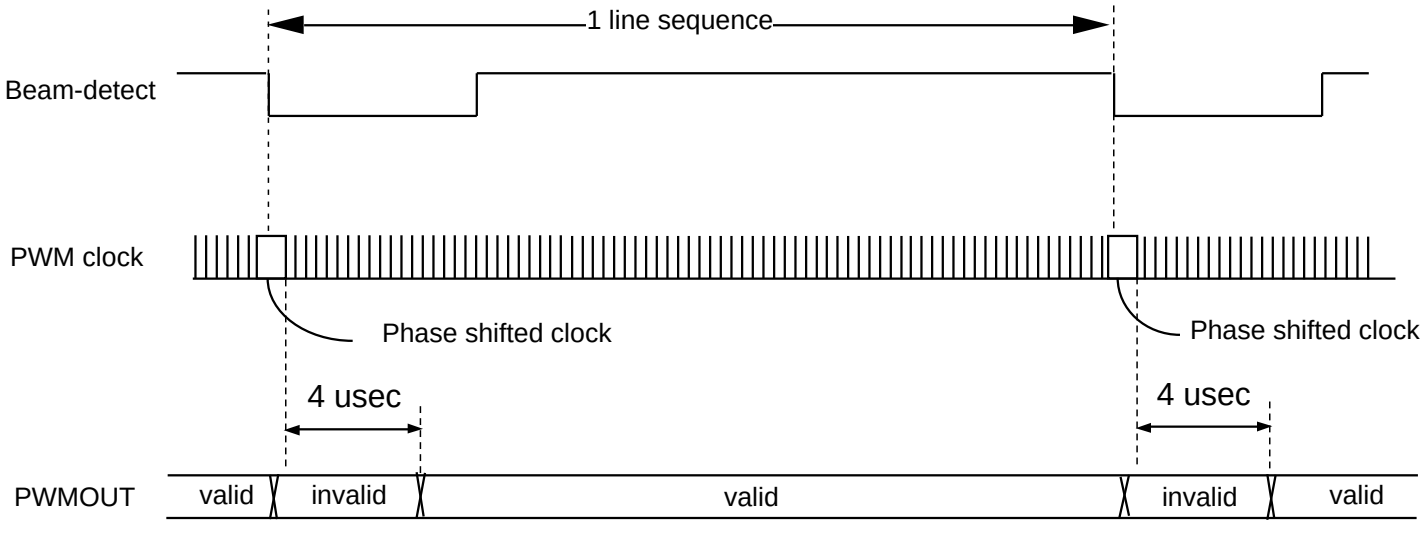
NOTE : OUTPUT LOAD 10pF

Solution for clock period is shifted

In the printer or copier system, there are some possibility that clock period is shifted because beam detect signal generates at the beginning of each pass across the paper.

If clock period is shifted one time, PWMOUT will be invalid. It needs long time to recover valid PWMOUT after previous clock period inputted.

To settle above problem, beam detect signal take in to LS (16 pin) of M66244FP.
For this, It can recover valid PWMOUT within 4usec after previous clock period inputted.



Example of operating timing using LS function

clock stopped time (ns)	recovery time(ns)
20	1000
40	1000
60	2000
80	4000
100	7000
200	10000
400	14000
600	17000
800	20000
1000	23000
2000	30000
4000	40000

recovery time that not using LS function

TEST CIRCUIT DESCRIPTION (JTAG)

GENERAL DESCRIPTION

The Test Access Port conforms with the IEEE standard 1149.1.
This standard defines a test access port and boundary-scan architecture for digital integrated circuits.
The facilities defined by the standard seek to provide a solution to the problem of testing assembled printed circuit boards and other products based on highly complex digital integrated circuits and high-density surface-mounting assembly techniques. They also provide a means of accessing and controlling design-for-test features build into digital integrated circuits themselves.

PIN DESCRIPTION

TCK,TMS,TDI,TRST,TDO are used in this test operation.

•Test Clock Input (TCK)
TCK provides the clock for the test logic defined by this standard. Stored-state devices contained in the test logic retain their state indefinitely when the signal applied to TCK is stopped at 0.

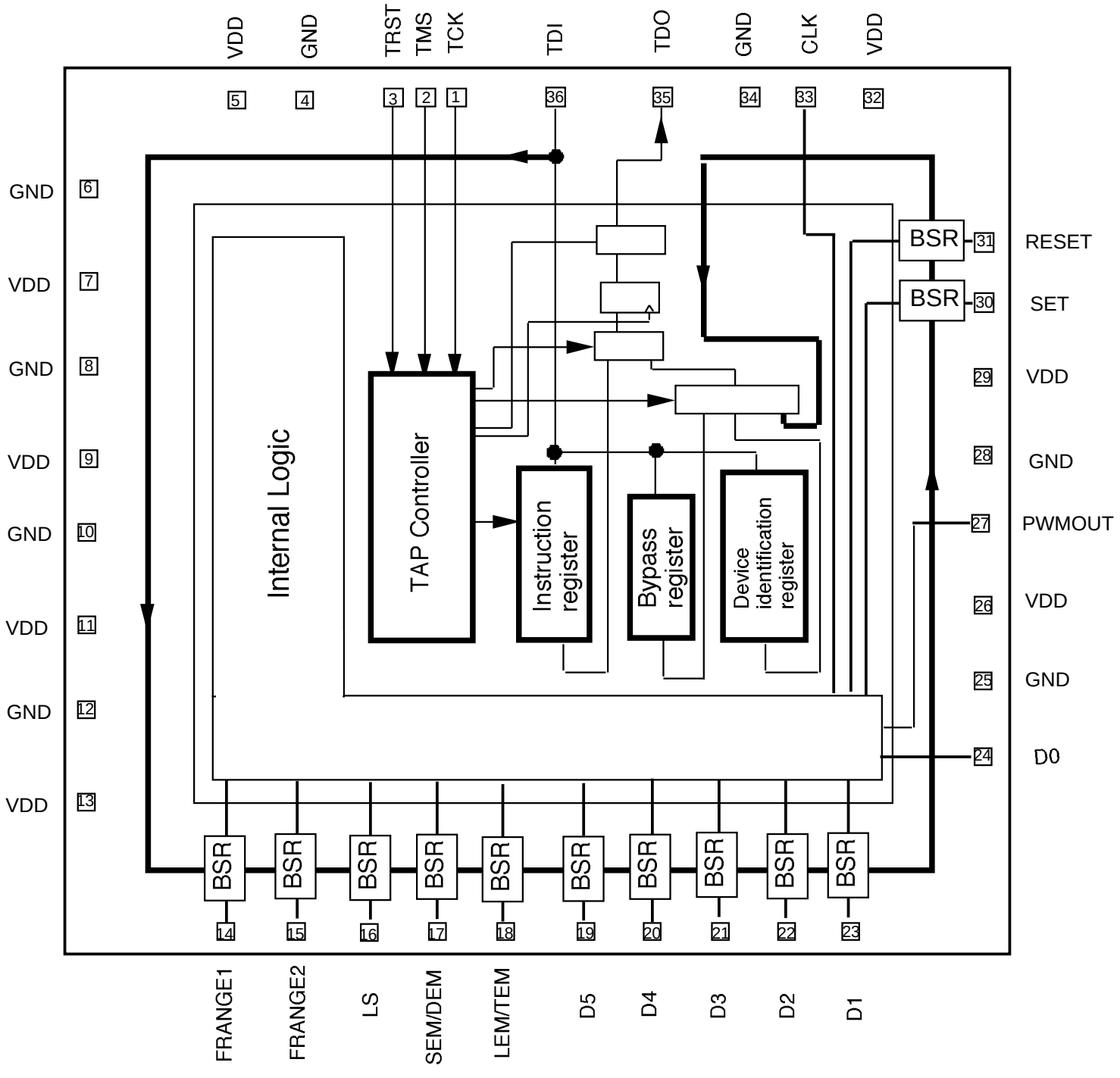
•Test Mode Select Input (TMS)
The signal received at TMS is decoded by the TAP controlled to control test operation.
The signal presented at TMS is sampled by the test logic on the rising edge of TCK.

•Test Data Input (TDI)
Serial test instructions and data are received by the test logic at TDI.
The signal presented at TDI is sampled by the test logic on the rising edge of TCK.

•Test Reset Input (TRST)
The TRST input provides for asynchronous initialization of the TAP controller.
If TRST is included in the TAP, then the TAPcontroller is asynchronously reset to the Test-Logic-Reset controller state when a logic 0 is applied to TRST.

•Test Data Input (TDO)
TDO is a serial output for test instructions and data from the test logic defined in this standard.
Changes in the state of the signal driven through TDO occur only on the falling edge of TCK. The TDO driver is set to its inactive drive state except when the scanning of data is in progress.

BLOCK DIAGRAM OF TEST CIRCUIT



NOTE1 : **BSR routing order = FRANGE1→FRANGE2→LS →SEMDEM→ LEMTEM→D5→D4→D3→D2→D1→D0 →SET →RESET**

NOTE2 : CLK(33pin) and PWMOUT(27pin) do not have BSR.

TAP CONTROLLER DESCRIPTION

The TAP controller is a synchronous finite state machine that responds to change at the TMS and TCK signals of the TAP and controls the sequence of operations of the circuitry defined by this standard.

The state diagram for the TAP controller is shown in following figure.

All state transitions of the TAP controller occur on the value of TMS at the time of a rising edge of TCK.

INSTRUCTION DESCRIPTION

INSTRUCTION SET

Instruction	Code (Binary)	Selected TDR
EXTEST	000	BSR (Boundary Scan Register)
IDCODE	001	DIR (Device Identification Register)
SAMPLE/PRELAOD	010	BSR
BYPASS	111	BPR (Bypass Register)

EXTEST INSTRUCTION

EXTEST instruction allows testing of off-cihp circuitry and board level interconnections. Data would typically be loaded onto the latched parallel outputs of boundary-scan shift-register stages using the SAMPLE/PRELOAD instruction prior to selection of the EXTEST instruction.

The EXTEST instruction select only the BSR(Boundary-scan register) to be connected for serial access between TDI and TDO in the Shift-DR controller state.

When the EXTEST instruction is selected, the state of all signals received at system input pins are loaded into the boundary-scan register on the rising edge of TCK in the Capture-DR controller state.

PWMOUT pin does not have BSR, so PWMOUT pin can not test interconnection to board using the EXTEST instruction.

BYPASS INSTRUCTION

The bypass register contains a single shift-register stage and is used to provided a minimum-length serial path between the TDI and the TDO pins of a M66244FP when no test operation of M66244FP is required.

This allows more rapid movement of test data to and from other components on a board that are required to perform test operations.

The BYPASS instruction select the bypass register to be connected for serial access between TDI and TDO in the Shift-DR controller state.

SAMPLE/PRELOAD INSTRUCTION

The SAMPLE/PRELOAD instruction allows a snapshot of normal operation of the component to the taken and examined. It also allows data values to be loaded onto the latched parallel outputs of the boundary-scan shift register prior to selection of the other boundary-scan test instruction.

The SAMPLE/PRELOAD instruction select only the boundary-scan register to be connected for serial access between TDI and TDO in the Shift-DR controller state.

When SAMPLE/PRELOAD instruction is selected, the state of all signals flowing through system pins are loaded into the register on the rising edge of TCK in the Capture-DR controller state.
When SAMPLE/PRELOAD instruction is selected, parallel output registers/latches included in boundary-scan register cells load the data held associated shift-register stage on the falling edge of TCK in the Update-DR controller state.

IDCOAD INSTRUCTION

Use of the device identification register allows a code to be serially read from the component that shows:

(1)The version number for the part
(2)The part number
(3)The manufacturer's identity

The IDCODE instruction select only the device identification register to be connected for serial access between TDI and TDO in the Shift-DR controller state.
When the IDCODE instruction is selected, the vendor identification code is loaded into the device identification register on the rising edge of TCK following entry into Capture-DR controller state.

ID code of M66244FP is as follow;

Version (4bit)	bit num.	31 30 29 28	
	code	0 0 0 0	
Part num. (16bit)	bit num.	27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12	binary code of "6244"
	code	0 0 0 1 1 0 0 0 0 1 1 0 0 1 0 0	
Manufacture num. (11bit)	bit num.	11 10 9 8 7 6 5 4 3 2 1	JEDEC code of MITSUBISHI
	code	0 0 0 0 0 0 1 1 1 0 0	
LSB (4bit)	bit num.	0	fixed value
	code	1	

