M64895BFP/GP

I²C BUS FREQUENCY SYNTHESIZER FOR TV/VCR

DESCRIPTION

The M64895B is a semiconductor integrated circuit consisting of PLL frequency synthesizer for TV/VCR using I²C BUS control. It contains the prescaler with operating up to1.3GHz, 4 band drivers and tuning Amplifier for direct tuning. Built-in 4 band drivers.

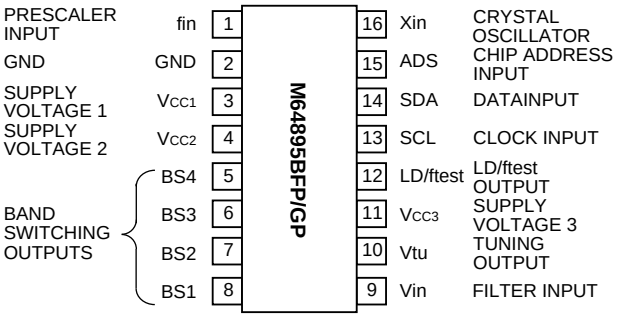
FEATURES

- 4 integrated PNP band drivers (Io=40mA,Vsat=0.2V typ@Vcc1 to 13.2V)
- Built-in high-withstanding voltage tuning Amplifier
- Low power dissipation (Icc=20mA, Vcc=5V)
- Built-in prescaler with input amplifier (Fmax=1.3GHz)
- PLL lock/unlock status display out put
- (Built-in pull up resistor)
- I²C bus control (write mode only)
- X'tal 4MHz is used to realize 3 type of tuning steps (Division ratio 1/512, 1/640, 1/1024)
- Programmable chip address
- Small package (16Pin SOP/SSOP)

APPLICATION

TV, VCR tuners

PIN CONFIGURATION (TOP VIEW)



Outline 16P2S-A/16P2Z-A

RECOMMENDED OPERATING CONDITION

Supply voltage range.....V_{CC1}=4.5 to 5.5V

V_{CC2}=V_{CC1} to 13.2V

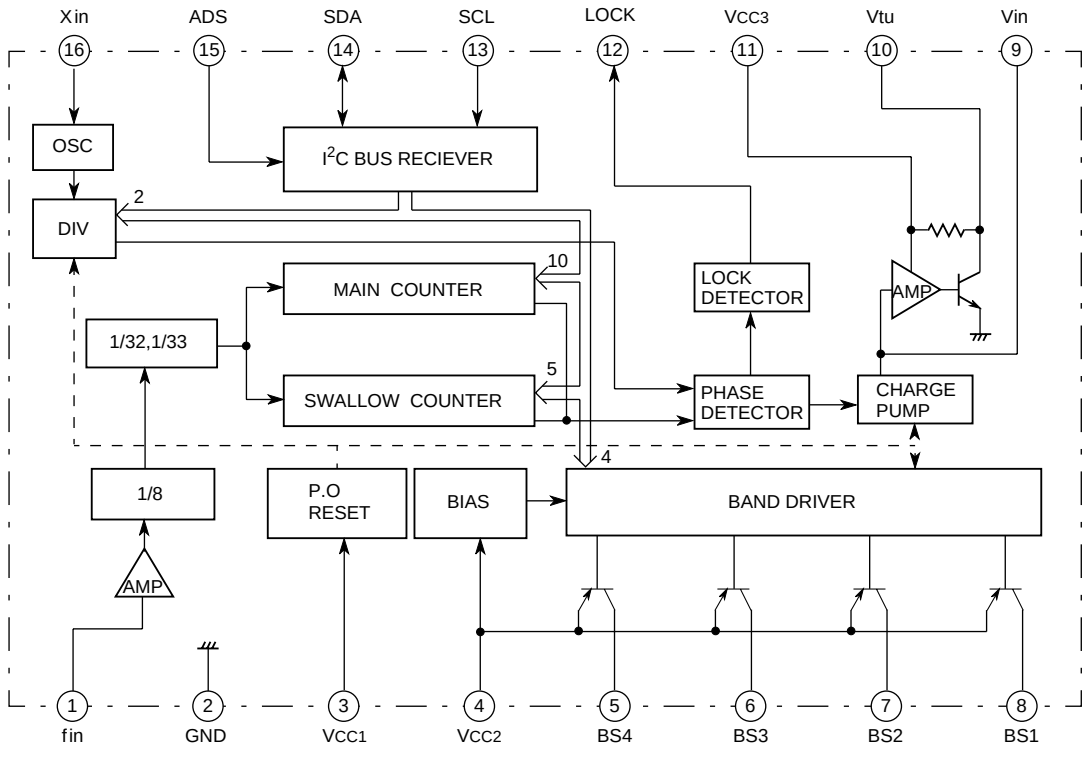
V_{CC3}=28 to 35V

Rated supply voltage.....V_{CC1}=5V

V_{CC2}=12V

V_{CC3}=33V

BLOCK DIAGRAM



DESCRIPTION OF PIN

Pin No.	Symbol	Pin name	Function
1	f in	Prescaler input	Input for the VCO frequency.
2	GND	GND	Ground to 0V.
3	V_{CC1}	Power supply voltage 1	Power supply voltage terminal. 5.0V±0.5V
4	V_{CC2}	Power supply voltage 2	Power supply for band switching, Vcc1 to 13.2V
5 6 7 8	BS4 BS3 BS2 BS1	Band switching outputs	PNP open collector method is used. When the band switching data is "H",the output is ON. When it is "L",the output is OFF.
9	Vin	Filter input (Charge pump output)	This is the output terminal for the LPF input and charge pump output. When the phase of the programmable divider output (f1/N) is ahead compared to the reference frequency (f_{REF}), the "source" current state becomes active. If it is behind, the "sink" current becomes active. If the phases are the same, the high impedance state becomes active.
10	Vtu	Tuning output	This supplies the tuning voltage.
11	V_{CC3}	Power supply voltage 3	Power supply voltage for tuning voltage 28 to 35V
12	LD/ftest	Lock detectt/ Test port	Lock detector is output. Programmabule freq. Divider output and reference freq. output is selected by the test mode.
13	SCL	Clock input	Data is read into the shift register when the clock signal falls
14	SDA	Data input	Input for band SW and programmable freq. divider set up.
15	ADS	Address switching input	Chip address sets it up with the input condition of terminal.
16	Xin	This is connected to the crystal oscillator.	4.0MHz crystal oscillator is connected.

ABSOLUTE MAXIMUM RATINGS (Ta=-20°C to +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC1}	Super voltage 1	Pin3	6.0	V
V_{CC2}	Super voltage 2	Pin4	14.4	V
V_{CC3}	Super voltage 3	Pin11	36.0	V
V_I	Input voltage	Not to exceed V_{CC1}	6.0	V
V_O	Output voltage	Pin16	6.0	V
V_{BSOFF}	Voltage applied when the band output is OFF	per 1 band output circuit 50mA per 1 band output	14.4	V
I_{BSON}	Band output current	circuit	50.0	mA
t_{BSON}	ON the time when the band output is ON	3circuits are pn at same time	10	sec
P_d	Power dissipation	Ta=75°C	470	mW
T_{opr}	Operating temperature		-20 to +75	°C
T_{stg}	Storage temperature		-40 to +125	°C

RECOMMENDED OPERATING CONDITIONS (Ta=-20°C to +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC1}	Super voltage 1	Pin3	4.5 to 5.5	V
V_{CC2}	Super voltage 2	Pin4	V_{CC1} to 13.2	V
V_{CC3}	Super voltage 3	Pin11	28 to 35	V
f_{opr1}	Operating frequency (1)	Crystal oscillation circuit	4.0	MHz
f_{opr2}	Operating frequency (2)		80 to 1300	MHz
I_{BDL}	Band output current 5 to 8	Normally 1 circuit is on. 2 circuits on at the same time is max. It is prohibited to have 3 or more circuits turned on at the same time.	0 to 40	mA

ELECTRICAL CHARACTERISTICS (Ta=-20°C to +75°C, unless otherwise noted, V_{CC1}=5.0V, V_{CC2}=12V, V_{CC3}=33V)

Symbol	Parameter		Test pin	Test conditions	Limits			Unit
					Min.	Typ.	Max.	
V_{IH}	Input terminals	"H" input voltage	13 to 14		3.0	–	V_{CC1}+0.3	V
V_{IL}		"L" input voltage	13 to 14		–	–	1.5	V
I_{IH}		"H" input current	13 to 14	V_{CC1}=5.5V, Vi=4.0V	–	–	10	µA
I_{IL}		"L" input current	13/14	V_{CC1}=5.5V, Vi=0.4V	–	-4/-14	-10/-30	µA
V_{OL}	SDA output	"L" output voltage	14	V_{CC1}=5.5V, Io=3mA	–	–	0.4	µA
I_{LO}		Leak current	14	V_{CC1}=5.5V, Vo=5.5V	–	–	10	µA
V_{BS}	Band SW	Output voltage	5 to 8	V_{CC2}=12V, Io=-40mA	11.6	11.8	–	V
I_{OLK1}		Leak current	5 to 8	V_{CC2}=12V band SW is OFF Vo=0V	–	–	-10	µA
V_{toH}	Tuning output	Output voltage "H"	10	V_{CC3}=33V	32.5	–	–	V
V_{toL}		Output voltage "L"	10	V_{CC3}=33V	–	0.2	0.4	V
I_{OH}	Charge pump	"H" output current	9	V_{CC1}=5.0V, Vo=2.5V	–	±270	±370	µA
I_{OL}		"L" output current	9	V_{CC1}=5.0V, Vo=2.5V	–	±70	±110	µA
I_{CPLK}		Leak current	9	V_{CC1}=5.0V, Vo=2.5V	–	–	±50	nA
I_{CC1}	Supply current 1		3	V_{CC1}=5.5V	–	20	30	mA
I_{CC2A}	Supply current 2	4 circuits: OFF	4	V_{CC2}=12V	–	–	0.3	mA
I_{CC2B}		1 circuits: ON, Output: OPEN	4	V_{CC2}=12V	–	6.0	8.0	mA
I_{CC2C}		Output current 40mA	4	V_{CC2}=12V Io=-40mA	–	46.0	48.0	mA
I_{CC3}	Supply current 3		11	V_{CC3}=33V Output ON	–	3.0	4.0	mA

The typical values are at V_{CC1}=5.0V V_{CC2}=12V V_{CC3}=33V, Ta=+25°C.

SWITCHING CHARACTERISTICS (Ta=-20°C to +75°C, unless otherwise noted, V_{CC1}=5.0V, V_{CC2}=12V, V_{CC3}=33V)

Symbol	Parameter	Test pin	Test conditions		Limits			Unit
					Min.	Typ.	Max.	
f_{opr}	Prescaler operating frequency	1	V_{CC1}=4.5 to 5.5V Vin=Vinmin to Vinmax		80	–	1300	MHz
Vin	Operating input voltage	1	V_{CC1}=4.5 to 5.5V	80 to 100MHz	-24	–	4	dBm
				100 to 200MHz	-27	–	4	
				200 to 800MHz	-30	–	4	
				800 to 1000MHz	-27	–	4	
				1000 to 1300MHz	-18	–	4	
f_{SCL}	Clock pulse frequency	13	V_{CC1}=4.5 to 5.5V		0	–	100	kHz
t_{BUF}	Bus free time	14	V_{CC1}=4.5 to 5.5V		4.7	–	–	µs
$t_{HD_{STA}}$	Data hold time	13	V_{CC1}=4.5 to 5.5V		4	–	–	µs
t_{LOW}	SCL low hold time	13	V_{CC1}=4.5 to 5.5V		4.7	–	–	µs
t_{HIGH}	SCL high hold time	13	V_{CC1}=4.5 to 5.5V		4	–	–	µs
$t_{SU_{STA}}$	Set up time	13, 14	V_{CC1}=4.5 to 5.5V		4.7	–	–	µs
$t_{HD_{DAT}}$	Data hold time	13, 14	V_{CC1}=4.5 to 5.5V		0	–	–	s
$t_{SU_{DAT}}$	Data set up time	13, 14	V_{CC1}=4.5 to 5.5V		250	–	–	ns
t_r	Rise time	13, 14	V_{CC1}=4.5 to 5.5V		–	–	1000	ns
t_f	Fall time	13, 14	V_{CC1}=4.5 to 5.5V		–	–	300	ns
$t_{SU_{STO}}$	Set up time	13, 14	V_{CC1}=4.5 to 5.5V		4	–	–	µs

METHOD OF SETTING DATA

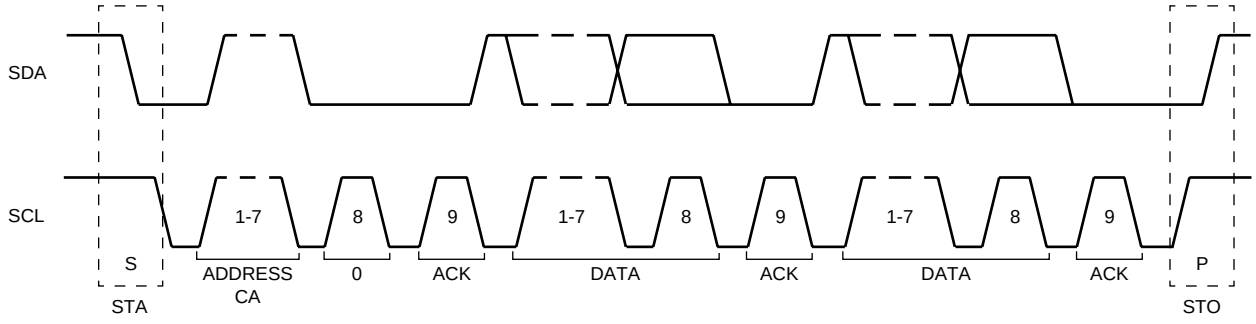
The input information to consit of 2 or data of 4bytes to lead to Chip Address is received in I²Cbus receiver. It shows a definition of bus protocol admitted in the following.

1_STA CA CB BB STO
2_STA CA D1 D2 STO
3_STA CA CB BB D1 D2 STO
4_STA CA D1 D2 CB BB STO

STA : Start condition
STO : Stop condition
CA : Chip address
CB : Control data byte
BB : BandS.W. data byte
D1 : Divider data byte
D2 : Divider data byte

The information of 5 bytes necessary for circuit operation is chip address and control data, bandS.W. data of 2 bytes and divider byte of 2 bytes. After the chip address input, 2 or data of 4 bytes are received.

Function bit is contained the first and the third data byte to distinguish between divider data and control data, band data, and "0" goes ahead of divider data, and "1" goes ahead of control data, bandS.W. data.



Write mode format

Byte	MSB								LSB
Address Byte	1	1	0	0	0	MA1	MA0	0	A
Devider Byte1	0	N14	N13	N12	N11	N10	N9	N8	A
Devider Byte2	N7	N6	N5	N4	N3	N2	N1	N0	A
Control Byte1	1	CP	T2	T1	T0	RSa	RSb	OS	A
Band SW Byte	X	X	X	X	BS4	BS3	BS2	BS1	A

TEST MODE DATA SET UP METHOD

Test Mode Bit Set Up

X : Random, 0 or 1. normal "0"

MA1 ,MA0 : Programmabule Address Bit

Address input voltage	MA1	MA0
0 to 0.1∗V_{CC1}	0	0
Always valid	0	1
0.4∗V_{CC1} to 0.6*V_{CC1}	1	0
0.9∗V_{CC1} to V_{CC1}	1	1

N14 to N0 : How to set dividing ratio of the programable the divider

Dividing ratio=N14(2^{14}=16384)+ ··· +N0(2^0=1)

Therefore, the range of division N is 1,024 to 32,768

Example) fvco=f_{REF}×8×N

=3.90625×8×N

=31.25×N (kHz)

CP: Setting up the charge pump current of the phase comparator

CP	Charge pump current	Mode
0	70μA	Test
1	270μA	Normal

T2,T1,T0 : Setting up for the test mode

T2 T1 T0	Charge pump	Pin 12 condition	Mode
0 0 X	Normal operation	Lock output	Normal operation
0 1 X	High impedance	Lock output	Test mode
1 1 0	Sink	Lock output	Test mode
1 1 1	Source	Lock output	Test mode
1 0 0	High impedance	f_{REF} output	Test mode
1 0 1	High impedance	f1/N output	Test mode

RSa, RSb : Set up for the reference frequency division ratio

RSa	RSb	Division ratio
1	1	1/512
0	1	1/1024
X	0	1/640

OS : Set up the tuning amplifier

OS	Tuning voltage output	Mode
0	ON	Normal
1	OFF	Test

Power on reset operation (Initial state the power is turned ON)

BS4 to BS1 : OFF

Charge pump : High impedance

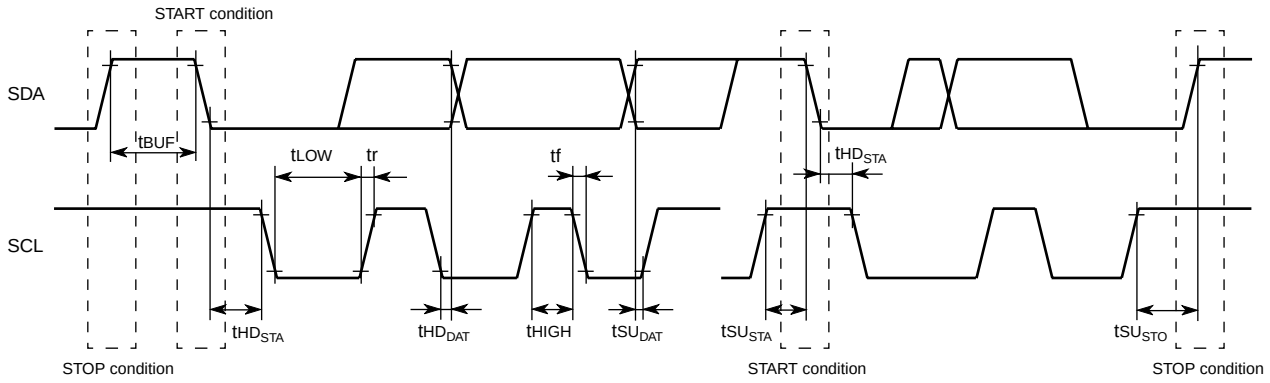
Tuning amplifier : OFF

Charge pump current : 270μA

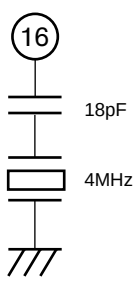
Frequency division ratio : 1/1024

Lock detector : High

TIMING DIAGRAM

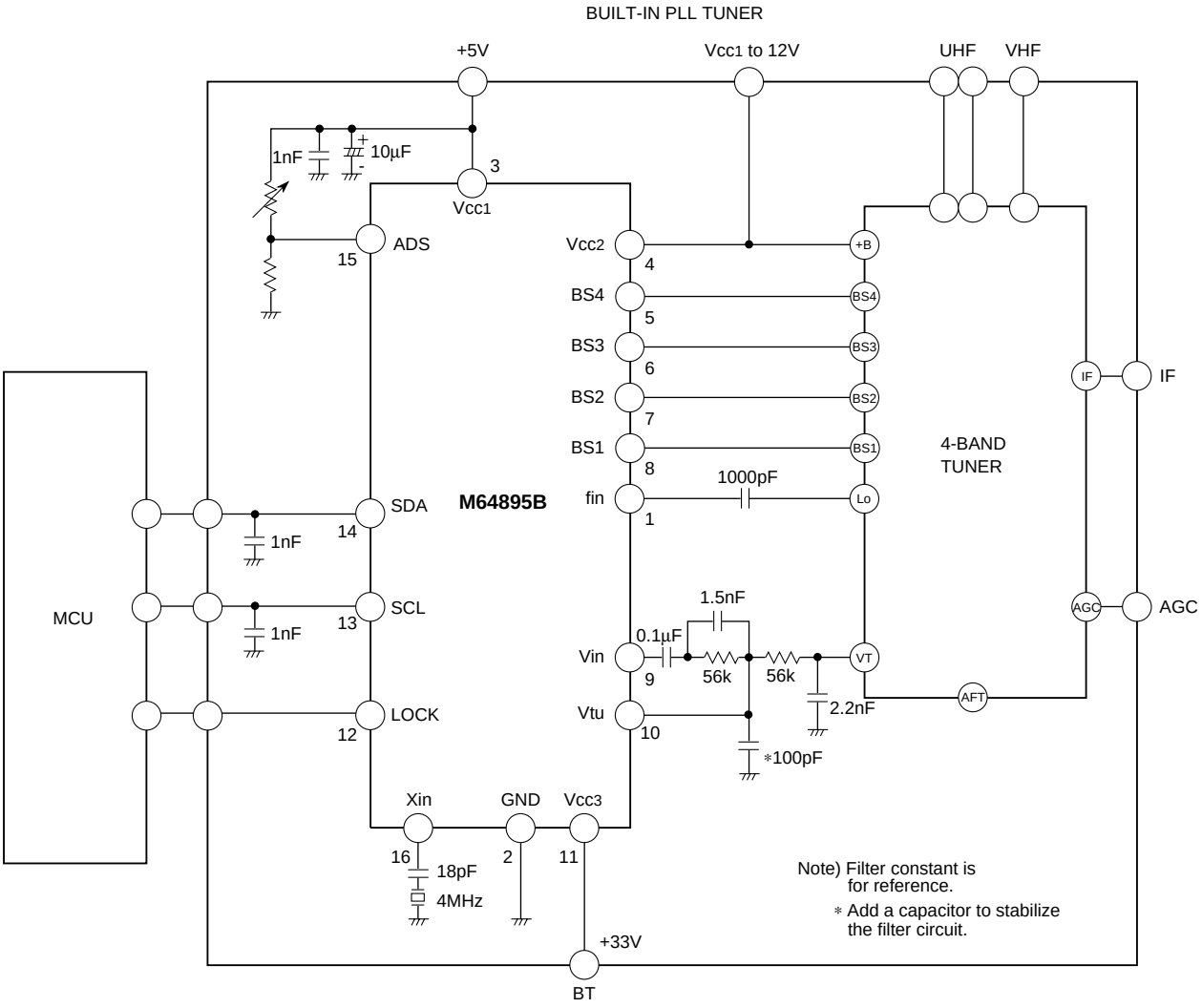


CRYSTAL OSCILLATOR CONNECTION DIAGRAM



Crystal oscillator characteristics
Actual resistance : less then 300Ω
Load capacitance : 20pF

APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F